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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	WDT
Number of I/O	13
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	32 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8e00010pec

PIN DESCRIPTION

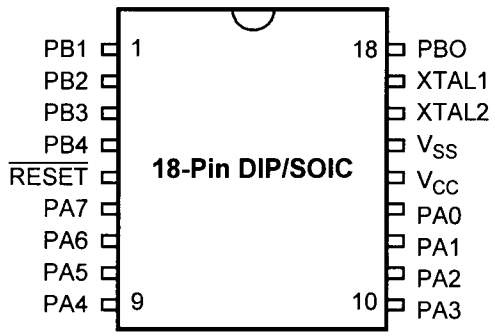


Figure 3. 18-Pin DIP/SOIC Pin Identification

Table 1. 18-Pin DIP/SOIC Pin Assignments

Standard Mode			
Pin #	**Symbol**	**Function**	**Direction**
1–4	PB1–PB4	Port B, Pins 1,2,3,4	In/Output
5	$\overline{\text{RESET}}$	Reset	Input
6–9	PA7–PA4	Port A, Pins 7,6,5,4	In/Output
10–13	PA3–PA0	Port A, Pins 3,2,1,0	In/Output
14	V_{CC}	Power Supply	
15	V_{SS}	Ground	
16	XTAL2	Crystal Oscillator Clock	Output
17	XTAL1	Crystal Oscillator Clock	Input
18	PB0	Port B, Pin 0	In/Output

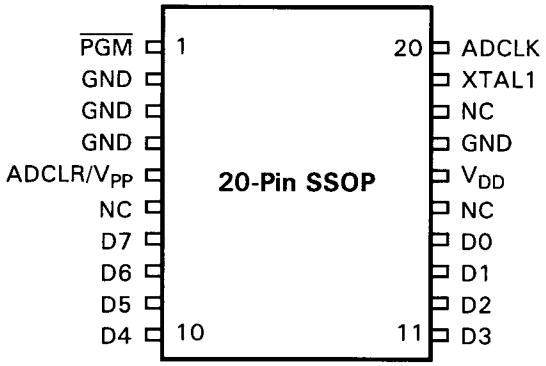


Figure 6. 20-Pin SSOP Pin Identification; EPROM Programming Mode

Table 4. 20-Pin SSOP Pin Assignments; EPROM Programming Mode

EPROM Programming Mode

Pin #	Symbol	Function	Direction
1	$\overline{PGM}$	Program Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clock/Program Voltage	Input
6	NC	No Connection	
7–10	D7–D4	Data 7,6,5,4	In/Output
11–14	D3–D0	Data 3,2,1,0	In/Output
15	NC	No Connection	
16	V_{DD}	Power Supply	
17	GND	Ground	
18	NC	No Connection	
19	XTAL1	1 MHz Clock	Input
20	ADCLK	Address Clock	Input

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on $\overline{RESET}$ Pin with Respect to V_{SS}	–0.6	V_{DD}+1	V	2
Total Power Dissipation		880	mW	
Maximum Allowable Current out of V_{SS}		80	mA	
Maximum Allowable Current into V_{DD}		80	mA	
Maximum Allowable Current into an Input Pin	–600	+600	mA	3
Maximum Allowable Current into an Open-Drain Pin	–600	+600	mA	4
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sunk by Port A		40	mA	
Maximum Allowable Output Current Sourced by Port A		40	mA	
Maximum Allowable Output Current Sunk by Port B		40	mA	
Maximum Allowable Output Current Sourced by Port B		40	mA	

Notes:
1. Applies to all pins except the $\overline{RESET}$ pin and where otherwise noted.
2. There is no input protection diode from pin to V_{DD}.
3. Excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings can cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period can affect device reliability. Total power dissipation should not exceed 880 mW for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})] + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{0L} \times I_{0L})$$

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 7).

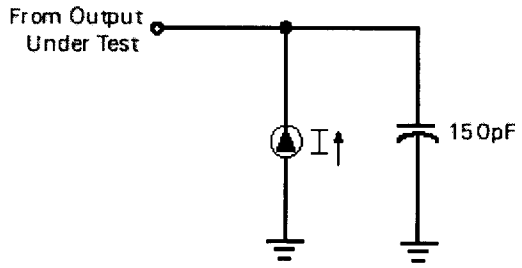


Figure 7. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

AC ELECTRICAL CHARACTERISTICS

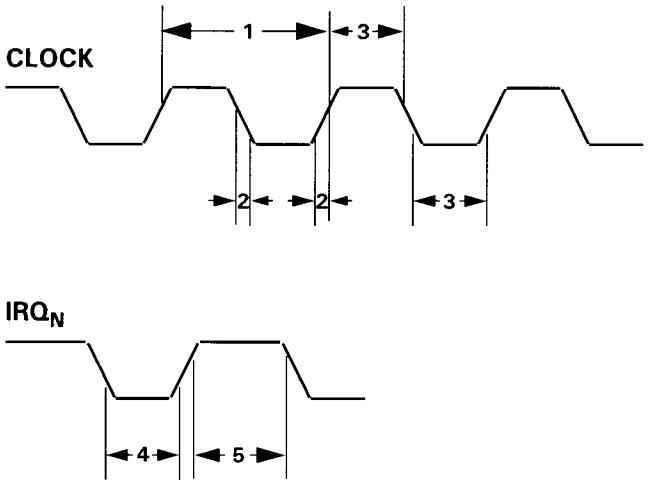


Figure 8. AC Electrical Timing Diagram

Table 5. Additional Timings

				T_A = –40°C to +105°C @ 10 MHz			
No	**Symbol**	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	3.5V	100	DC	ns	2
			5.5V	100	DC	ns	2
2	TrC,TfC	Clock Input Rise and Fall Times	3.5V		15	ns	2
			5.5V		15	ns	2
3	TwC	Input Clock Width	3.5V	50		ns	2
			5.5V	50		ns	2
4	TwIL	Int. Request Input Low Time	3.5V	70		ns	2
			5.5V	70		ns	2
5	TwIH	Int. Request Input High Time	3.5V	5TpC			2
			5.5V	5TpC			2
6	Twsm	STOP Mode Recovery Width Spec.	3.5V	12		ns	
			5.5V	12		ns	
7	Tost	Oscillator Start-Up Time	3.5V		5TpC		
			5.5V		5TpC		

Notes:
1. The V_{DD} voltage specification of 3.5V guarantees 3.5V. The V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

Z8PLUS CORE

The Z8E000 is based on the ZiLOG Z8Plus Core Architecture. This core is capable of addressing up to 64KBytes of program memory and 4KBytes of RAM. Register RAM is accessed as either 8- or 16-bit registers, using a combination of 4-, 8-, and 12-bit addressing modes. The architecture supports up to 15 vectored interrupts from external and internal sources. The processor decodes 44 CISC instructions, using six addressing modes. See the Z8Plus User's Manual for more information.

RESET

This section describes the Z8E000 reset conditions, reset timing, and register initialization procedures. Reset is generated by the Reset Pin, Watch-Dog Timer (WDT), and Stop-Mode Recovery (SMR).

A system reset overrides all other operating conditions and puts the Z8E000 into a known state. To initialize the chip's internal logic, the $\overline{\text{RESET}}$ input must be held Low for at least 30 XTAL clock cycles. The control registers and ports are reset to their default conditions after a reset from the $\overline{\text{RESET}}$ pin. The control registers and ports are not reset to their default conditions after wakeup from Stop Mode or WDT timeout.

During $\overline{\text{RESET}}$, the program counter is loaded with 0020H. I/O ports and control registers are configured to their default reset state. Resetting the Z8E000 does not affect the contents of the general-purpose registers.

RESET PIN OPERATION

The Z8E000 hardware $\overline{\text{RESET}}$ pin initializes the control and peripheral registers, as indicated in Table 6. Specific reset values are indicated by 1 or 0, while bits whose states are unchanged are indicated by the letter U.

$\overline{\text{RESET}}$ must first be held Low until the oscillator stabilizes. From than point, the pin then must be held for an additional 30 XTAL clock cycles to be sure that the internal reset is complete. The $\overline{\text{RESET}}$ pin has a Schmitt-Trigger input with a trip point. There is no High side protection diode. The user should place an external diode from $\overline{\text{RESET}}$ to V_{CC}. The internal pull-up resistor on the $\overline{\text{RESET}}$ pin is approximately 500 KΩ, typical.

Program execution starts 10 XTAL clock cycles after $\overline{\text{RESET}}$ has returned High. The initial instruction fetch is from location 0020H. Figure 9 indicates reset timing.

After a reset, the first routine executed must be one that initializes the TCTLHI control register to the required system configuration. This routine is then followed by initialization of the remaining control registers.

Table 6. Control and Peripheral Register Reset Values

Register		Bits								
(HEX)	Register Name	7	6	5	4	3	2	1	0	Comments
FF	Stack Pointer	0	0	U	U	U	U	U	U	Stack pointer is not affected by $\overline{\text{RESET}}$
FE	Reserved									
FD	Register Pointer	U	U	U	U	0	0	0	0	Register pointer is not affected by $\overline{\text{RESET}}$
FC	Flags	U	U	U	U	U	U	*	*	Only WDT & SMR flags are affected by $\overline{\text{RESET}}$
FB	Interrupt Mask	0	0	0	0	0	0	0	0	All interrupts masked by $\overline{\text{RESET}}$
FA	Interrupt Request	0	0	0	0	0	0	0	0	All interrupt requests cleared by $\overline{\text{RESET}}$
F9–F0	Reserved									
EF–E0	Virtual Copy									Virtual Copy of the Current Working Register Set
DF–D8	Reserved									
D7	PortB Spec. Func.	0	0	0	0	0	0	0	0	Deactivates all port special functions after $\overline{\text{RESET}}$
D6	PortB Directional Control	0	0	0	0	0	0	0	0	Defines all bits as inputs in PortB after $\overline{\text{RESET}}$
D5	PortB Output	U	U	U	U	U	U	U	U	Output register not affected by $\overline{\text{RESET}}$

RESET PIN OPERATION (Continued)

Table 6. Control and Peripheral Register Reset Values

Register		Bits								
(HEX)	Register Name	7	6	5	4	3	2	1	0	Comments
D4	PortB Input	U	U	U	U	U	U	U	U	Current sample of the input pin following $\overline{\text{RESET}}$
D3	PortA Spec. Func.	0	0	0	0	0	0	0	0	Deactivates all port special functions after $\overline{\text{RESET}}$
D2	PortA Directional Control	0	0	0	0	0	0	0	0	Defines all bits as inputs in PortA after $\overline{\text{RESET}}$
D1	PortA Output	U	U	U	U	U	U	U	U	Output register not affected by $\overline{\text{RESET}}$
D0	PortA Input	U	U	U	U	U	U	U	U	Current sample of the input pin following $\overline{\text{RESET}}$
CF	Reserved									
CE	Reserved									
CD	Reserved									
CC	Reserved									
CB	T3VAL	U	U	U	U	U	U	U	U	
CA	T2VAL	U	U	U	U	U	U	U	U	
C9	T3AR	U	U	U	U	U	U	U	U	
C8	T2AR	U	U	U	U	U	U	U	U	
C7	Reserved									
C6	Reserved									
C5	Reserved									
C4	Reserved									
C3	WDTHI	1	1	1	1	1	1	1	1	
C2	WDTLO	1	1	1	1	1	1	1	1	
C1	TCTLHI	1	1	1	1	1	0	0	0	WDT Enabled in HALT Mode, WDT timeout at maximum value, STOP Mode disabled
C0	TCTLLO	0	0	0	0	0	0	0	0	Standard timer is disabled

Note: *The SMR and WDT flags are set indicating the source of the RESET, as shown below:

D1	D0	Reset Source
0	0	$\overline{\text{RESET}}$ Pin
0	1	SMR Recovery
1	0	WDT Reset
1	1	Reserved

RESET PIN OPERATION (Continued)

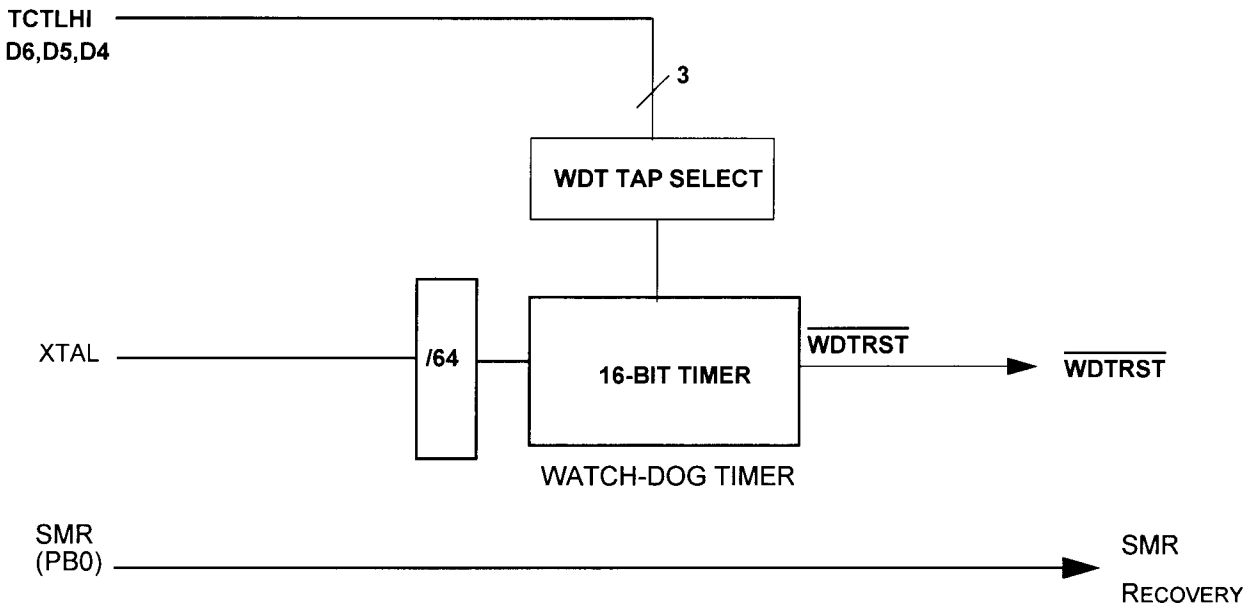


Figure 11. Z8E000 Reset Circuitry with WDT and SMR

Z8E000 WATCH-DOG TIMER (WDT) (Continued)

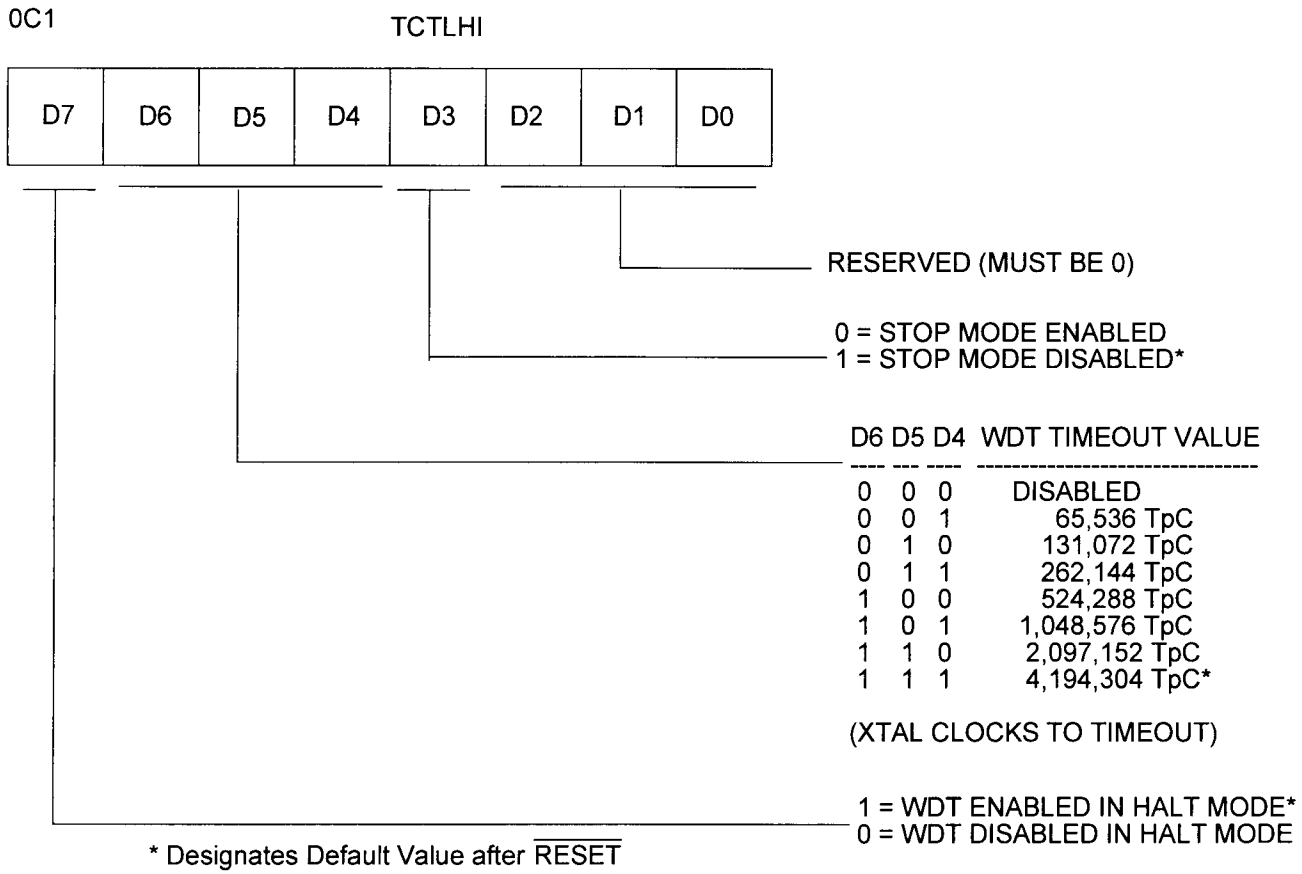


Figure 12. Z8E000 TCTLHI Register for Control of WDT

Note: The WDT can only be disabled via software if the first instruction out of RESET performs this function. Logic within the Z8E000 will detect that it is in the process of executing the first instruction after the part leaves RESET. During the execution of this instruction, the upper five bits of the TCTLHI register can be written. After this first instruction, hardware will not allow the upper five bits of this register to be written.

The TCTLHI bits for control of the WDT are described below:

WDT Time Select (D6, D5, D4). Bits 6, 5, and 4 determine the time-out period. Table 7 indicates the range of timeout values that can be obtained. The default values of D6, D5, and D4 are all 1, thus setting the WDT to its maximum timeout period when coming out of RESET.

Table 7. Time-Out Period of the WDT

D6	D5	D4	Crystal Clocks to Timeout	Time-Out Using a10 MHz Crystal
0	0	0	Disabled	Disabled
0	0	1	65,536 TpC	6.55 ms
0	1	0	131,072 TpC	13.11 ms
0	1	1	262,144 TpC	26.21 ms
1	0	0	524,288 TpC	52.43 ms
1	0	1	1,048,576 TpC	104.86 ms
1	1	0	2,097,152 TpC	209.72 ms
1	1	1	4,194,304 TpC	419.43 ms

Notes:
TpC = XTAL clock cycle.
The default on reset is D6 = D5 = D4 = 1.

WDT During HALT (D7). This bit determines whether or not the WDT is active during HALT Mode. A "1" indicates active during HALT. A "0" prevents the WDT from resetting the part while halted.Coming out of reset, the WDT will be enabled during HALT Mode.

STOP MODE (D3). Coming out of $\overline{\text{RESET}}$, the Z8E000 will have the STOP Mode disabled. If an application requires use of STOP Mode, bit D3 must be cleared immediately upon leaving $\overline{\text{RESET}}$. If bit D3 is set, the STOP instruction will execute as a NOP. If bit D3 is cleared, the STOP instruction will enter Stop Mode. Whenever the Z8E000 wakes up after having been in STOP Mode, the STOP Mode will be disabled once again.

Bits 2, 1 and 0. These bits are reserved and must be 0.

POWER-DOWN MODES

In addition to the standard RUN mode, the Z8E000 MCU supports two Power-Down modes to minimize device current consumption. The two modes supported are HALT and STOP.

HALT MODE OPERATION

The HALT Mode suspends instruction execution and turns off the internal CPU clock. The on-chip oscillator circuit remains active, so the internal clock continues to run and is applied to the timers and interrupt logic.

To enter the HALT Mode, the Z8E000 only requires a HALT instruction. It is NOT necessary to execute a NOP instruction immediately before the HALT instruction.

```
7F    HALT    ; enter HALT Mode
```

The HALT Mode can be exited by servicing an interrupt (either externally or internally). Upon completion of the interrupt service routine, the user program continues from the instruction after HALT.

The HALT Mode can also be exited via a $\overline{\text{RESET}}$ activation or a Watch-Dog Timer (WDT) timeout. In these cases, program execution will restart at the reset address 0020H.

RESET CONDITIONS

After a hardware $\overline{\text{RESET}}$, the timers are disabled. See Table 5 for timer control, value, and auto-initialization register status after $\overline{\text{RESET}}$.

I/O PORTS

The Z8E000 has 13 lines dedicated to input and output. These lines are grouped into two ports known as Port A and Port B. Port A is an 8-bit port that is bit-programmable as either inputs or outputs. Port B can be programmed to provide standard input/output or the following special functions: SMR input and external interrupt inputs.

All ports have push-pull CMOS outputs. In addition, the outputs of Port A, on a bit-wise basis, can be configured for open-drain operation. As such, the register values for "/" at a given bit position only affect the bit in question.

Each port is defined by a set of four control registers. See Figure 21.

Directional Control and Special Function Registers

Each port on the Z8E000 has an associated and dedicated Directional Control Register that determines on a bit-wise basis whether a given port bit will operate as an input or as an output.

Each port on the Z8E000 has a Special Function Register that, in conjunction with the directional control register, implements on a bit-wise basis, and supports special functionality that can be defined for each particular port bit.

Input and Output Value Registers

Each port has an Output Value Register and an Input Value Register. For port bits configured as an input by means of the Directional Control Register, the Input Value Register for that bit position will contain the current synchronized input value.

REGISTER	ADDRESS	IDENTIFIER
Port B SPECIAL FUNCTION	0D7H	PTBSFR
Port B DIRECTIONAL CONTROL	0D6H	PTBDIR
Port B OUTPUT VALUE	0D5H	PTBOUT
Port B INPUT VALUE	0D4H	PTBIN
Port A SPECIAL FUNCTION	0D3H	PTASFR
Port A DIRECTIONAL CONTROL	0D2H	PTADIR
Port A OUTPUT VALUE	0D1H	PTAOUT
Port A INPUT VALUE	0D0H	PTAIN

Figure 21. Z8E000 I/O Ports Registers

For port bits configured as an output by means of the Directional Control Register, the value held in the corresponding bit of the Output Value Register is driven directly onto the output pin. The opposite register bit for a given pin (the output register bit for an input pin and the input register bit for an output pin) will hold their previous value. They will not be changed by hardware nor will they have any effect on the hardware.

READ/WRITE OPERATIONS

The control for each port is done on a bit-wise basis. All bits are capable of operating as inputs or outputs, depending upon the setting of the port's directional control register. If configured as an input, each bit is provided a Schmitt-trigger. The output of the Schmitt-trigger is latched twice to perform a synchronization function, while the output of the synchronizer is fed to the port input register, which can be read by software.

A write to a port input register has the effect of updating the contents of the input register, but subsequent reads will not necessarily return the same value that was written. If the bit in question is defined as an input, the input register for that bit position will contain the current synchronized input value. Thus, writes to that bit position will be overwritten on the next clock cycle with the newly sampled input data. However, if the particular port bit is programmed as an output, the input register for that bit will retain the software-updated value. The port bits that are programmed as outputs do not sample the value being driven out.

Any bit in either port can be defined as an output by setting the appropriate bit in the directional control register. If such is the case, the value held in the appropriate bit of the port output register is driven directly onto the output pin.

Note: The above result does not necessarily reflect the actual output value. If an external error is holding an output pin either High or Low against the output driver, the software read will return the *required* value, not the actual state caused by the contention. When a bit is defined as an output, the Schmitt-trigger on the input will be disabled to save power.

Updates to the output register will take effect based upon the timing of the internal instruction pipeline; however, this timing is referenced to the rising edge of the clock. The output register can be read at any time, and will return the current output value that is held. No restrictions are placed on the timing of reads and/or writes to any of the port registers with respect to the others, but care should be taken when updating the directional control and special function registers.

When updating a directional control register, the special function register should first be disabled. If this precaution is not taken, spurious events could take place as a result of the change in port I/O status. This precaution is especially important when defining changes in Port B, as the spurious event referred to above could be one or more interrupts. Clearing of the SFR register should be the first step in configuring the port, and setting the SFR register should be the final step in the port configuration process. To ensure deterministic behavior, the SFR register should not be written until the pins are being driven appropriately and all initialization has been completed.

PORT A

Port A is a general-purpose port (Figure 23). Each of its lines can be independently programmed as input or output via the Port A Directional Control Register (PTADIR at 0D2H) as seen in Figure 22. A bit set to a "1" in PTADIR configures the corresponding bit in Port A as an output, while a bit cleared to "0" configures the corresponding bit in Port A as an input.

The input buffers are Schmitt-triggered. Bits programmed as outputs can be individually programmed as either push-pull or open drain by setting the corresponding bit in the Special Function Register (PTASFR, Figure 27.)

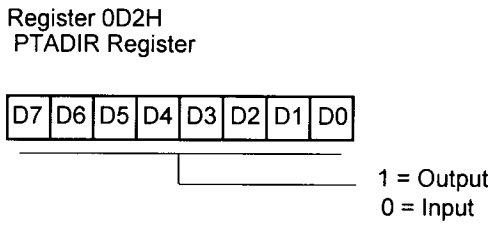


Figure 22. Port A Directional Control Register

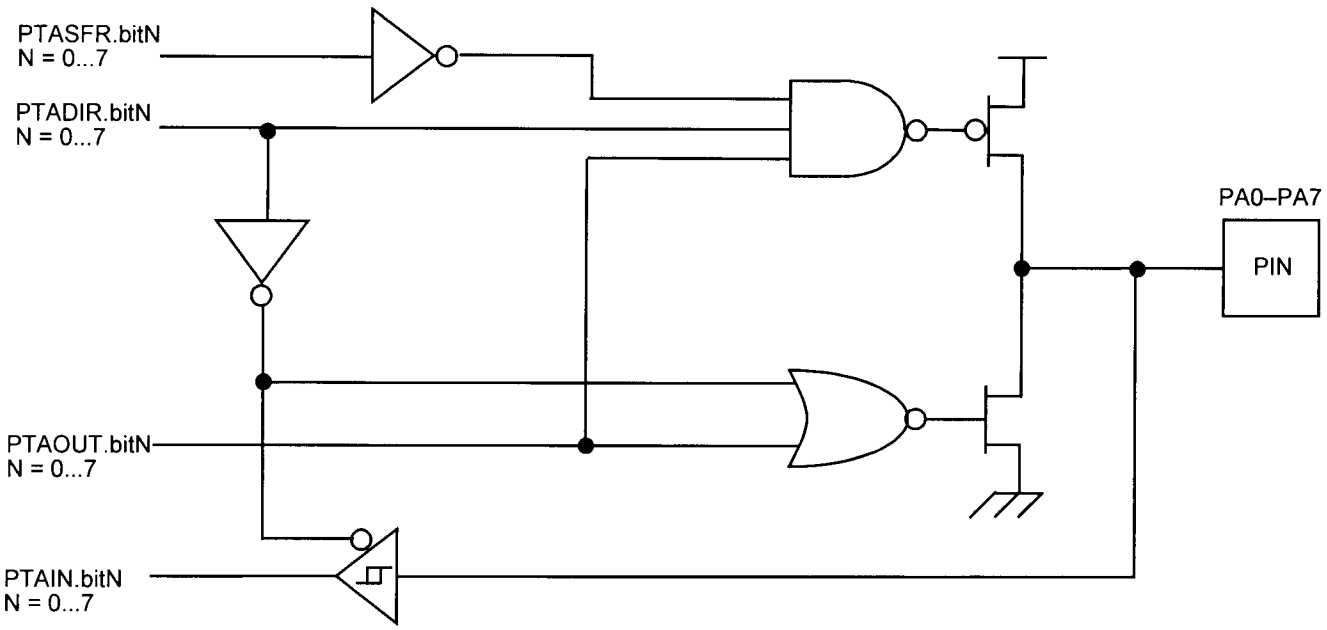


Figure 23. Port A Configuration with Open-Drain Capability and Schmitt-Trigger

PORT B

Port B Description

Port B is a 5-bit, bidirectional, CMOS-compatible I/O port. These five I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered. See Figure 29 through Figure 33 for diagrams of all five Port B pins.

In addition to standard input/output capability on all five pins of Port B, each pin provides special functionality as indicated in Table 8:

Table 8. Port B Special Functions

Port Pin	Input Special Function	Output Special Function
PB0	Stop Mode Recovery Input	None
PB1	None	None
PB2	IRQ3	None
PB3	None	None
PB4	IRQ1/IRQ4	None

Special functionality is invoked via the Port B Special Function Register. See Figure 28 for the arrangement and control conventions for this register.

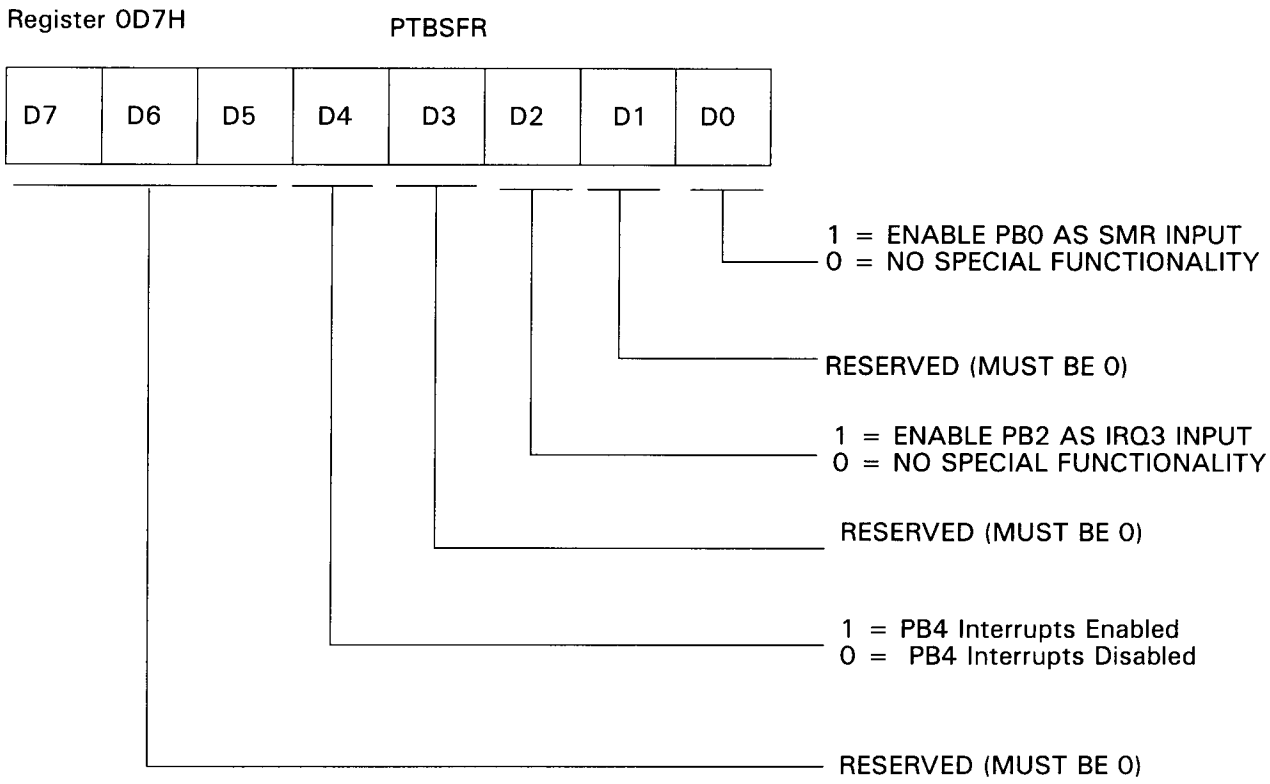


Figure 28. Port B Special Function Register

PORT B—PIN 0 CONFIGURATION

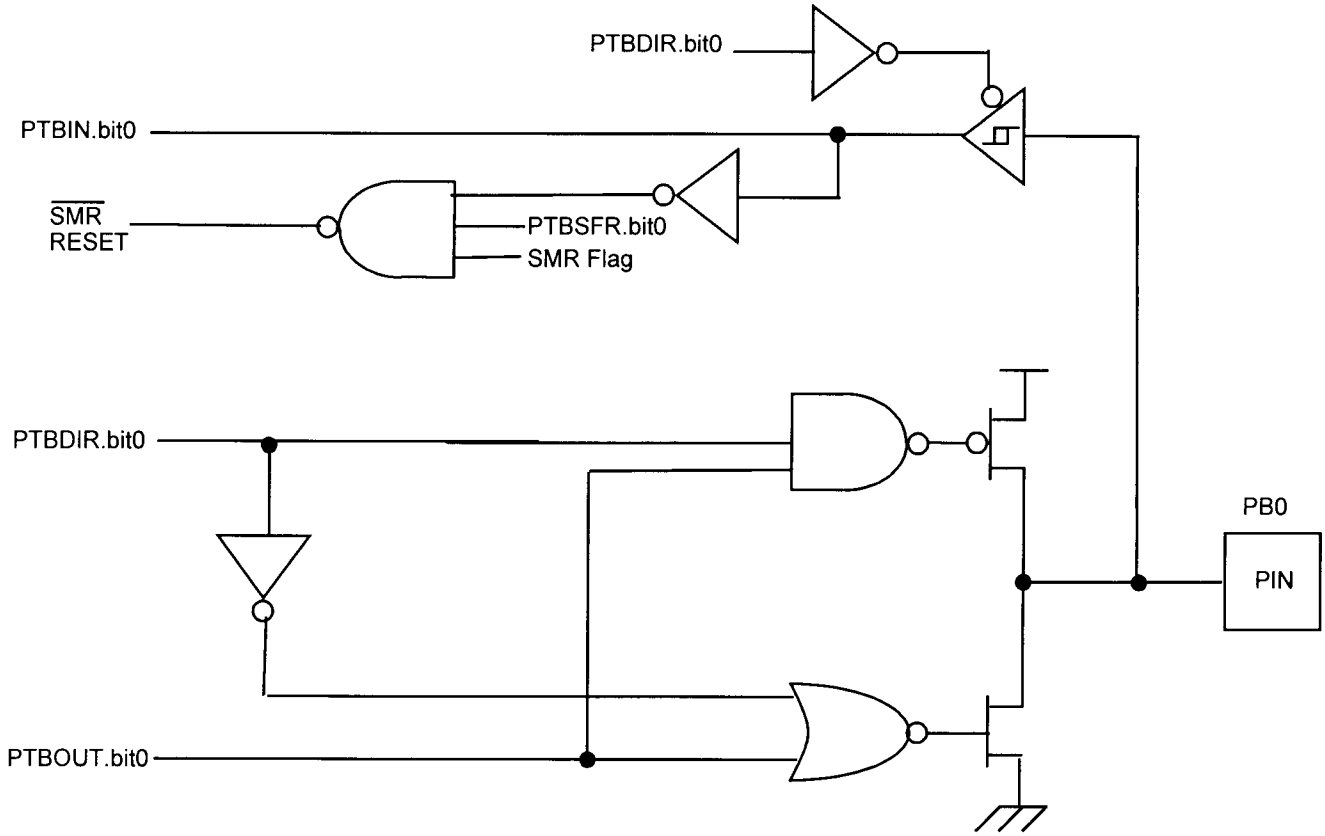


Figure 29. Port B Pin 0 Diagram

PORT B—PIN 1 CONFIGURATION

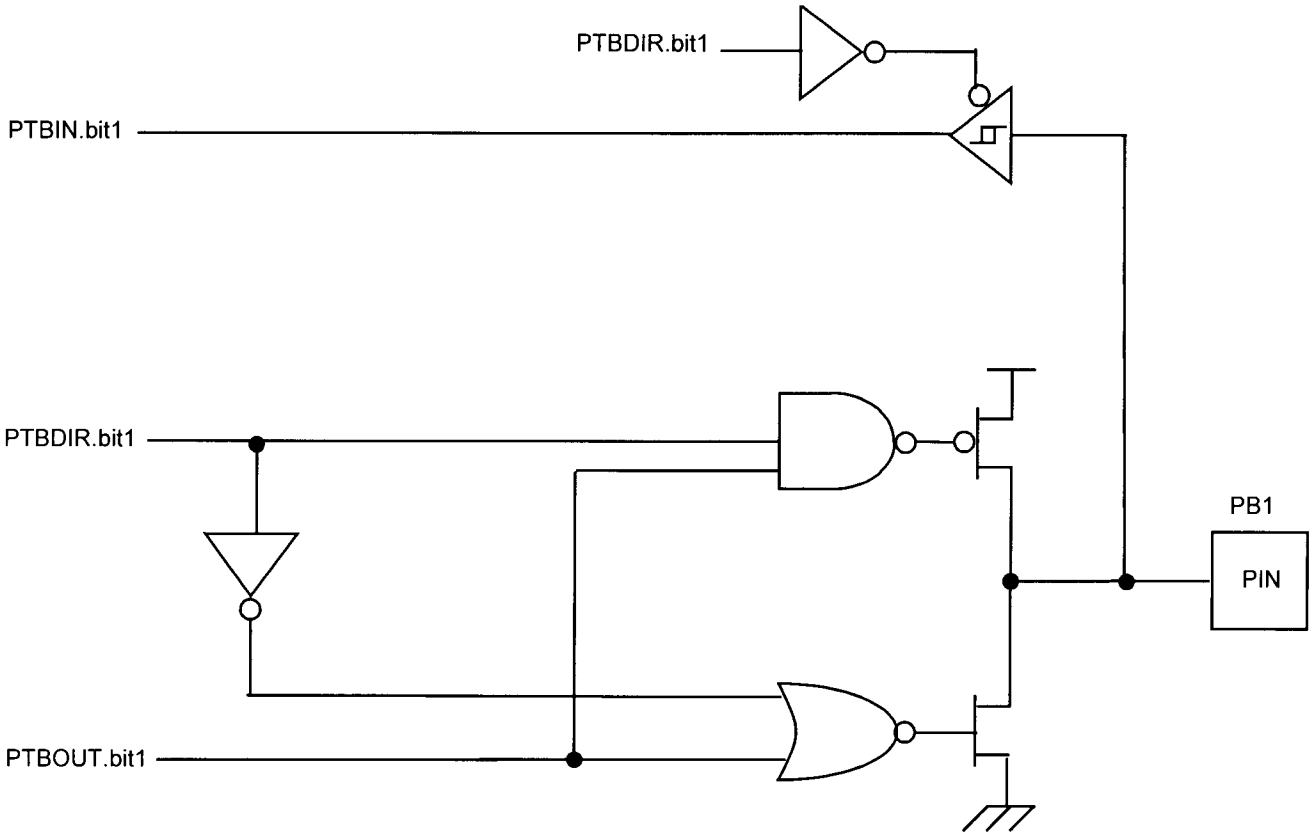


Figure 30. Port B Pin 1 Diagram

PORT B—PIN 2 CONFIGURATION

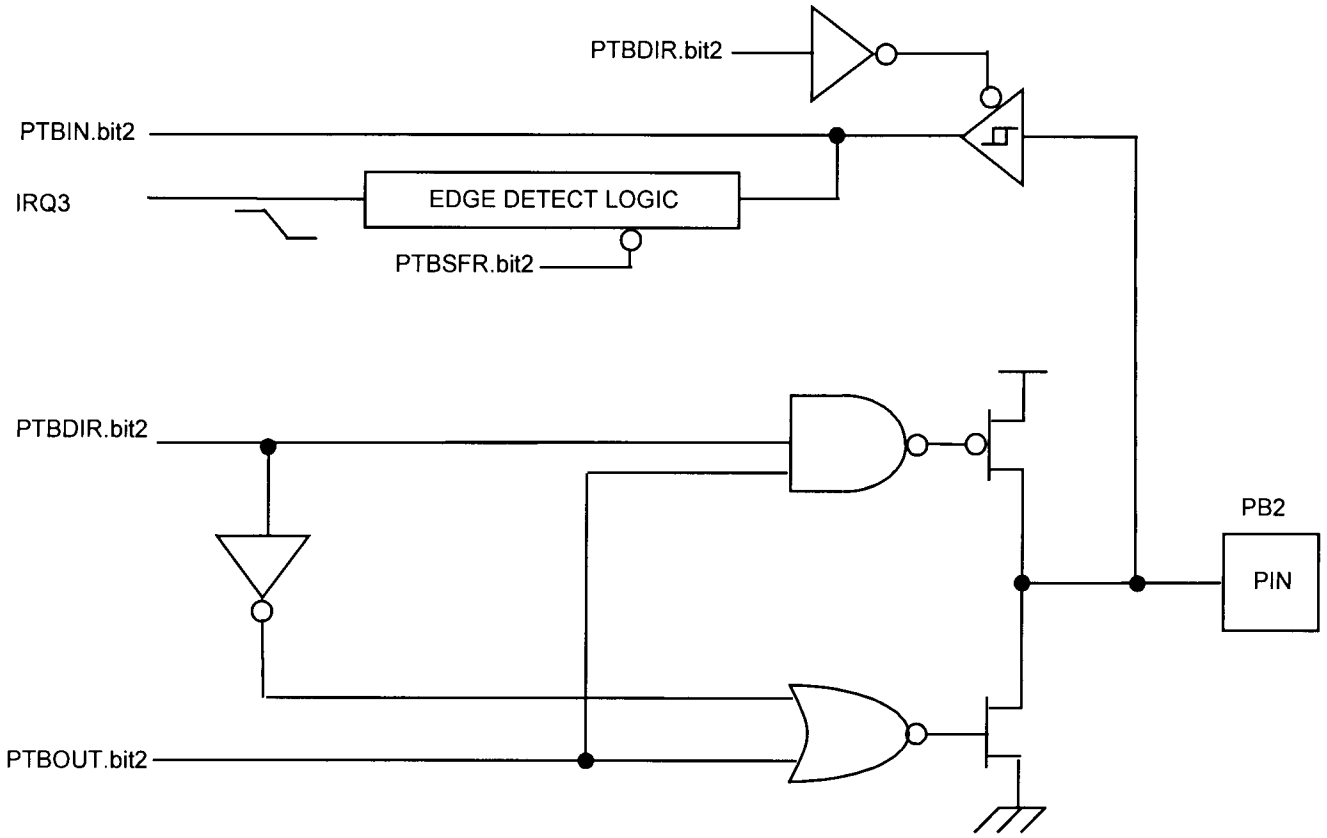


Figure 31. Port B Pin 2 Diagram

PORT B CONTROL REGISTER DEFINITIONS (Continued)

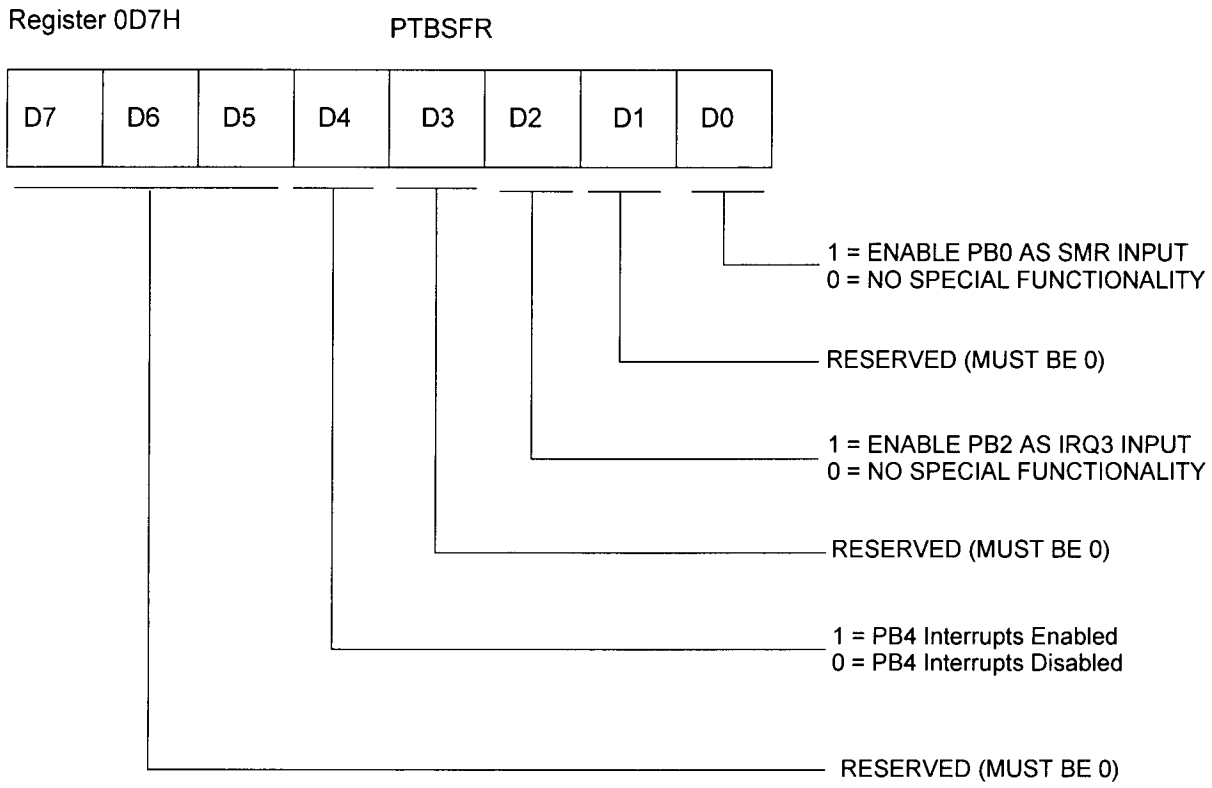
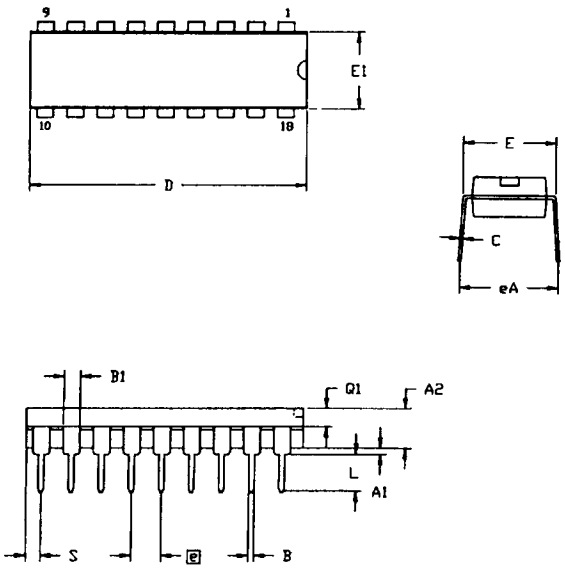


Figure 36. Port B Special Function Register

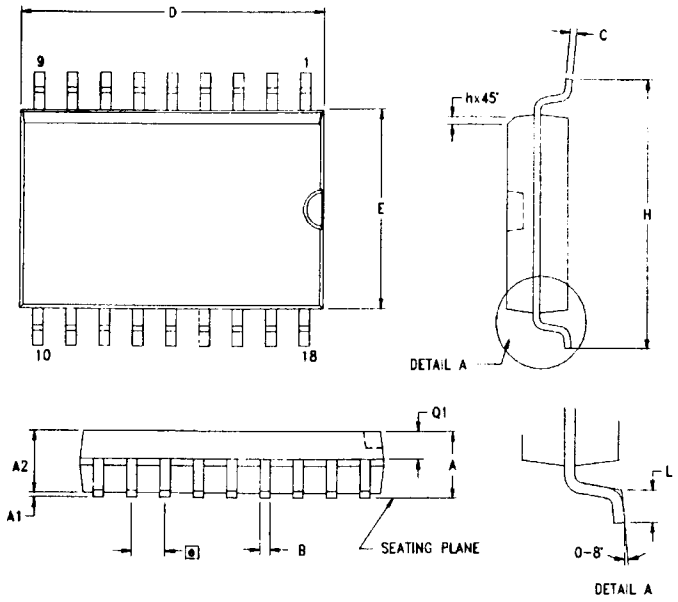
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

Figure 39. 18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
e	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 40. 18-Pin SOIC Package Diagram

Pre-Characterization Product:

The product represented by this data sheet is newly introduced and ZiLOG has not completed the full characterization of the product. The data sheet states what ZiLOG knows about this product at this time, but additional features or nonconformance with some aspects of the data sheet may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

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