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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	WDT
Number of I/O	13
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	32 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8e00010peg

GENERAL DESCRIPTION (Continued)

Note: All signals with an overline, "‾", are active Low. For example, B/$\overline{W}$ (WORD is active Low, only); $\overline{B}$/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

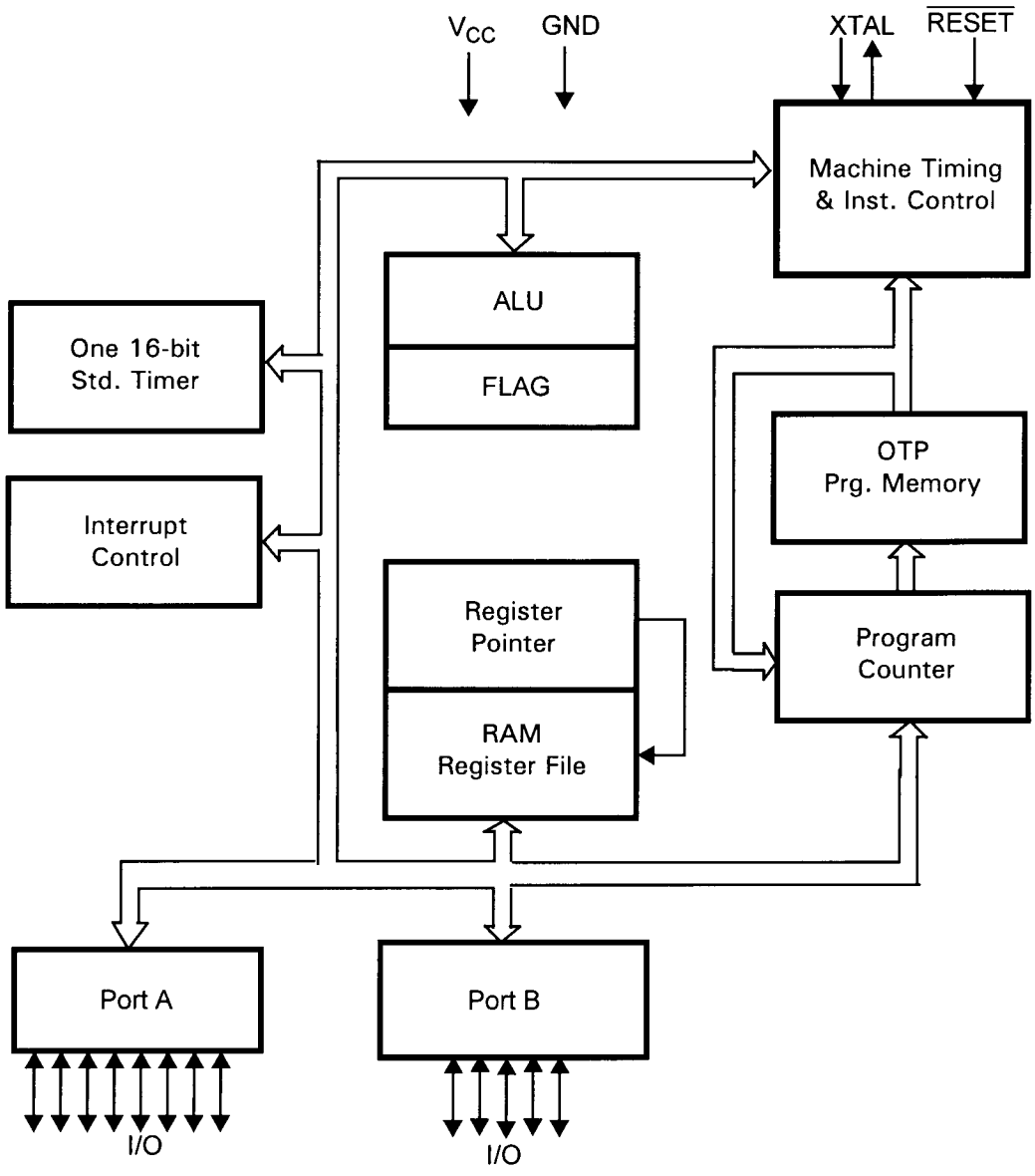


Figure 1. Functional Block Diagram

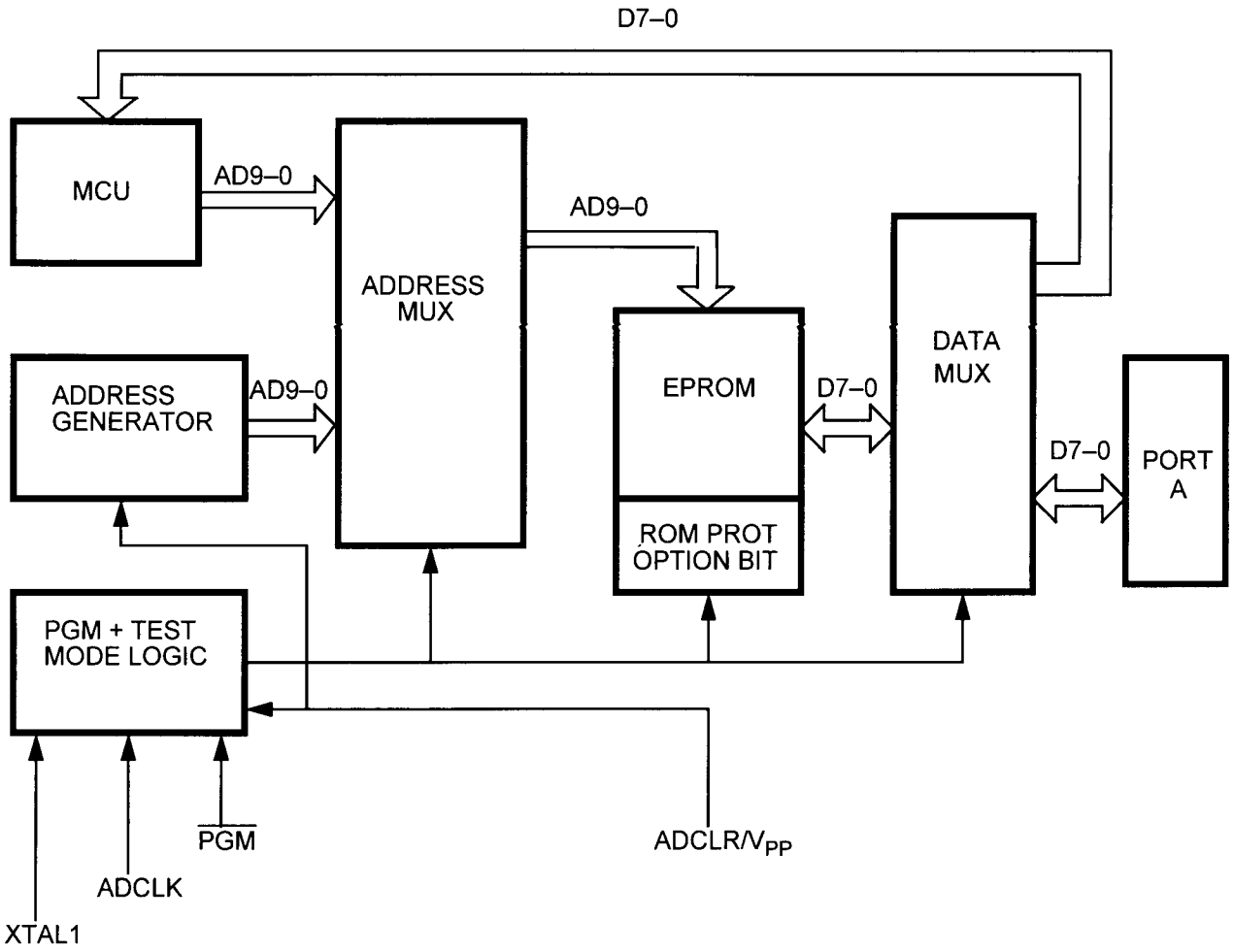


Figure 2. EPROM Programming Mode Block Diagram

PIN DESCRIPTION

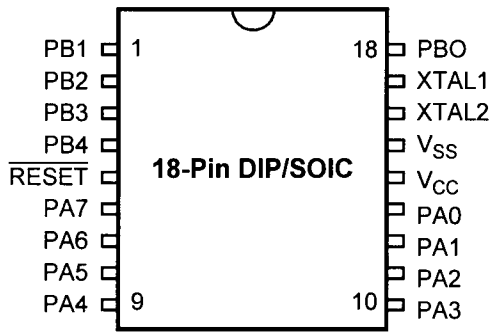


Figure 3. 18-Pin DIP/SOIC Pin Identification

Table 1. 18-Pin DIP/SOIC Pin Assignments

Standard Mode			
Pin #	**Symbol**	**Function**	**Direction**
1–4	PB1–PB4	Port B, Pins 1,2,3,4	In/Output
5	$\overline{\text{RESET}}$	Reset	Input
6–9	PA7–PA4	Port A, Pins 7,6,5,4	In/Output
10–13	PA3–PA0	Port A, Pins 3,2,1,0	In/Output
14	V_{CC}	Power Supply	
15	V_{SS}	Ground	
16	XTAL2	Crystal Oscillator Clock	Output
17	XTAL1	Crystal Oscillator Clock	Input
18	PB0	Port B, Pin 0	In/Output

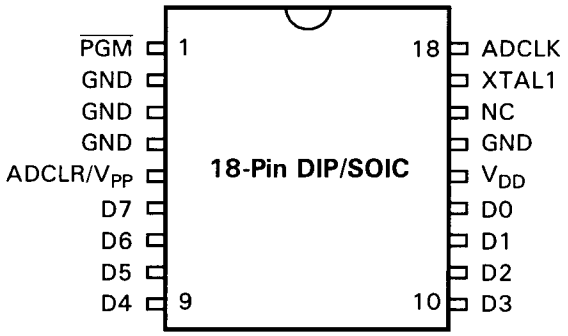


Figure 4. 18-Pin DIP/SOIC Pin Identification; EPROM Programming Mode

Table 2. 18-Pin DIP/SOIC Pin Assignments; EPROM Programmable Mode

EPROM Programming Mode			
Pin #	**Symbol**	**Function**	**Direction**
1	$\overline{PGM}$	Program Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clock/Program Voltage	Input
6–9	D7–D4	Data 7,6,5,4	In/Output
10–13	D3–D0	Data 3,2,1,0	In/Output
14	V_{DD}	Power Supply	
15	GND	Ground	
16	NC	No Connection	
17	XTAL1	1 MHz Clock	Input
18	ADCLK	Address Clock	Input

DC ELECTRICAL CHARACTERISTICS

			T_A = 0°C to +70°C					
Sym	Parameter	V_{CC}[1]	Min	Max	Typical @ 25°C[2]	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.5V	$0.7V_{CC}$	V_{CC}+0.3	1.3	V	Driven by External Clock Generator	
		5.5V	$0.7V_{CC}$	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.5V	V_{SS}–0.3	$0.2V_{CC}$	0.7	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.5V	$0.7V_{CC}$	V_{CC}+0.3	1.3	V		
		5.5V	$0.7V_{CC}$	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	3.5V	V_{SS}–0.3	$0.2V_{CC}$	0.7	V		
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.5	V		
V_{OH}	Output High Voltage	3.5V	V_{CC}–0.4		3.1	V	I_{OH} = –2.0 mA	
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	
V_{OL1}	Output Low Voltage	3.5V		0.6	0.2	V	I_{OL} = +4.0 mA	
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	
V_{OL2}	Output Low Voltage	3.5V		1.2	0.5	V	I_{OL} = +6 mA	
		5.5V		1.2	0.5	V	I_{OL} = +12 mA	
V_{RH}	Reset Input High Voltage	3.5V	$0.5V_{CC}$	V_{CC}	1.1	V		
		5.5V	$0.5V_{CC}$	V_{CC}	2.2	V		
V_{RL}	Reset Input Low Voltage	3.5V	V_{SS}–0.3	$0.2V_{CC}$	0.9	V		
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.4	V		
I_{IL}	Input Leakage	3.5V	–1.0	2.0	0.064	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	0.064	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.5V	–1.0	2.0	0.114	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	0.114	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.5V	–10	–60	–30	µA		
		5.5V	–20	–180	–100	µA		
I_{CC}	Supply Current	3.5V		2.5	2.0	mA	@ 10 MHz	3,4
		5.5V		6.0	4.0	mA	@ 10 MHz	3,4
I_{CC1}	Standby Current	3.5V		2.0	1.0	mA	Halt Mode V_{IN} = 0V V_{CC}@10 MHz	3,4
		5.5V		6.0	4.0	mA	Halt Mode V_{IN} = 0V V_{CC}@10 MHz	3,4

Sym	Parameter	V_{CC}[1]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C[2]	Units	Conditions	Notes
I_{CC2}	Standby Current	3.5V		500	150	nA	Stop Mode V_{IN} = 0V, V_{CC}	5
		5.5V		500	250	nA	Stop Mode V_{IN} = 0V, V_{CC}	5

Notes:

1. The V_{CC} voltage specification of 3.5 V guarantees 3.5 V and the V_{CC} voltage specification of 5.5 V guarantees 5.0 V ±0.5 V.
2. Typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V.
3. All outputs unloaded, I/O pins floating, and all inputs are at V_{CC} or V_{SS} level.
4. CL1 = CL2 = 22 pF.
5. Same as note 3 except inputs at V_{CC}.

AC ELECTRICAL CHARACTERISTICS

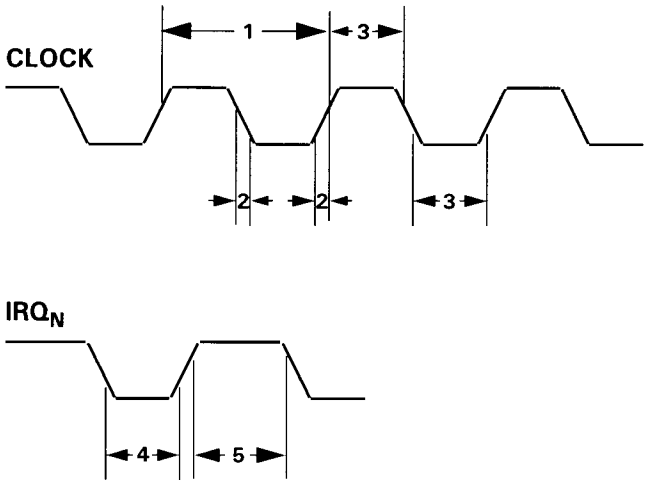


Figure 8. AC Electrical Timing Diagram

Table 5. Additional Timings

				T_A = –40°C to +105°C @ 10 MHz			
No	**Symbol**	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	3.5V	100	DC	ns	2
			5.5V	100	DC	ns	2
2	TrC,TfC	Clock Input Rise and Fall Times	3.5V		15	ns	2
			5.5V		15	ns	2
3	TwC	Input Clock Width	3.5V	50		ns	2
			5.5V	50		ns	2
4	TwIL	Int. Request Input Low Time	3.5V	70		ns	2
			5.5V	70		ns	2
5	TwIH	Int. Request Input High Time	3.5V	5TpC			2
			5.5V	5TpC			2
6	Twsm	STOP Mode Recovery Width Spec.	3.5V	12		ns	
			5.5V	12		ns	
7	Tost	Oscillator Start-Up Time	3.5V		5TpC		
			5.5V		5TpC		

Notes:
1. The V_{DD} voltage specification of 3.5V guarantees 3.5V. The V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

Z8PLUS CORE

The Z8E000 is based on the ZiLOG Z8Plus Core Architecture. This core is capable of addressing up to 64KBytes of program memory and 4KBytes of RAM. Register RAM is accessed as either 8- or 16-bit registers, using a combination of 4-, 8-, and 12-bit addressing modes. The architecture supports up to 15 vectored interrupts from external and internal sources. The processor decodes 44 CISC instructions, using six addressing modes. See the Z8Plus User's Manual for more information.

RESET

This section describes the Z8E000 reset conditions, reset timing, and register initialization procedures. Reset is generated by the Reset Pin, Watch-Dog Timer (WDT), and Stop-Mode Recovery (SMR).

A system reset overrides all other operating conditions and puts the Z8E000 into a known state. To initialize the chip's internal logic, the $\overline{\text{RESET}}$ input must be held Low for at least 30 XTAL clock cycles. The control registers and ports are reset to their default conditions after a reset from the $\overline{\text{RESET}}$ pin. The control registers and ports are not reset to their default conditions after wakeup from Stop Mode or WDT timeout.

During $\overline{\text{RESET}}$, the program counter is loaded with 0020H. I/O ports and control registers are configured to their default reset state. Resetting the Z8E000 does not affect the contents of the general-purpose registers.

RESET PIN OPERATION

The Z8E000 hardware $\overline{\text{RESET}}$ pin initializes the control and peripheral registers, as indicated in Table 6. Specific reset values are indicated by 1 or 0, while bits whose states are unchanged are indicated by the letter U.

$\overline{\text{RESET}}$ must first be held Low until the oscillator stabilizes. From than point, the pin then must be held for an additional 30 XTAL clock cycles to be sure that the internal reset is complete. The $\overline{\text{RESET}}$ pin has a Schmitt-Trigger input with a trip point. There is no High side protection diode. The user should place an external diode from $\overline{\text{RESET}}$ to V_{CC}. The internal pull-up resistor on the $\overline{\text{RESET}}$ pin is approximately 500 KΩ, typical.

Program execution starts 10 XTAL clock cycles after $\overline{\text{RESET}}$ has returned High. The initial instruction fetch is from location 0020H. Figure 9 indicates reset timing.

After a reset, the first routine executed must be one that initializes the TCTLHI control register to the required system configuration. This routine is then followed by initialization of the remaining control registers.

Table 6. Control and Peripheral Register Reset Values

Register		Bits								
(HEX)	Register Name	7	6	5	4	3	2	1	0	Comments
FF	Stack Pointer	0	0	U	U	U	U	U	U	Stack pointer is not affected by $\overline{\text{RESET}}$
FE	Reserved									
FD	Register Pointer	U	U	U	U	0	0	0	0	Register pointer is not affected by $\overline{\text{RESET}}$
FC	Flags	U	U	U	U	U	U	*	*	Only WDT & SMR flags are affected by $\overline{\text{RESET}}$
FB	Interrupt Mask	0	0	0	0	0	0	0	0	All interrupts masked by $\overline{\text{RESET}}$
FA	Interrupt Request	0	0	0	0	0	0	0	0	All interrupt requests cleared by $\overline{\text{RESET}}$
F9–F0	Reserved									
EF–E0	Virtual Copy									Virtual Copy of the Current Working Register Set
DF–D8	Reserved									
D7	PortB Spec. Func.	0	0	0	0	0	0	0	0	Deactivates all port special functions after $\overline{\text{RESET}}$
D6	PortB Directional Control	0	0	0	0	0	0	0	0	Defines all bits as inputs in PortB after $\overline{\text{RESET}}$
D5	PortB Output	U	U	U	U	U	U	U	U	Output register not affected by $\overline{\text{RESET}}$

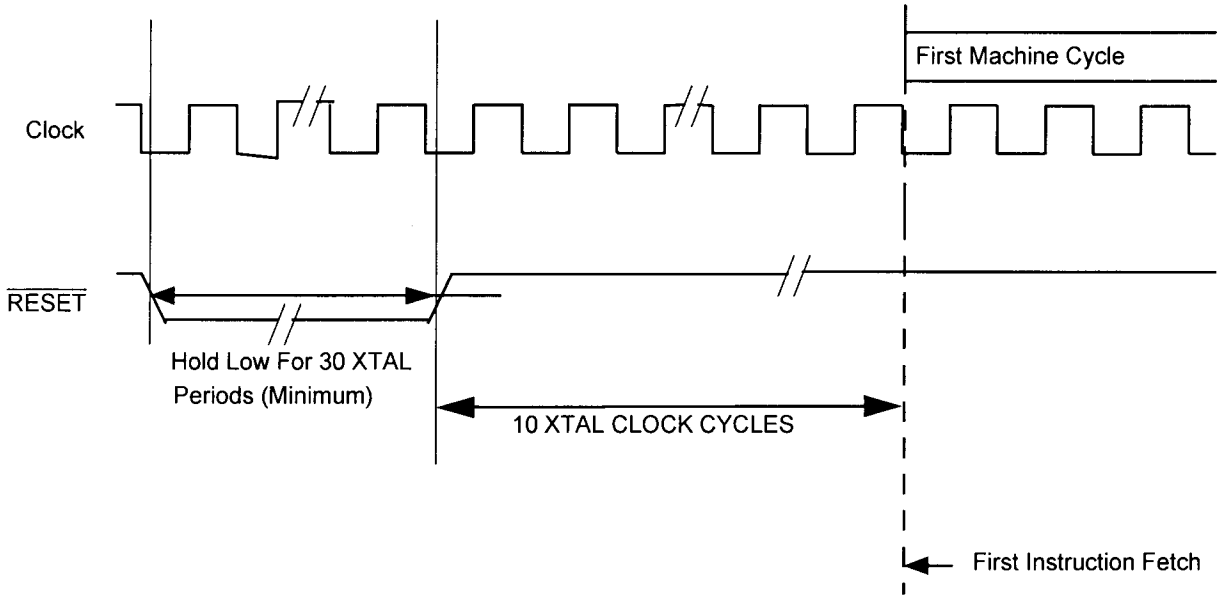


Figure 9. Reset Timing

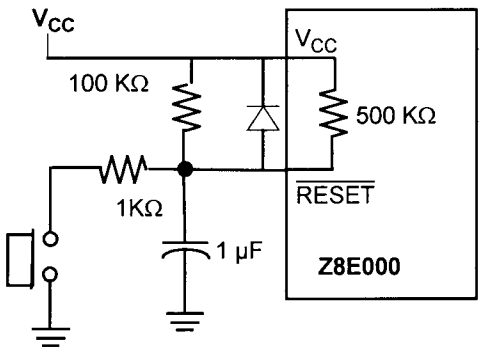


Figure 10. Example of External Power-On Reset Circuit

Z8E000 WATCH-DOG TIMER (WDT)

The Watch-Dog Timer is a retriggerable one-shot 16-bit timer that resets the Z8E000 if it reaches its terminal count. The WDT is driven by the XTAL2 clock pin. To provide the longer timeout periods required in applications, the WDT is only updated every 64th clock cycle. When operating in the RUN or HALT Modes, a WDT timeout reset is functionally equivalent to an interrupt vectoring the PC to 0020H and setting the WDT flag to a one state. Coming out of $\overline{\text{RESET}}$, the WDT will be fully enabled with its timeout value set at the maximum value, unless otherwise programmed during the first instruction. Subsequent executions of the WDT instruction reinitialize the watch-dog timer registers (C2H and C3H) to their initial values as defined by bits D6, D5, and D4 of the TCTLHI register (Figure 12). The WDT cannot be disabled except on the first cycle after $\overline{\text{RESET}}$, and if the device enters Stop mode.

The WDT instruction should be executed often enough to provide some margin before allowing the WDT registers to get near 0. Because the WDT timeout periods are relatively long, a WDT reset *will* occur in the unlikely event that the WDT times out on exactly the same cycle that the WDT instruction is executed.

The WDT and SMR flags are the only flags that are affected by the external $\overline{\text{RESET}}$ pin. $\overline{\text{RESET}}$ clears both the WDT and SMR flags. A WDT timeout sets the WDT flag. The STOP instruction sets the SMR flag. This behavior enables software to determine whether a pin $\overline{\text{RESET}}$ occurred, whether a WDT timeout occurred, or whether a return from STOP Mode occurred. Reading the WDT flag does not reset it to zero. The user must clear the WDT flag via software. Failure to clear the WDT flag can result in undefined behavior.

Z8E000 WATCH-DOG TIMER (WDT) (Continued)

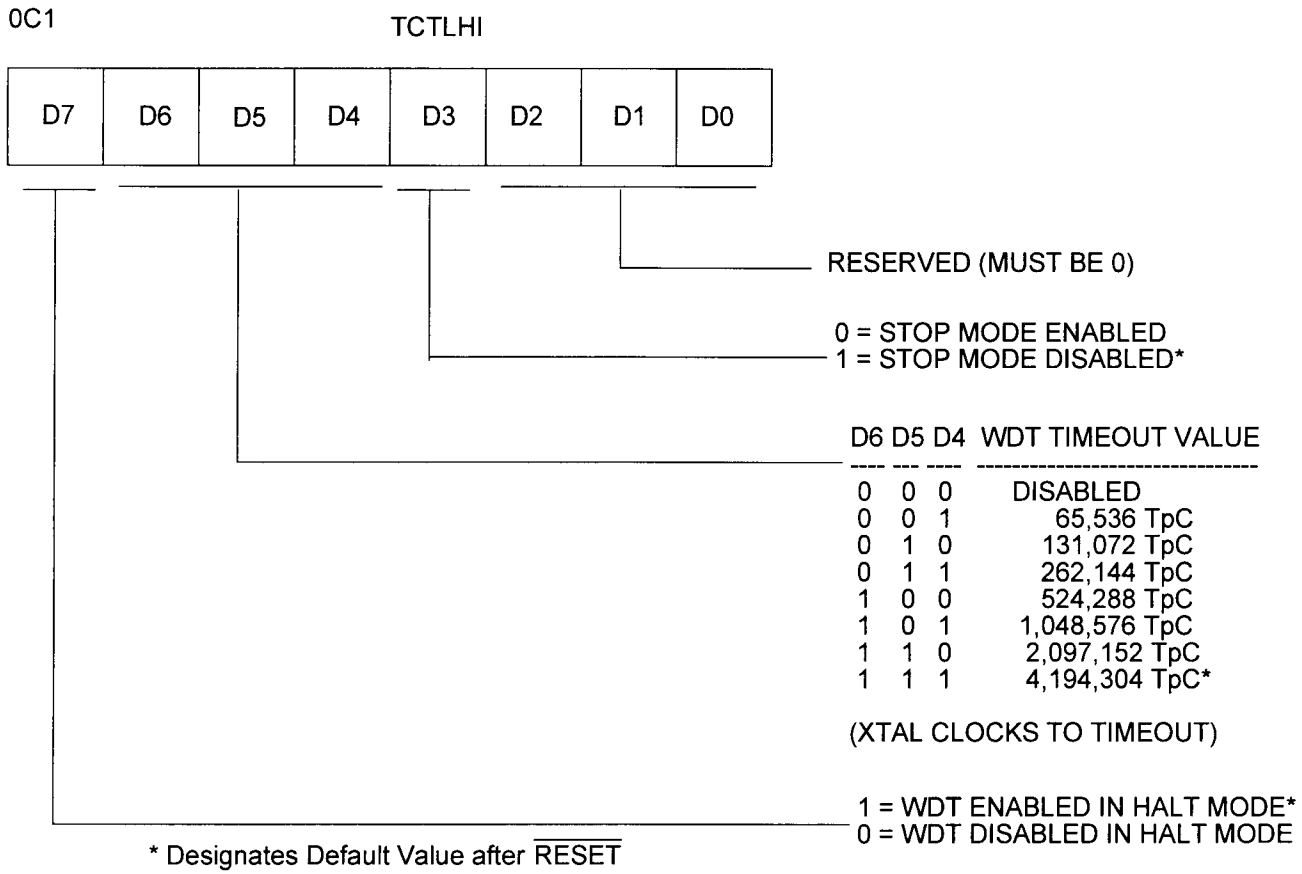


Figure 12. Z8E000 TCTLHI Register for Control of WDT

Note: The WDT can only be disabled via software if the first instruction out of RESET performs this function. Logic within the Z8E000 will detect that it is in the process of executing the first instruction after the part leaves RESET. During the execution of this instruction, the upper five bits of the TCTLHI register can be written. After this first instruction, hardware will not allow the upper five bits of this register to be written.

The TCTLHI bits for control of the WDT are described below:

WDT Time Select (D6, D5, D4). Bits 6, 5, and 4 determine the time-out period. Table 7 indicates the range of timeout values that can be obtained. The default values of D6, D5, and D4 are all 1, thus setting the WDT to its maximum timeout period when coming out of RESET.

Table 7. Time-Out Period of the WDT

D6	D5	D4	Crystal Clocks to Timeout	Time-Out Using a10 MHz Crystal
0	0	0	Disabled	Disabled
0	0	1	65,536 TpC	6.55 ms
0	1	0	131,072 TpC	13.11 ms
0	1	1	262,144 TpC	26.21 ms
1	0	0	524,288 TpC	52.43 ms
1	0	1	1,048,576 TpC	104.86 ms
1	1	0	2,097,152 TpC	209.72 ms
1	1	1	4,194,304 TpC	419.43 ms

Notes:
TpC = XTAL clock cycle.
The default on reset is D6 = D5 = D4 = 1.

STOP MODE OPERATION

The STOP Mode provides the lowest possible device stand-by current. This instruction turns off the on-chip oscillator and internal system clock.

To enter the STOP Mode, the Z8E000 only requires a STOP instruction. It is NOT necessary to execute a NOP instruction immediately before the STOP instruction.

```
6F    STOP    ;enter STOP Mode
```

The STOP Mode is exited by any one of the following resets: $\overline{\text{RESET}}$ pin or a STOP-Mode Recovery source. Upon reset generation, the processor will always restart the application program at address 0020H, thereby setting the STOP Mode Flag. Reading the STOP-Mode flag does not clear it. The user must clear the STOP-Mode flag with software.

Note: Failure to clear the STOP-Mode flag can result in undefined behavior.

The Z8E000 provides a dedicated STOP Mode Recovery (SMR) circuit. In this case, a low level applied to input pin PB0 will trigger a SMR. To use this mode, pin PB0 (I/O Port B, bit 0) must be configured as an input before the STOP Mode is entered. The low level on PB0 must be held for a minimum pulse width T_{WSM}, in addition to any oscillator startup time. Program execution starts at address 0020H after PBO is raised back to a high level.

Notes: Use of the PB0 input for the STOP mode recovery does not initialize the control registers.

The STOP Mode current (I_{CC2}) will be minimized when:

- V_{CC} is at the low end of the device's operating range.
- Output current sourcing is minimized.
- All inputs (digital and analog) are at the Low or High rail voltages.

CLOCK

The Z8E000 MCU derives its timing from on-board clock circuitry connected to pins XTAL1 and XTAL2. The clock circuitry consists of an oscillator, a glitch filter, a divide-by-two shaping circuit, a divide-by-four shaping circuit, and a divide-by-eight shaping circuit. Figure 13 illustrates the clock circuitry. The oscillator's input is XTAL1 and its output is XTAL2. The clock can be driven by a crystal, a ceramic resonator, LC clock, or an external clock source.

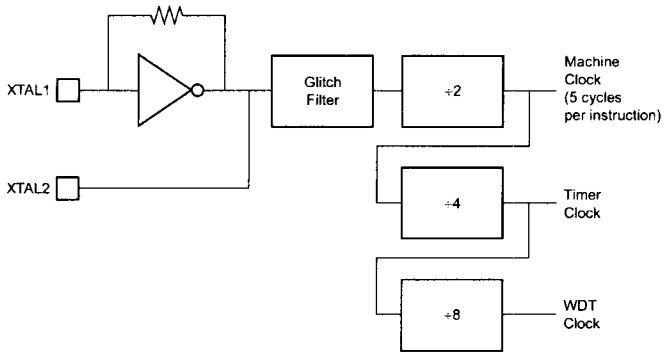


Figure 13. Z8E000 Clock Circuit

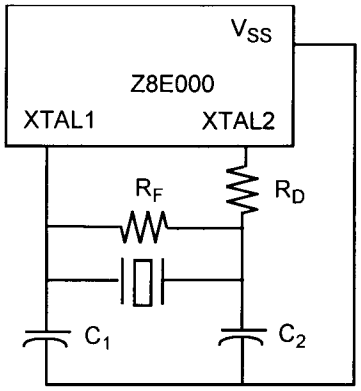


Figure 16. Crystal/Ceramic Resonator Oscillator

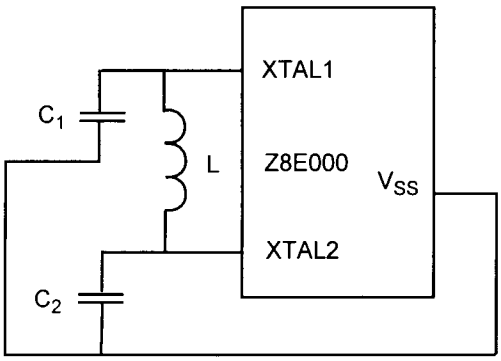


Figure 17. LC Clock

In most cases, the R_D is zero ohms (0Ω), and R_F is infinite. The set value is determined and specified by the crystal/ceramic resonator manufacturer. R_D can be increased to decrease the amount of drive from the oscillator output to the crystal. R_D can also be used as an adjustment to avoid clipping of the oscillator signal to reduce noise. R_F can be used to improve the start-up of the crystal/ceramic resonator. The Z8E000 oscillator already has an internal shunt resistor in parallel to the crystal/ceramic resonator.

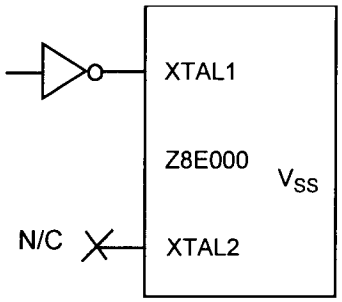
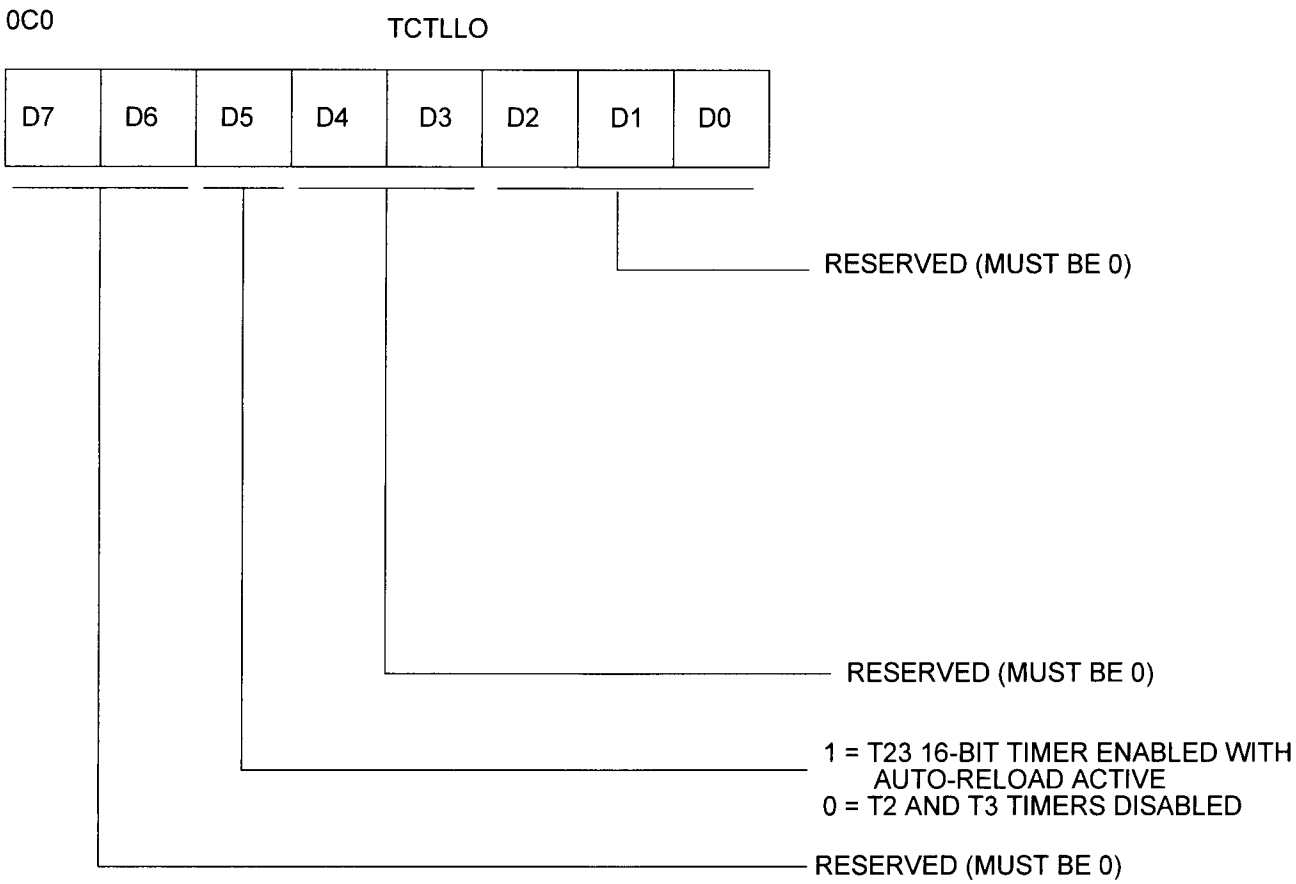


Figure 18. External Clock

Figure 16, Figure 17, and Figure 18 recommend that the load capacitor ground trace connect directly to the V_{SS} (GND) pin of the Z8E000, thereby ensuring that no system noise is injected into the Z8E000 clock. This trace should not be shared with any other components except at the V_{SS} pin of the Z8E000.

Note: A parallel resonant crystal or resonator data sheet will specify a load capacitor value that is the series combination of C_1 and C_2, including all parasitics (PCB and holder).



Note: Timer T23 is a standard 16-bit timer formed by cascading 8-bit timers t3(msb) and t2(lsb).

Figure 20. TCTLLO Register

Each 8-bit timer is equipped with a pair of readable and writable registers, which are both readable and writable. One of the registers is defined to contain the auto-initialization value for the timer, while the second register contains the current value for the timer. When a timer is enabled, the timer will decrement whatever value is currently held in its count register. From that point, the timer continues decrementing until it reaches 0, at which time an interrupt will be generated and the contents of the auto-initialization register are optionally copied into the count value register. If auto-initialization is not enabled, the timer will stop counting upon reaching 0, and control logic will clear the appropriate control register bit to disable the timer. This operation is referred to as a "single-shot". If auto-initialization is enabled, the timer will continue counting from the initialization value. Software should not attempt to use registers that are defined as having timer functionality for any other purpose.

Software is allowed to write to any register at any time, but care should be taken if timer registers are updated while the timer is enabled. If software updates the count value while the timer is in operation, the timer will continue counting based upon the software-updated value. Strange behavior can result if the software update occurred at exactly the point that the timer was reaching 0 to trigger an interrupt and/or reload.

Similarly, if software updates the initialization value register while the timer is active, the next time that the timer reaches 0, it will be initialized using the updated value. Again, strange behavior could result if the initialization value register is being written while the timer is in the process of being initialized. Whether initialization is done with the new or old value is a function of the exact timing of the write operation. In all cases, the Z8E000 will prioritize the software write above that of a decrementer writeback. Howev-

TIMERS (Continued)

er, when hardware clears a control register bit for a timer that is configured for single-shot operation, the clearing of the control bit will override a software write. Reading either register can be done at any time, and will have no effect on the functionality of the timer.

When defined to operate as a single 16-bit entity, the entire 16-bit value must reach 0 before an interrupt is generated. In this case, a single interrupt will be generated, and the interrupt will correspond to the even 8-bit timer. For example, timers T2 and T3 are cascaded to form a single 16-bit timer, so the interrupt for the combined timer will be defined to be that of timer T2 rather than T3 (Figure 20). When a timer pair is specified to act as a single 16-bit timer, the even timer registers in the pair (timer T2) will be defined to hold the timer's least significant byte. Conversely, the odd timer in the pair (timer T3) will hold the timer's most significant byte.

In parallel with the posting of the interrupt request, the interrupting timer's count value will be initialized by copying the contents of the auto-initialization value register to the count value register.

Note: Any time that a timer pair is defined to act as a single 16-bit timer, the auto-reload function will be performed automatically. All 16-bit timers will continue counting while their interrupt requests are active, and will operate in a free-running manner.

If interrupts are disabled for a long period of time, it is possible for the timer to decrement to 0 again before its initial interrupt has been responded to. This condition is termed a degenerate case, and hardware is not required to detect it.

When the timer control register is written, all timers that are enabled by the write will begin counting using the value that is held in their count register. In this case, an auto-initialization is not performed. All timers can receive an internal clock source only. Each timer that is enabled will be updated every 8th XTAL clock cycle.

RESET CONDITIONS

After a hardware $\overline{\text{RESET}}$, the timers are disabled. See Table 5 for timer control, value, and auto-initialization register status after $\overline{\text{RESET}}$.

I/O PORTS

The Z8E000 has 13 lines dedicated to input and output. These lines are grouped into two ports known as Port A and Port B. Port A is an 8-bit port that is bit-programmable as either inputs or outputs. Port B can be programmed to provide standard input/output or the following special functions: SMR input and external interrupt inputs.

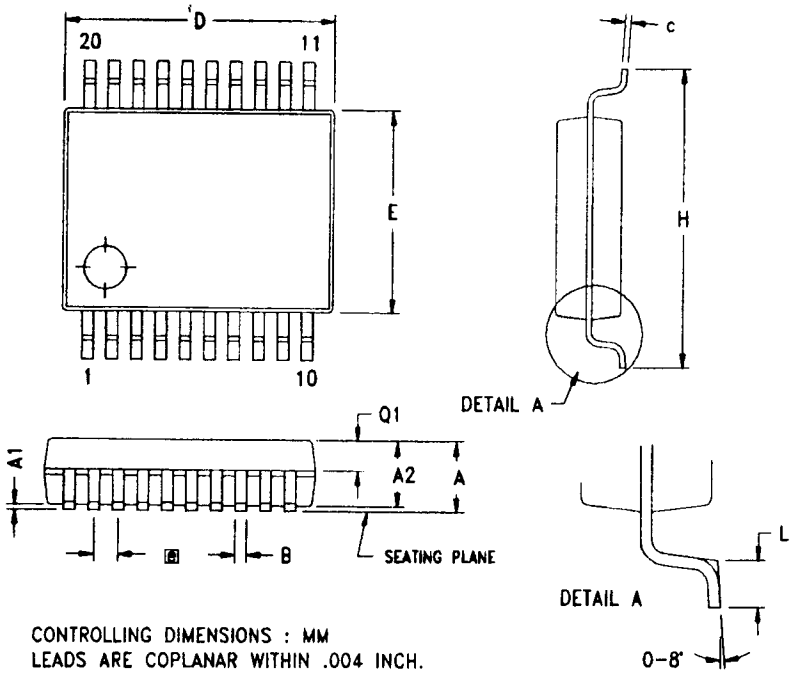
All ports have push-pull CMOS outputs. In addition, the outputs of Port A, on a bit-wise basis, can be configured for open-drain operation. As such, the register values for "/" at a given bit position only affect the bit in question.

Each port is defined by a set of four control registers. See Figure 21.

Directional Control and Special Function Registers

Each port on the Z8E000 has an associated and dedicated for that bit position will contain the current synchronized input value.

REGISTER	ADDRESS	IDENTIFIER
Port B SPECIAL FUNCTION	0D7H	PTBSFR
Port B DIRECTIONAL CONTROL	0D6H	PTBDIR
Port B OUTPUT VALUE	0D5H	PTBOUT
Port B INPUT VALUE	0D4H	PTBIN
Port A SPECIAL FUNCTION	0D3H	PTASFR
Port A DIRECTIONAL CONTROL	0D2H	PTADIR
Port A OUTPUT VALUE	0D1H	PTAOUT



SYMBOL	MILLIMETER			INCH		

Z8E000
Z8PLUS One-Time Programmable Microcontroller ZiLOG

ORDERING INFORMATION

Standard Temperature		
18-Pin DIP	**18-Pin SOIC**	**20-Pin SSOP**
Z8E00010PSC	Z8E00010SSC	Z8E00010HSC

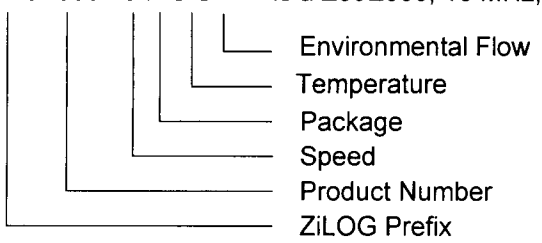
Extended Temperature		
18-Pin DIP	**18-Pin SOIC**	**20-Pin SSOP**
Z8E00010PEC	Z8E00010SEC	Z8E00010HEC

For fast results, contact your local ZiLOG sales office for assistance in ordering the part(s) required.

Codes	
Preferred Package	P = Plastic DIP
Longer Lead Time	S = SOIC
	H = SSOP
Preferred Temperature	S = 0°C to +70°C
	E = –40°C to +105°C
Speed	10 = 10 MHz
Environmental	C = Plastic Standard

Example:

Z 8E000 10 P S C is a Z86E000, 10 MHz, DIP, 0° to +70°C, Plastic Standard Flow



PORT A

Port A is a general-purpose port (Figure 23). Each of its lines can be independently programmed as input or output via the

Register 0D2H
PTADIR Register

PORT A REGISTER DEFINITIONS

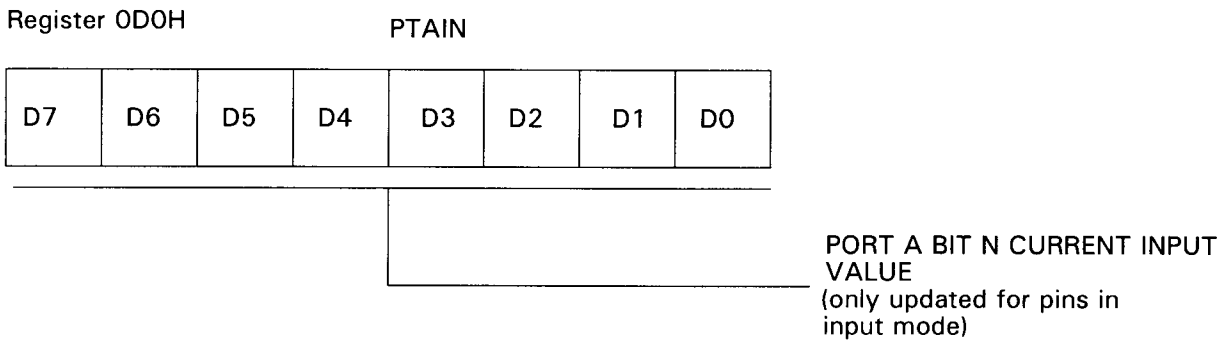


Figure 24. Port A Input Value Register

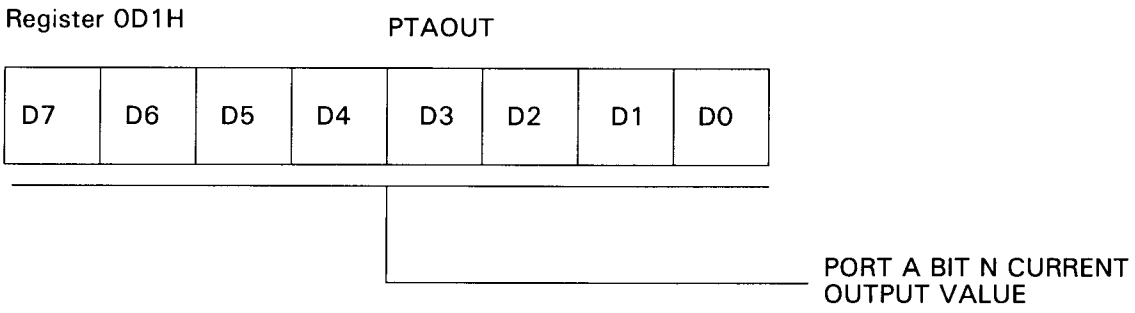


Figure 25. Port A Output Value Register

PORT B—PINS 3 AND 4 CONFIGURATION

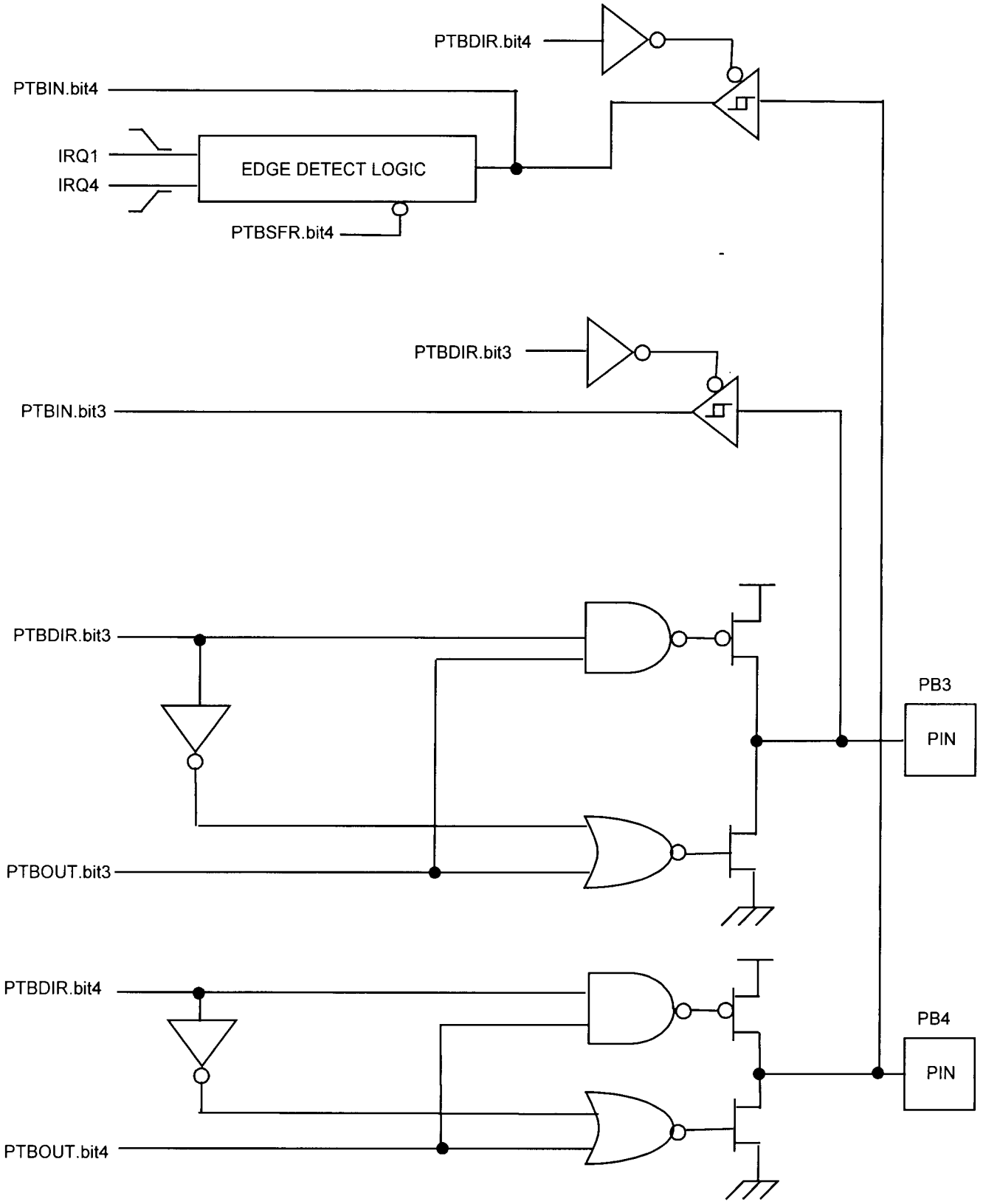


Figure 32. Port B Pins 3 and 4 Diagram