Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	WDT
Number of I/O	13
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	32 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8e00010psg

GENERAL DESCRIPTION (Continued)

Note: All signals with an overline, "‾", are active Low. For example, B/$\overline{W}$ (WORD is active Low, only); $\overline{B}$/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

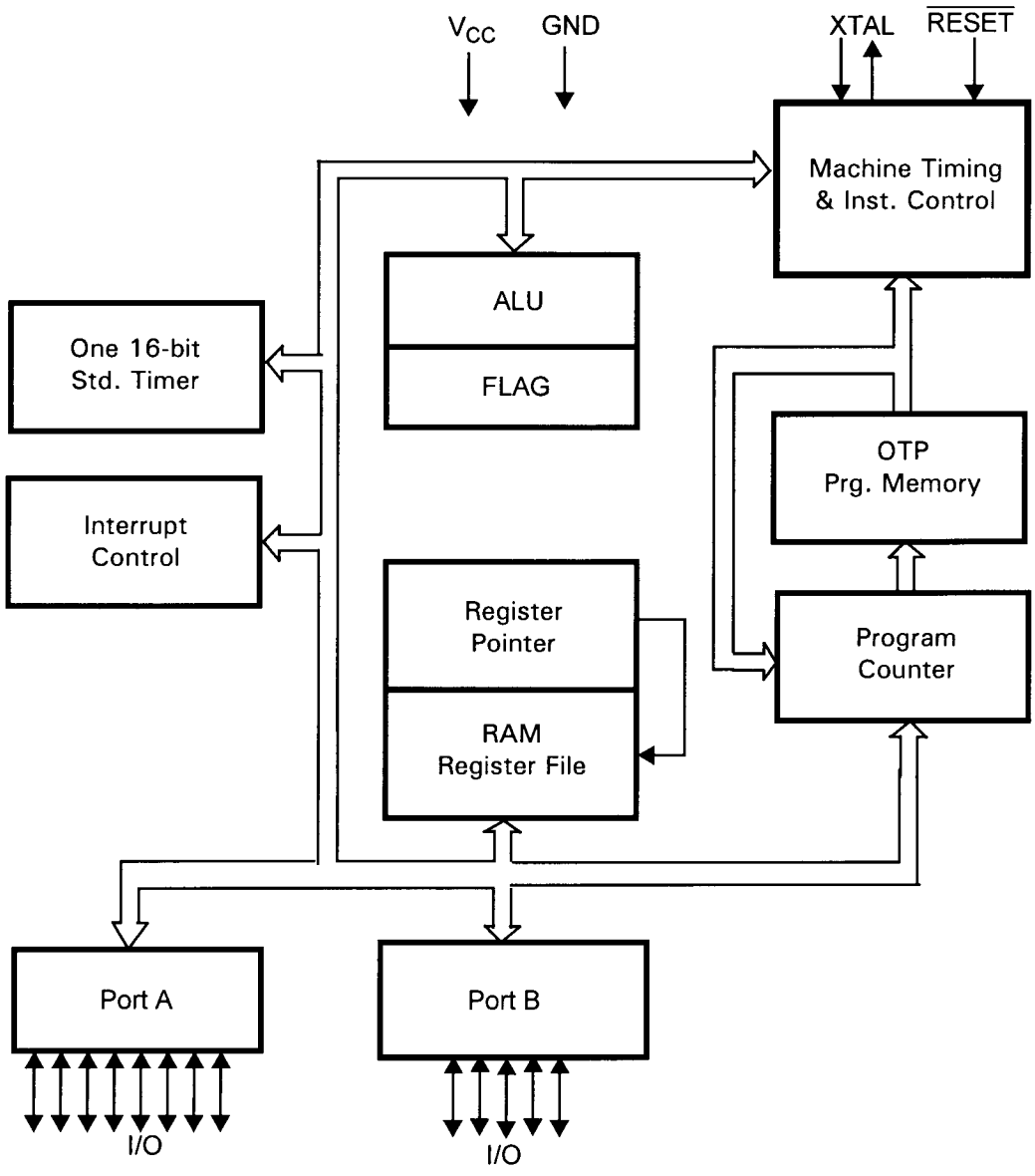


Figure 1. Functional Block Diagram

PIN DESCRIPTION (Continued)

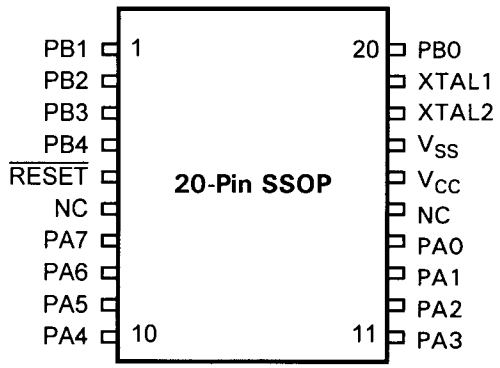


Figure 5. 20-Pin SSOP Pin Identification

Table 3. 20-Pin SSOP Pin Assignments

Standard Mode

Pin #	Symbol	Function	Direction
1–4	PB1–PB4	Port B, Pins 1,2,3,4	In/Output
5	$\overline{\text{RESET}}$	Reset	Input
6	NC	No Connection	
7–10	PA7–PA4	Port A, Pins 7,6,5,4	In/Output
11–14	PA3–PA0	Port A, Pins 3,2,1,0	In/Output
15	NC	No Connection	
16	V_{CC}	Power Supply	
17	V_{SS}	Ground	
18	XTAL2	Crystal Oscillator Clock	Output
19	XTAL1	Crystal Oscillator Clock	Input
20	PB0	Port B, Pin 0	In/Output

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 7).

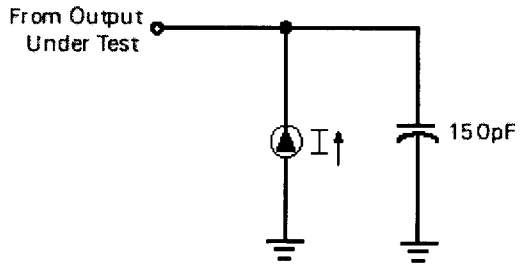


Figure 7. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

			T_A = 0°C to +70°C					
Sym	Parameter	V_{CC}[1]	Min	Max	Typical @ 25°C[2]	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.5V	$0.7V_{CC}$	V_{CC}+0.3	1.3	V	Driven by External Clock Generator	
		5.5V	$0.7V_{CC}$	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.5V	V_{SS}–0.3	$0.2V_{CC}$	0.7	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.5V	$0.7V_{CC}$	V_{CC}+0.3	1.3	V		
		5.5V	$0.7V_{CC}$	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	3.5V	V_{SS}–0.3	$0.2V_{CC}$	0.7	V		
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.5	V		
V_{OH}	Output High Voltage	3.5V	V_{CC}–0.4		3.1	V	I_{OH} = –2.0 mA	
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	
V_{OL1}	Output Low Voltage	3.5V		0.6	0.2	V	I_{OL} = +4.0 mA	
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	
V_{OL2}	Output Low Voltage	3.5V		1.2	0.5	V	I_{OL} = +6 mA	
		5.5V		1.2	0.5	V	I_{OL} = +12 mA	
V_{RH}	Reset Input High Voltage	3.5V	$0.5V_{CC}$	V_{CC}	1.1	V		
		5.5V	$0.5V_{CC}$	V_{CC}	2.2	V		
V_{RL}	Reset Input Low Voltage	3.5V	V_{SS}–0.3	$0.2V_{CC}$	0.9	V		
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.4	V		
I_{IL}	Input Leakage	3.5V	–1.0	2.0	0.064	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	0.064	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.5V	–1.0	2.0	0.114	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	0.114	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.5V	–10	–60	–30	µA		
		5.5V	–20	–180	–100	µA		
I_{CC}	Supply Current	3.5V		2.5	2.0	mA	@ 10 MHz	3,4
		5.5V		6.0	4.0	mA	@ 10 MHz	3,4
I_{CC1}	Standby Current	3.5V		2.0	1.0	mA	Halt Mode V_{IN} = 0V V_{CC}@10 MHz	3,4
		5.5V		6.0	4.0	mA	Halt Mode V_{IN} = 0V V_{CC}@10 MHz	3,4

Sym	Parameter	V_{CC}[1]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C[2]	Units	Conditions	Notes
I_{CC2}	Standby Current	3.5V		500	150	nA	Stop Mode V_{IN} = 0V, V_{CC}	5
		5.5V		500	250	nA	Stop Mode V_{IN} = 0V, V_{CC}	5

Notes:

1. The V_{CC} voltage specification of 3.5 V guarantees 3.5 V and the V_{CC} voltage specification of 5.5 V guarantees 5.0 V ±0.5 V.
2. Typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V.
3. All outputs unloaded, I/O pins floating, and all inputs are at V_{CC} or V_{SS} level.
4. CL1 = CL2 = 22 pF.
5. Same as note 3 except inputs at V_{CC}.

DC ELECTRICAL CHARACTERISTICS (Continued)

			T_A = –40°C to +105°C					
Sym	Parameter	V_{CC} [1]	Min	Max	Typical @ 25°C [2]	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	4.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL} = +4.0 mA	
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	
V_{OL2}	Output Low Voltage	4.5V		1.2	0.5	V	I_{OL} = +12 mA,	
		5.5V		1.2	0.5	V	I_{OL} = +12 mA,	
V_{RH}	Reset Input High Voltage	4.5V	0.5V_{CC}	V_{CC}	1.1	V		
		5.5V	0.5V_{CC}	V_{CC}	2.2	V		
I_{IL}	Input Leakage	4.5V	–1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V	–1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	4.5V	–18	–180	–112	mA		
		5.5V	–18	–180	–112	mA		
I_{CC}	Supply Current	4.5V		7.0	4.0	mA	@ 10 MHz	3,4
		5.5V		7.0	4.0	mA	@ 10 MHz	3,4
I_{CC1}	Standby Current	4.5V		2.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 10 MHz	3,4
		5.5V		2.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 10 MHz	3,4

AC ELECTRICAL CHARACTERISTICS

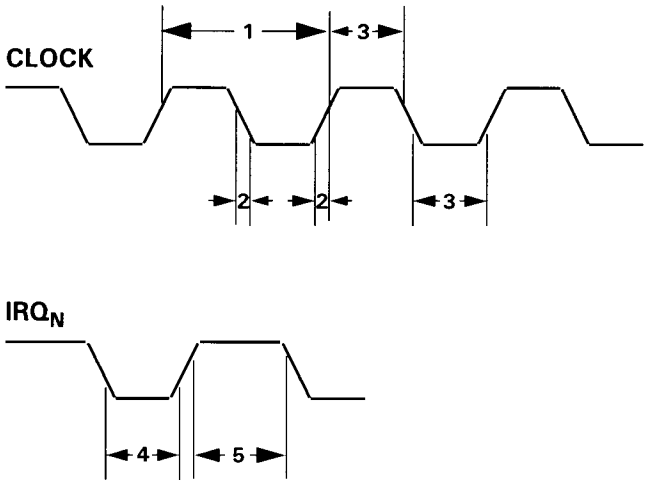


Figure 8. AC Electrical Timing Diagram

Table 5. Additional Timings

				T_A = –40°C to +105°C @ 10 MHz			
No	**Symbol**	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	3.5V	100	DC	ns	2
			5.5V	100	DC	ns	2
2	TrC,TfC	Clock Input Rise and Fall Times	3.5V		15	ns	2
			5.5V		15	ns	2
3	TwC	Input Clock Width	3.5V	50		ns	2
			5.5V	50		ns	2
4	TwIL	Int. Request Input Low Time	3.5V	70		ns	2
			5.5V	70		ns	2
5	TwIH	Int. Request Input High Time	3.5V	5TpC			2
			5.5V	5TpC			2
6	Twsm	STOP Mode Recovery Width Spec.	3.5V	12		ns	
			5.5V	12		ns	
7	Tost	Oscillator Start-Up Time	3.5V		5TpC		
			5.5V		5TpC		

Notes:
1. The V_{DD} voltage specification of 3.5V guarantees 3.5V. The V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

Z8E000 WATCH-DOG TIMER (WDT)

The Watch-Dog Timer is a retriggerable one-shot 16-bit timer that resets the Z8E000 if it reaches its terminal count. The WDT is driven by the XTAL2 clock pin. To provide the longer timeout periods required in applications, the WDT is only updated every 64th clock cycle. When operating in the RUN or HALT Modes, a WDT timeout reset is functionally equivalent to an interrupt vectoring the PC to 0020H and setting the WDT flag to a one state. Coming out of $\overline{\text{RESET}}$, the WDT will be fully enabled with its timeout value set at the maximum value, unless otherwise programmed during the first instruction. Subsequent executions of the WDT instruction reinitialize the watch-dog timer registers (C2H and C3H) to their initial values as defined by bits D6, D5, and D4 of the TCTLHI register (Figure 12). The WDT cannot be disabled except on the first cycle after $\overline{\text{RESET}}$, and if the device enters Stop mode.

The WDT instruction should be executed often enough to provide some margin before allowing the WDT registers to get near 0. Because the WDT timeout periods are relatively long, a WDT reset *will* occur in the unlikely event that the WDT times out on exactly the same cycle that the WDT instruction is executed.

The WDT and SMR flags are the only flags that are affected by the external $\overline{\text{RESET}}$ pin. $\overline{\text{RESET}}$ clears both the WDT and SMR flags. A WDT timeout sets the WDT flag. The STOP instruction sets the SMR flag. This behavior enables software to determine whether a pin $\overline{\text{RESET}}$ occurred, whether a WDT timeout occurred, or whether a return from STOP Mode occurred. Reading the WDT flag does not reset it to zero. The user must clear the WDT flag via software. Failure to clear the WDT flag can result in undefined behavior.

WDT During HALT (D7). This bit determines whether or not the WDT is active during HALT Mode. A "1" indicates active during HALT. A "0" prevents the WDT from resetting the part while halted.Coming out of reset, the WDT will be enabled during HALT Mode.

STOP MODE (D3). Coming out of $\overline{\text{RESET}}$, the Z8E000 will have the STOP Mode disabled. If an application requires use of STOP Mode, bit D3 must be cleared immediately upon leaving $\overline{\text{RESET}}$. If bit D3 is set, the STOP instruction will execute as a NOP. If bit D3 is cleared, the STOP instruction will enter Stop Mode. Whenever the Z8E000 wakes up after having been in STOP Mode, the STOP Mode will be disabled once again.

Bits 2, 1 and 0. These bits are reserved and must be 0.

POWER-DOWN MODES

In addition to the standard RUN mode, the Z8E000 MCU supports two Power-Down modes to minimize device current consumption. The two modes supported are HALT and STOP.

HALT MODE OPERATION

The HALT Mode suspends instruction execution and turns off the internal CPU clock. The on-chip oscillator circuit remains active, so the internal clock continues to run and is applied to the timers and interrupt logic.

To enter the HALT Mode, the Z8E000 only requires a HALT instruction. It is NOT necessary to execute a NOP instruction immediately before the HALT instruction.

```
7F    HALT    ; enter HALT Mode
```

The HALT Mode can be exited by servicing an interrupt (either externally or internally). Upon completion of the interrupt service routine, the user program continues from the instruction after HALT.

The HALT Mode can also be exited via a $\overline{\text{RESET}}$ activation or a Watch-Dog Timer (WDT) timeout. In these cases, program execution will restart at the reset address 0020H.

STOP MODE OPERATION

The STOP Mode provides the lowest possible device stand-by current. This instruction turns off the on-chip oscillator and internal system clock.

To enter the STOP Mode, the Z8E000 only requires a STOP instruction. It is NOT necessary to execute a NOP instruction immediately before the STOP instruction.

```
6F    STOP    ;enter STOP Mode
```

The STOP Mode is exited by any one of the following resets: $\overline{\text{RESET}}$ pin or a STOP-Mode Recovery source. Upon reset generation, the processor will always restart the application program at address 0020H, thereby setting the STOP Mode Flag. Reading the STOP-Mode flag does not clear it. The user must clear the STOP-Mode flag with software.

Note: Failure to clear the STOP-Mode flag can result in undefined behavior.

The Z8E000 provides a dedicated STOP Mode Recovery (SMR) circuit. In this case, a low level applied to input pin PB0 will trigger a SMR. To use this mode, pin PB0 (I/O Port B, bit 0) must be configured as an input before the STOP Mode is entered. The low level on PB0 must be held for a minimum pulse width T_{WSM}, in addition to any oscillator startup time. Program execution starts at address 0020H after PBO is raised back to a high level.

Notes: Use of the PB0 input for the STOP mode recovery does not initialize the control registers.

The STOP Mode current (I_{CC2}) will be minimized when:

- V_{CC} is at the low end of the device's operating range.
- Output current sourcing is minimized.
- All inputs (digital and analog) are at the Low or High rail voltages.

CLOCK

The Z8E000 MCU derives its timing from on-board clock circuitry connected to pins XTAL1 and XTAL2. The clock circuitry consists of an oscillator, a glitch filter, a divide-by-two shaping circuit, a divide-by-four shaping circuit, and a divide-by-eight shaping circuit. Figure 13 illustrates the clock circuitry. The oscillator's input is XTAL1 and its output is XTAL2. The clock can be driven by a crystal, a ceramic resonator, LC clock, or an external clock source.

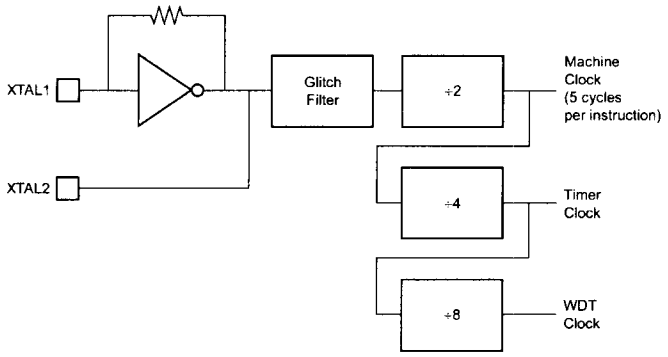


Figure 13. Z8E000 Clock Circuit

OSCILLATOR OPERATION

The Z8E000 MCU uses a Pierce oscillator with an internal feedback circuit (Figure 14). The advantages of this circuit are low cost, large output signal, low power level in the crystal, stability with respect to V_{CC} and temperature, and low impedances (not disturbed by stray effects).

One draw back to the oscillator is the requirement for high gain in the amplifier to compensate for feedback path losses. The oscillator amplifies its own noise at start-up until it settles at the frequency that satisfies the gain/phase requirements ($A \times B = 1$, where $A = V_o/V_i$ is the gain of the amplifier and $B = V_i/V_o$ is the gain of the feedback element). The total phase shift around the loop is forced to zero (360 degrees). VIN must be in phase with itself. The amplifier/inverter thereby provides a 180-degree phase shift, forcing the feedback element to provide the other 180 degrees of phase shift.

R_I is a resistive component placed from output to input of the amplifier. The purpose of this feedback is to bias the amplifier in its linear region and to provide the start-up transition.

Capacitor C_2, combined with the amplifier output resistance, provides a small phase shift. It will also provide some attenuation of overtones.

Capacitor C_1, combined with the crystal resistance, provides additional phase shift.

C_1 and C_2 can affect the start-up time if they increase dramatically in size. As C_1 and C_2 increase, the start-up time increases until the oscillator reaches a point where it does not start up any more.

It is recommended for fast and reliable oscillator start-up (over the manufacturing process range) that the load capacitors be sized as low as possible without resulting in overtone operation.

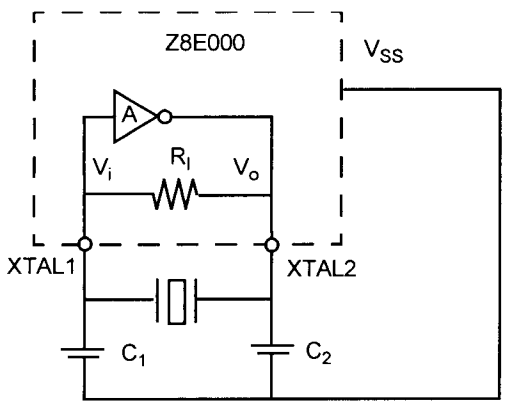


Figure 14. Pierce Oscillator with Internal Feedback Circuit

Layout

Traces connecting crystal, caps, and the Z8E000 oscillator pins should be as short and wide as possible, to reduce parasitic inductance and resistance. The components (caps, crystal, resistors) should be placed as close as possible to the oscillator pins of the Z8E000.

The traces from the oscillator pins of the IC and the ground side of the lead caps should be guarded from all other traces (clock, V_{CC}, address/data lines, system ground) to reduce cross talk and noise injection. Guarding is usually accomplished by keeping other traces and system ground trace planes away from the oscillator circuit, and by placing a Z8E000 device V_{SS} ground ring around the traces/components. The ground side of the oscillator lead caps should be connected to a single trace of the Z8E000 V_{SS} (GND) pin. The ground side of these caps should not be shared with any other system ground trace or components except at the Z8E000 device V_{SS} pin. The objective is to prevent differential system ground noise injection into the oscillator (Figure 15).

Indications of an Unreliable Design

There are two major indicators that are used in working designs to determine their reliability over full lot and temperature variations. They are:

Start-up Time. If start-up time is excessive, or varies widely from unit to unit, there is probably a gain problem. C_1 and C_2 require reduction if the amplifier gain is not adequate at frequency, or crystal R's are too large.

Output Level. The signal at the amplifier output should swing from ground to V_{CC} to indicate adequate gain in the amplifier. As the oscillator starts up, the signal amplitude grows until clipping occurs. At this point, the loop gain is effectively reduced to unity, and constant oscillation is achieved. A signal of less than 2.5 volts peak-to-peak is an indication that low gain can be a problem. Either C_1 or C_2 should be made smaller or a low-resistance crystal should be used.

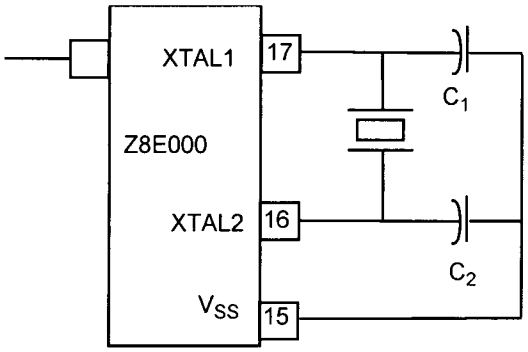
Circuit Board Design Rules

The following circuit board design rules are suggested:

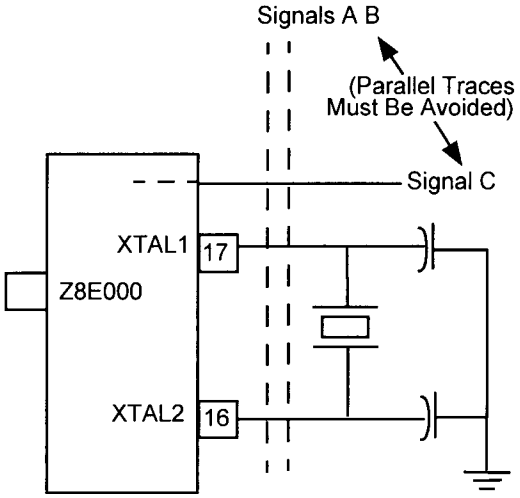
- To prevent induced noise, the crystal and load capacitors should be physically located as close to the Z8E000 as possible.
- Signal lines should not run parallel to the clock oscillator inputs. In particular, the crystal input circuitry and the internal system clock output should be separated as much as possible.

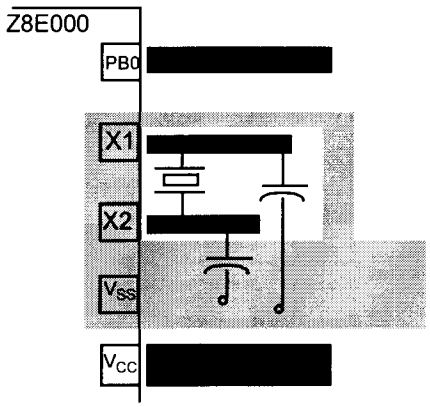
OSCILLATOR OPERATION (Continued)

- V_{CC} power lines should be separated from the clock oscillator input circuitry.
- Resistance between XTAL1 or XTAL2 and the other pins should be greater than 10 MΩ.



Clock Generator Circuit





Board Design Example
(Top View)

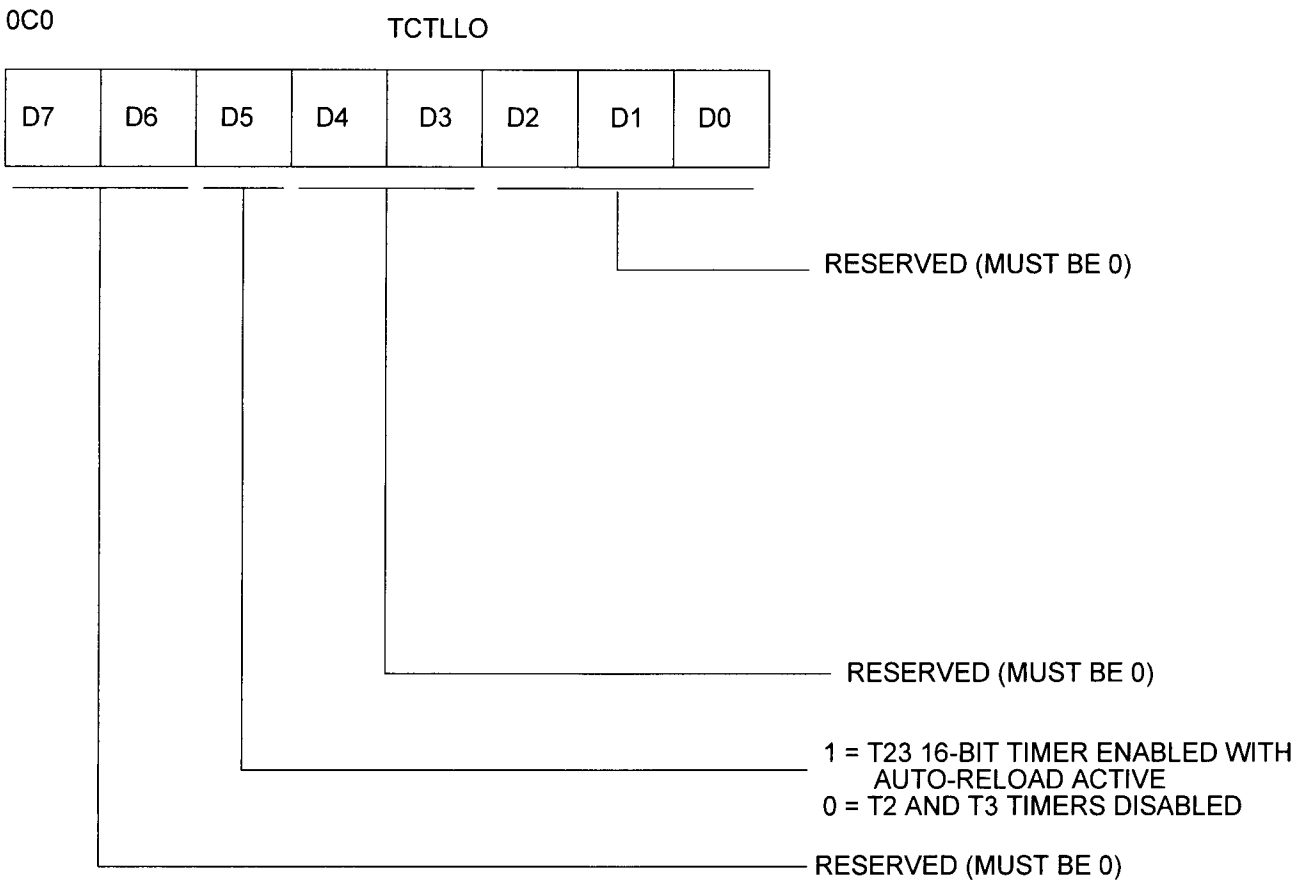
Figure 15. Circuit Board Design Rules

Crystals and Resonators

Crystals and ceramic resonators (Figure 16) should have the following characteristics to ensure proper oscillator operation:

Crystal Cut	AT (crystal only)
Mode	Parallel, Fundamental Mode
Crystal Capacitance	<7pF
Load Capacitance	10pF < CL < 220 pF, 15 typical
Resistance	100 ohms max

Depending on operation frequency, the oscillator can require the addition of capacitors C_1 and C_2 (shown in Figure 17 and Figure 18). The capacitance values are dependent on the manufacturer's crystal specifications.



Note: Timer T23 is a standard 16-bit timer formed by cascading 8-bit timers t3(msb) and t2(lsb).

Figure 20. TCTLLO Register

Each 8-bit timer is equipped with a pair of readable and writable registers, which are both readable and writable. One of the registers is defined to contain the auto-initialization value for the timer, while the second register contains the current value for the timer. When a timer is enabled, the timer will decrement whatever value is currently held in its count register. From that point, the timer continues decrementing until it reaches 0, at which time an interrupt will be generated and the contents of the auto-initialization register are optionally copied into the count value register. If auto-initialization is not enabled, the timer will stop counting upon reaching 0, and control logic will clear the appropriate control register bit to disable the timer. This operation is referred to as a "single-shot". If auto-initialization is enabled, the timer will continue counting from the initialization value. Software should not attempt to use registers that are defined as having timer functionality for any other purpose.

Software is allowed to write to any register at any time, but care should be taken if timer registers are updated while the timer is enabled. If software updates the count value while the timer is in operation, the timer will continue counting based upon the software-updated value. Strange behavior can result if the software update occurred at exactly the point that the timer was reaching 0 to trigger an interrupt and/or reload.

Similarly, if software updates the initialization value register while the timer is active, the next time that the timer reaches 0, it will be initialized using the updated value. Again, strange behavior could result if the initialization value register is being written while the timer is in the process of being initialized. Whether initialization is done with the new or old value is a function of the exact timing of the write operation. In all cases, the Z8E000 will prioritize the software write above that of a decrementer writeback. Howev-

TIMERS (Continued)

er, when hardware clears a control register bit for a timer that is configured for single-shot operation, the clearing of the control bit will override a software write. Reading either register can be done at any time, and will have no effect on the functionality of the timer.

When defined to operate as a single 16-bit entity, the entire 16-bit value must reach 0 before an interrupt is generated. In this case, a single interrupt will be generated, and the interrupt will correspond to the even 8-bit timer. For example, timers T2 and T3 are cascaded to form a single 16-bit timer, so the interrupt for the combined timer will be defined to be that of timer T2 rather than T3 (Figure 20). When a timer pair is specified to act as a single 16-bit timer, the even timer registers in the pair (timer T2) will be defined to hold the timer's least significant byte. Conversely, the odd timer in the pair (timer T3) will hold the timer's most significant byte.

In parallel with the posting of the interrupt request, the interrupting timer's count value will be initialized by copying the contents of the auto-initialization value register to the count value register.

Note: Any time that a timer pair is defined to act as a single 16-bit timer, the auto-reload function will be performed automatically. All 16-bit timers will continue counting while their interrupt requests are active, and will operate in a free-running manner.

If interrupts are disabled for a long period of time, it is possible for the timer to decrement to 0 again before its initial interrupt has been responded to. This condition is termed a degenerate case, and hardware is not required to detect it.

When the timer control register is written, all timers that are enabled by the write will begin counting using the value that is held in their count register. In this case, an auto-initialization is not performed. All timers can receive an internal clock source only. Each timer that is enabled will be updated every 8th XTAL clock cycle.

PORT A REGISTER DEFINITIONS

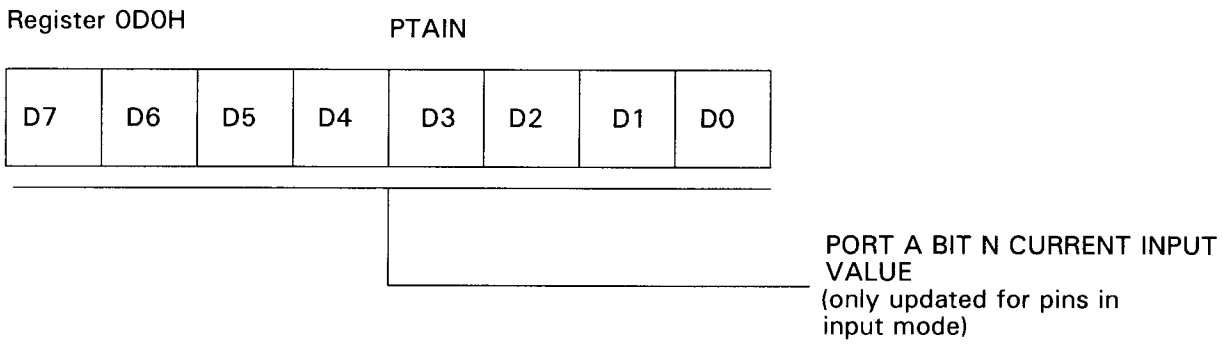


Figure 24. Port A Input Value Register

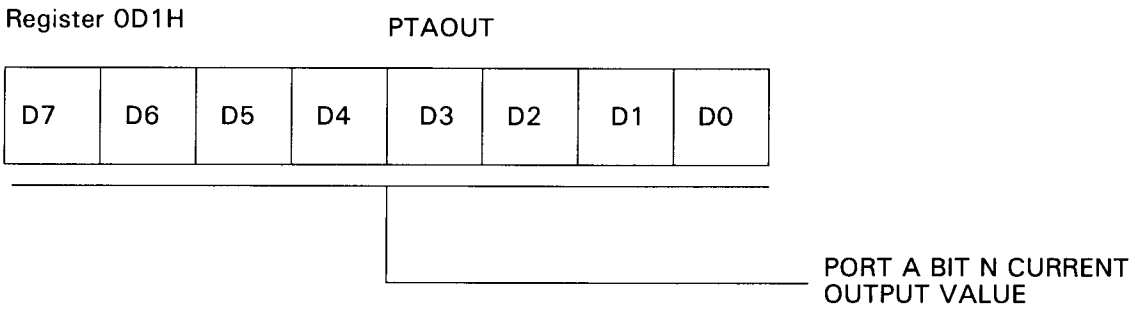


Figure 25. Port A Output Value Register

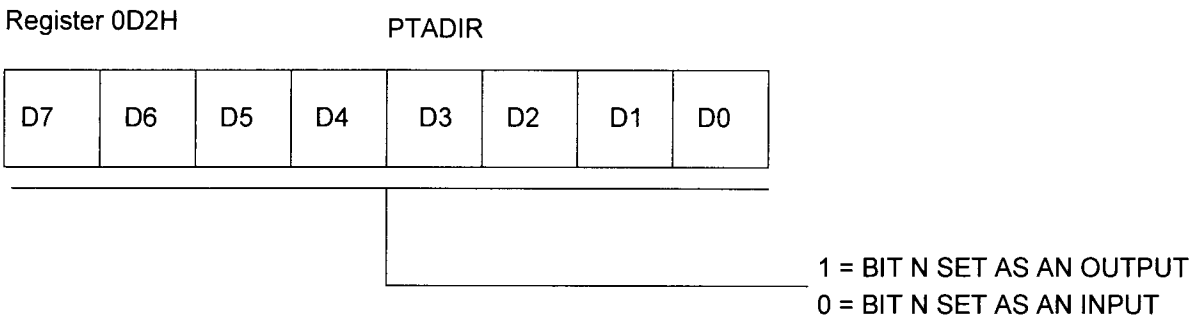


Figure 26. Port A Directional Control Register

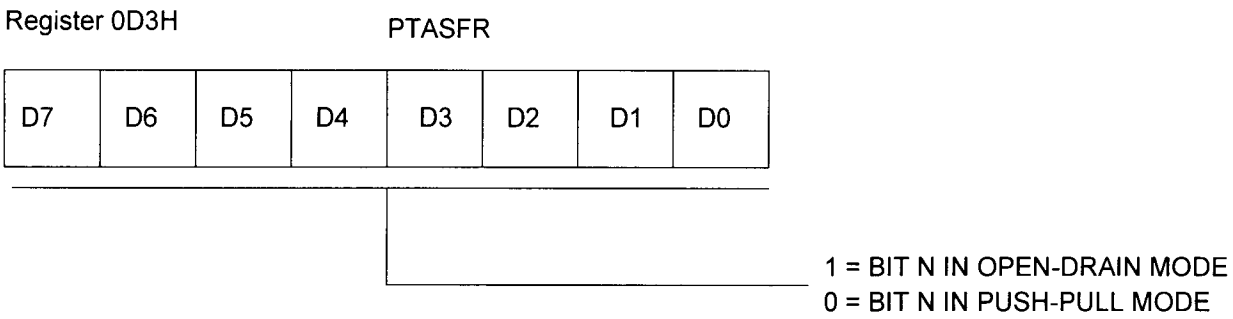


Figure 27. Port A Special Function Register

PORT B—PIN 1 CONFIGURATION

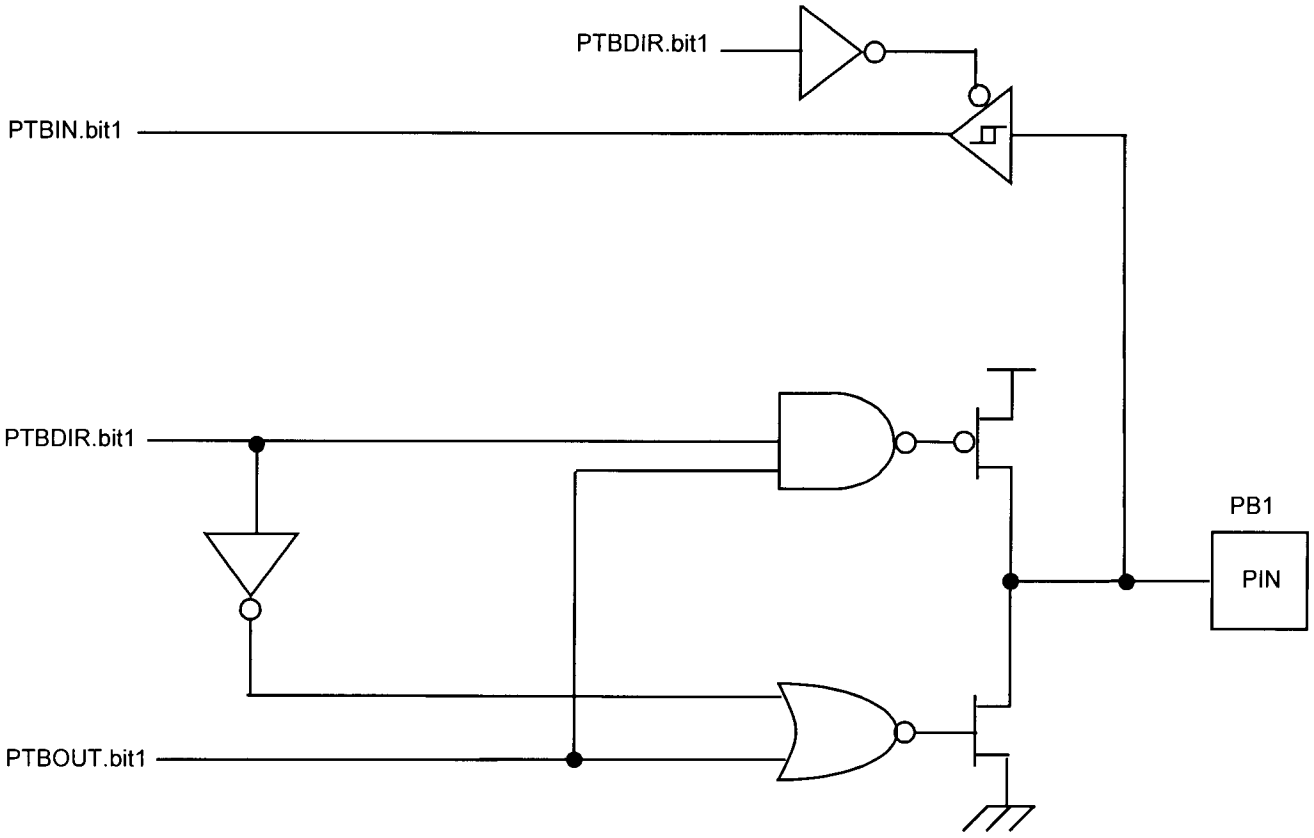


Figure 30. Port B Pin 1 Diagram

PORT B—PINS 3 AND 4 CONFIGURATION

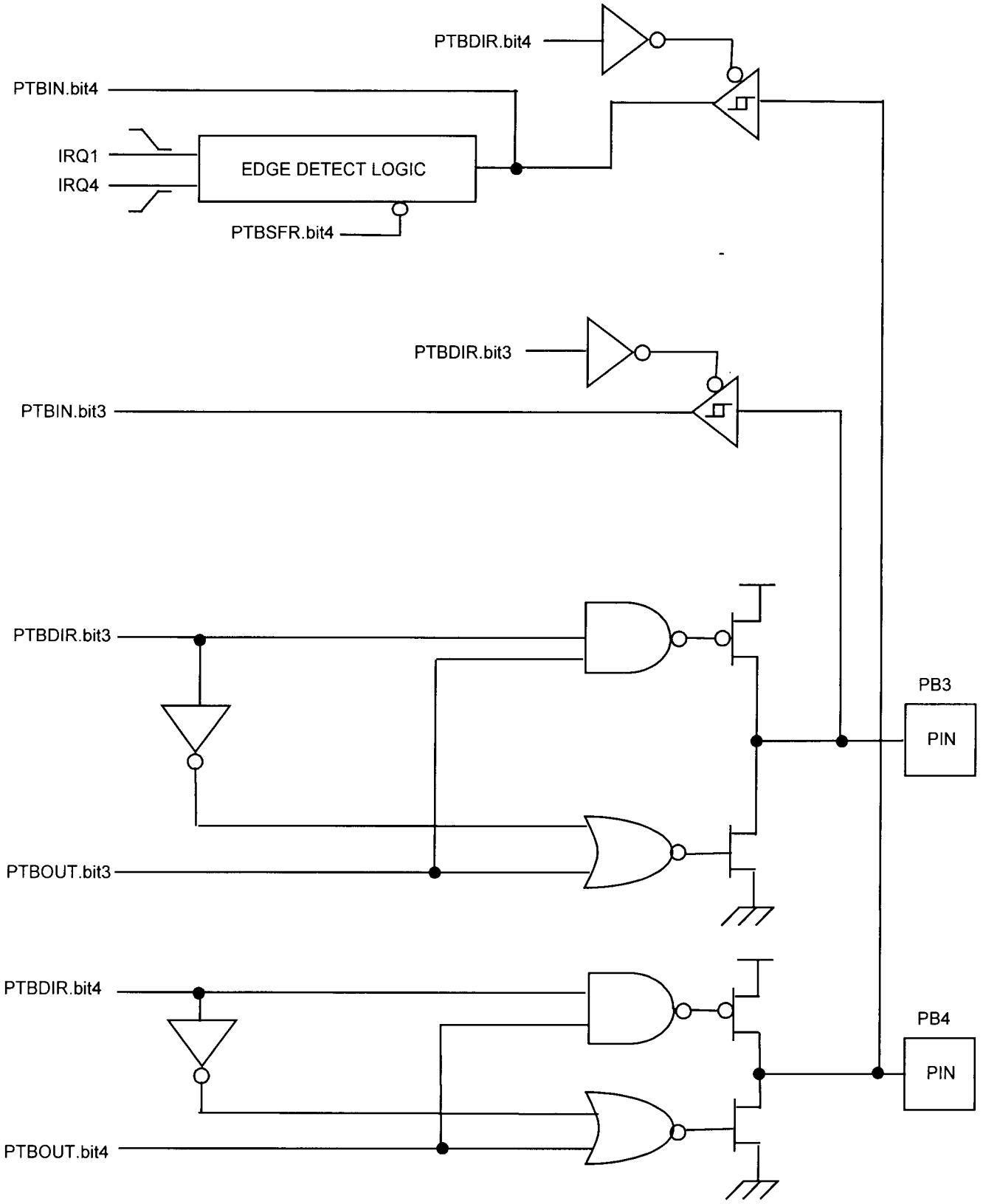


Figure 32. Port B Pins 3 and 4 Diagram

I/O PORT RESET CONDITIONS

Full Reset

Port A and Port B output value registers are not affected by $\overline{\text{RESET}}$.

On $\overline{\text{RESET}}$, the Port A and Port B directional control registers will be cleared to all zeros, which will define all pins in both ports as inputs.

On $\overline{\text{RESET}}$, the directional control registers redefine all pins as inputs, and the Port A and Port B input value registers will overwrite the previously held data with the current sample of the input pins.

On $\overline{\text{RESET}}$, the Port A and Port B special function registers will be cleared to all zeros, which will deactivate all port special functions.

Note: The SMR and WDT timeout events are NOT full device resets. None of the port control registers is affected by either of these events.

INPUT PROTECTION

All I/O pins on the Z8E000 have diode input protection. There is a diode from the I/O pad to V_{CC} and to V_{SS}. See Figure 37.

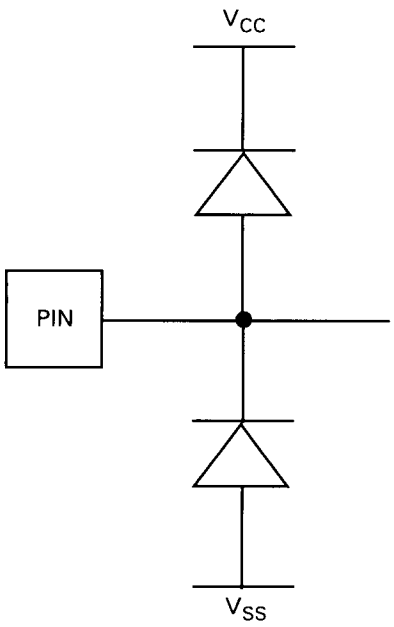


Figure 37. I/O Pin Diode Input Protection

However, on the Z8E000, the $\overline{\text{RESET}}$ pin has only the input protection diode from the pad to V_{SS}. See Figure 38.

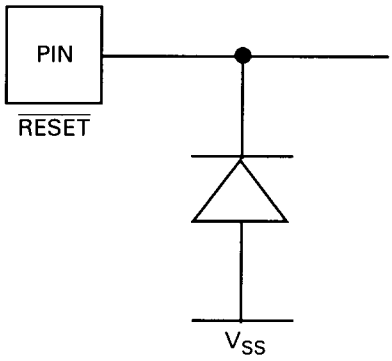


Figure 38. $\overline{\text{RESET}}$ Pin Input Protection

The High-side input protection diode was removed on this pin to allow the application of high voltage during the OTP programming mode.

For better noise immunity in applications that are exposed to system EMI, a clamping diode to V_{CC} from this pin is required to prevent entering the OTP programming mode, or to prevent high voltage from damaging this pin.

ORDERING INFORMATION

Standard Temperature		
18-Pin DIP	**18-Pin SOIC**	**20-Pin SSOP**
Z8E00010PSC	Z8E00010SSC	Z8E00010HSC

Extended Temperature		
18-Pin DIP	**18-Pin SOIC**	**20-Pin SSOP**
Z8E00010PEC	Z8E00010SEC	Z8E00010HEC

For fast results, contact your local ZiLOG sales office for assistance in ordering the part(s) required.

Codes	
Preferred Package	P = Plastic DIP
Longer Lead Time	S = SOIC
	H = SSOP
Preferred Temperature	S = 0°C to +70°C
	E = –40°C to +105°C
Speed	10 = 10 MHz
Environmental	C = Plastic Standard

Example:

Z 8E000 10 P S C is a Z86E000, 10 MHz, DIP, 0° to +70°C, Plastic Standard Flow