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Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	WDT
Number of I/O	13
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	32 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8e00010sec00tr

GENERAL DESCRIPTION (Continued)

Note: All signals with an overline, “ $\overline{}$ ”, are active Low. For example, $\overline{B/W}$ (WORD is active Low, only); $\overline{B/W}$ (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

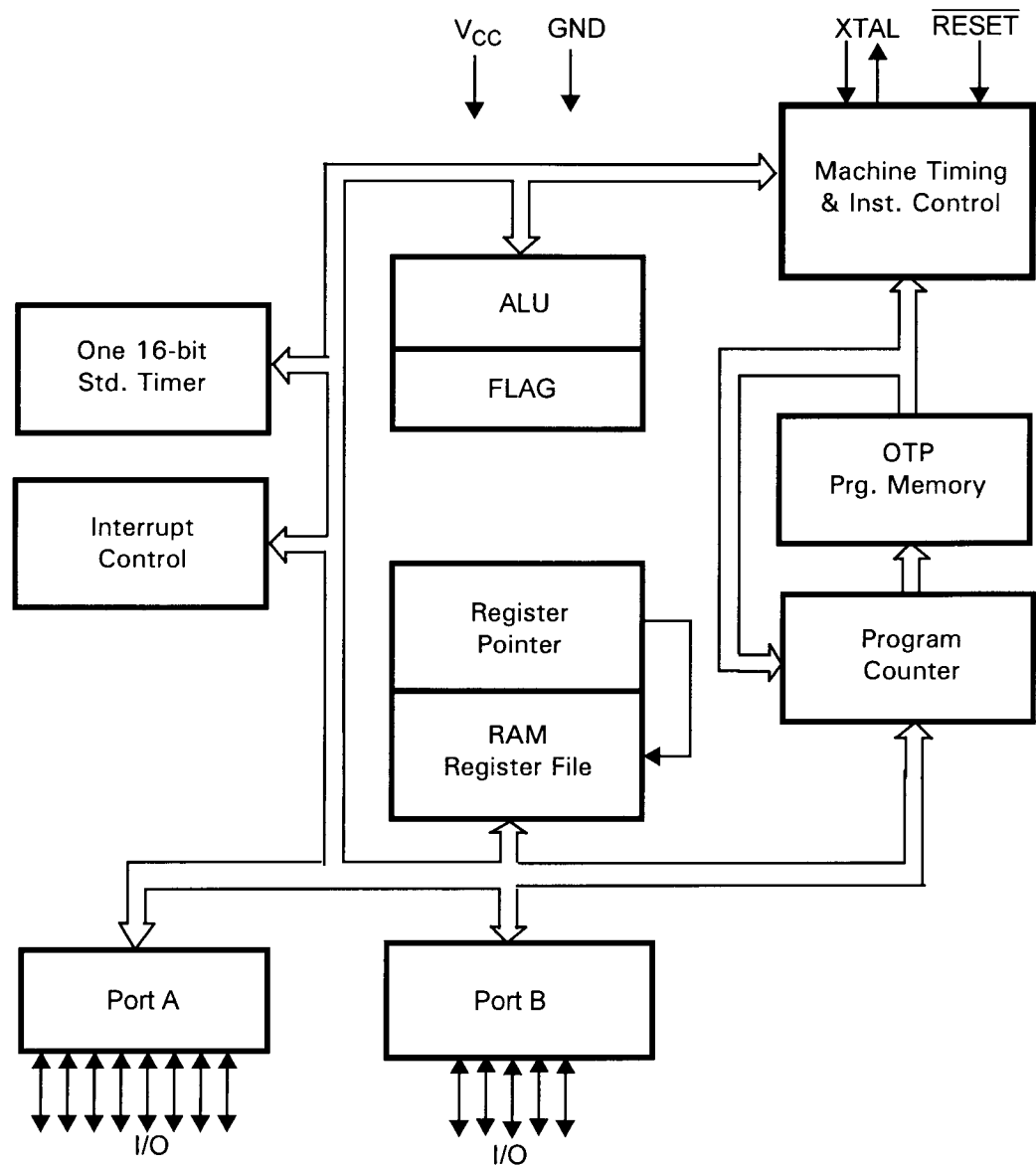


Figure 1. Functional Block Diagram

PIN DESCRIPTION

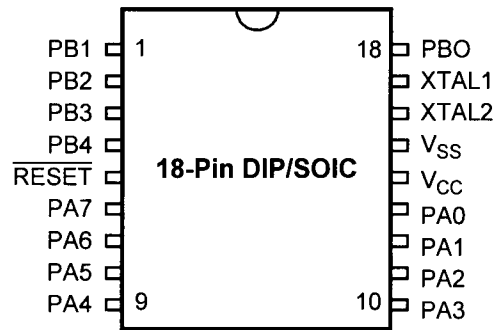


Figure 3. 18-Pin DIP/SOIC Pin Identification

Table 1. 18-Pin DIP/SOIC Pin Assignments

Standard Mode			
Pin #	Symbol	Function	Direction
1–4	PB1–PB4	Port B, Pins 1,2,3,4	In/Output
5	RESET	Reset	Input
6–9	PA7–PA4	Port A, Pins 7,6,5,4	In/Output
10–13	PA3–PA0	Port A, Pins 3,2,1,0	In/Output
14	V _{CC}	Power Supply	
15	V _{SS}	Ground	
16	XTAL2	Crystal Oscillator Clock	Output
17	XTAL1	Crystal Oscillator Clock	Input
18	PB0	Port B, Pin 0	In/Output

PIN DESCRIPTION (Continued)

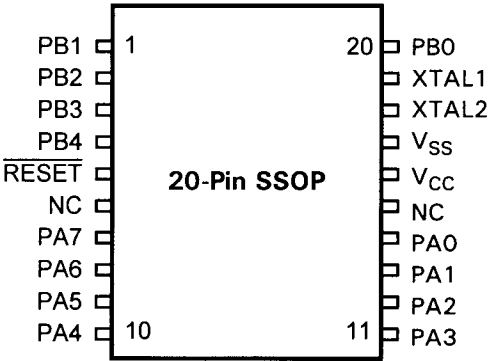


Figure 5. 20-Pin SSOP Pin Identification

Table 3. 20-Pin SSOP Pin Assignments

Standard Mode			
Pin #	Symbol	Function	Direction
1–4	PB1–PB4	Port B, Pins 1,2,3,4	In/Output
5	RESET	Reset	Input
6	NC	No Connection	
7–10	PA7–PA4	Port A, Pins 7,6,5,4	In/Output
11–14	PA3–PA0	Port A, Pins 3,2,1,0	In/Output
15	NC	No Connection	
16	V _{CC}	Power Supply	
17	V _{SS}	Ground	
18	XTAL2	Crystal Oscillator Clock	Output
19	XTAL1	Crystal Oscillator Clock	Input
20	PB0	Port B, Pin 0	In/Output

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 7).

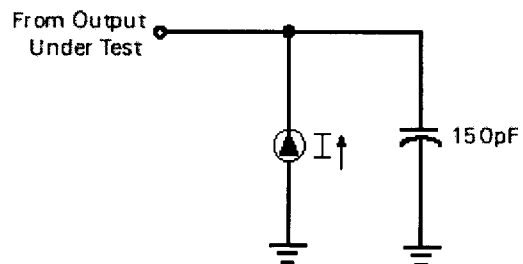


Figure 7. Test Load Diagram

CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$, $f = 1.0\text{ MHz}$, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$								
Sym	Parameter	V_{CC}^1	Min	Max	Typical @ 25°C ²	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.5V	$0.7V_{CC}$	$V_{CC}+0.3$	1.3	V	Driven by External Clock Generator	
		5.5V	$0.7V_{CC}$	$V_{CC}+0.3$	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.5V	$V_{SS}-0.3$	$0.2V_{CC}$	0.7	V	Driven by External Clock Generator	
		5.5V	$V_{SS}-0.3$	$0.2V_{CC}$	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.5V	$0.7V_{CC}$	$V_{CC}+0.3$	1.3	V		
		5.5V	$0.7V_{CC}$	$V_{CC}+0.3$	2.5	V		
V_{IL}	Input Low Voltage	3.5V	$V_{SS}-0.3$	$0.2V_{CC}$	0.7	V		
		5.5V	$V_{SS}-0.3$	$0.2V_{CC}$	1.5	V		
V_{OH}	Output High Voltage	3.5V	$V_{CC}-0.4$		3.1	V	$I_{OH} = -2.0 \text{ mA}$	
		5.5V	$V_{CC}-0.4$		4.8	V	$I_{OH} = -2.0 \text{ mA}$	
V_{OL1}	Output Low Voltage	3.5V		0.6	0.2	V	$I_{OL} = +4.0 \text{ mA}$	
		5.5V		0.4	0.1	V	$I_{OL} = +4.0 \text{ mA}$	
V_{OL2}	Output Low Voltage	3.5V		1.2	0.5	V	$I_{OL} = +6 \text{ mA}$	
		5.5V		1.2	0.5	V	$I_{OL} = +12 \text{ mA}$	
V_{RH}	Reset Input High Voltage	3.5V	$0.5V_{CC}$	V_{CC}	1.1	V		
		5.5V	$0.5V_{CC}$	V_{CC}	2.2	V		
V_{RL}	Reset Input Low Voltage	3.5V	$V_{SS}-0.3$	$0.2V_{CC}$	0.9	V		
		5.5V	$V_{SS}-0.3$	$0.2V_{CC}$	1.4	V		
I_{IL}	Input Leakage	3.5V	-1.0	2.0	0.064	μA	$V_{IN} = 0\text{V}, V_{CC}$	
		5.5V	-1.0	2.0	0.064	μA	$V_{IN} = 0\text{V}, V_{CC}$	
I_{OL}	Output Leakage	3.5V	-1.0	2.0	0.114	μA	$V_{IN} = 0\text{V}, V_{CC}$	
		5.5V	-1.0	2.0	0.114	μA	$V_{IN} = 0\text{V}, V_{CC}$	
I_{IR}	Reset Input Current	3.5V	-10	-60	-30	μA		
		5.5V	-20	-180	-100	μA		
I_{CC}	Supply Current	3.5V		2.5	2.0	mA	@ 10 MHz	3,4
		5.5V		6.0	4.0	mA	@ 10 MHz	3,4
I_{CC1}	Standby Current	3.5V		2.0	1.0	mA	Halt Mode $V_{IN} = 0\text{V}$ $V_{CC}@10 \text{ MHz}$	3,4
		5.5V		6.0	4.0	mA	Halt Mode $V_{IN} = 0\text{V}$ $V_{CC}@10 \text{ MHz}$	3,4

DC ELECTRICAL CHARACTERISTICS (Continued)

T _A = −40°C to +105°C								
Sym	Parameter	V _{CC} ¹	Min	Max	Typical @ 25°C ²	Units	Conditions	Notes
V _{CH}	Clock Input High Voltage	4.5V	0.7 V _{CC}	V _{CC} +0.3	2.5	V	Driven by External Clock Generator	
		5.5V	0.7 V _{CC}	V _{CC} +0.3	2.5	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	4.5V	V _{SS} −0.3	0.2 V _{CC}	1.5	V	Driven by External Clock Generator	
		5.5V	V _{SS} −0.3	0.2 V _{CC}	1.5	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	4.5V	0.7 V _{CC}	V _{CC} +0.3	2.5	V		
		5.5V	0.7 V _{CC}	V _{CC} +0.3	2.5	V		
V _{IL}	Input Low Voltage	4.5V	V _{SS} −0.3	0.2 V _{CC}	1.5	V		
		5.5V	V _{SS} −0.3	0.2 V _{CC}	1.5	V		
V _{OH}	Output High Voltage	4.5V	V _{CC} −0.4		4.8	V	I _{OH} = −2.0 mA	
		5.5V	V _{CC} −0.4		4.8	V	I _{OH} = −2.0 mA	
V _{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I _{OL} = +4.0 mA	
		5.5V		0.4	0.1	V	I _{OL} = +4.0 mA	
V _{OL2}	Output Low Voltage	4.5V		1.2	0.5	V	I _{OL} = +12 mA,	
		5.5V		1.2	0.5	V	I _{OL} = +12 mA,	
V _{RH}	Reset Input High Voltage	4.5V	0.5V _{CC}	V _{CC}	1.1	V		
		5.5V	0.5V _{CC}	V _{CC}	2.2	V		
I _{IL}	Input Leakage	4.5V	−1.0	2.0	<1.0	μA	V _{IN} = 0V, V _{CC}	
		5.5V	−1.0	2.0	<1.0	μA	V _{IN} = 0V, V _{CC}	
I _{OL}	Output Leakage	4.5V	−1.0	2.0	<1.0	μA	V _{IN} = 0V, V _{CC}	
		5.5V	−1.0	2.0	<1.0	μA	V _{IN} = 0V, V _{CC}	
I _{IR}	Reset Input Current	4.5V	−18	−180	−112	mA		
		5.5V	−18	−180	−112	mA		
I _{CC}	Supply Current	4.5V		7.0	4.0	mA	@ 10 MHz	3,4
		5.5V		7.0	4.0	mA	@ 10 MHz	3,4
I _{CC1}	Standby Current	4.5V		2.0	1.0	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 10 MHz	3,4
		5.5V		2.0	1.0	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 10 MHz	3,4

AC ELECTRICAL CHARACTERISTICS

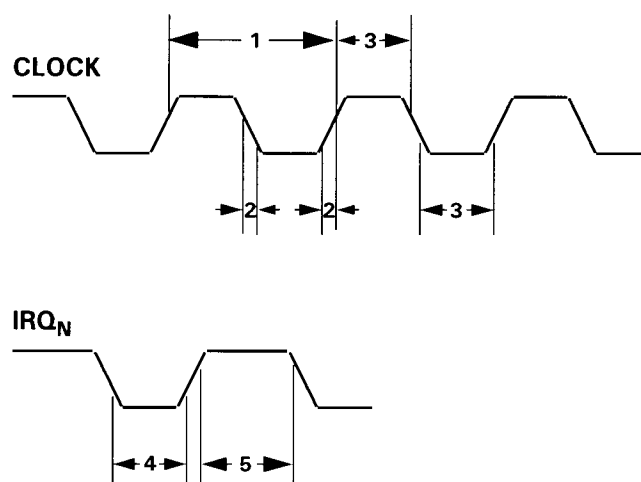


Figure 8. AC Electrical Timing Diagram

Table 5. Additional Timings

$T_A = -40^{\circ}\text{C to } +105^{\circ}\text{C}$
@ 10 MHz

No	Symbol	Parameter	V_{CC}^1	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.5V	100	DC	ns	2
			5.5V	100	DC	ns	2
2	TrC, TfC	Clock Input Rise and Fall Times	3.5V		15	ns	2
			5.5V		15	ns	2
3	TwC	Input Clock Width	3.5V	50		ns	2
			5.5V	50		ns	2
4	TwIL	Int. Request Input Low Time	3.5V	70		ns	2
			5.5V	70		ns	2
5	TwIH	Int. Request Input High Time	3.5V	5TpC			2
			5.5V	5TpC			2
6	Twsm	STOP Mode Recovery Width Spec.	3.5V	12		ns	
			5.5V	12		ns	
7	Tost	Oscillator Start-Up Time	3.5V		5TpC		
			5.5V		5TpC		

Notes:

1. The V_{DD} voltage specification of 3.5V guarantees 3.5V. The V_{DD} voltage specification of 5.5V guarantees $5.0V \pm 0.5V$.
2. Timing Reference uses $0.7 V_{CC}$ for a logic 1 and $0.2 V_{CC}$ for a logic 0.

Z8E000 WATCH-DOG TIMER (WDT) (Continued)

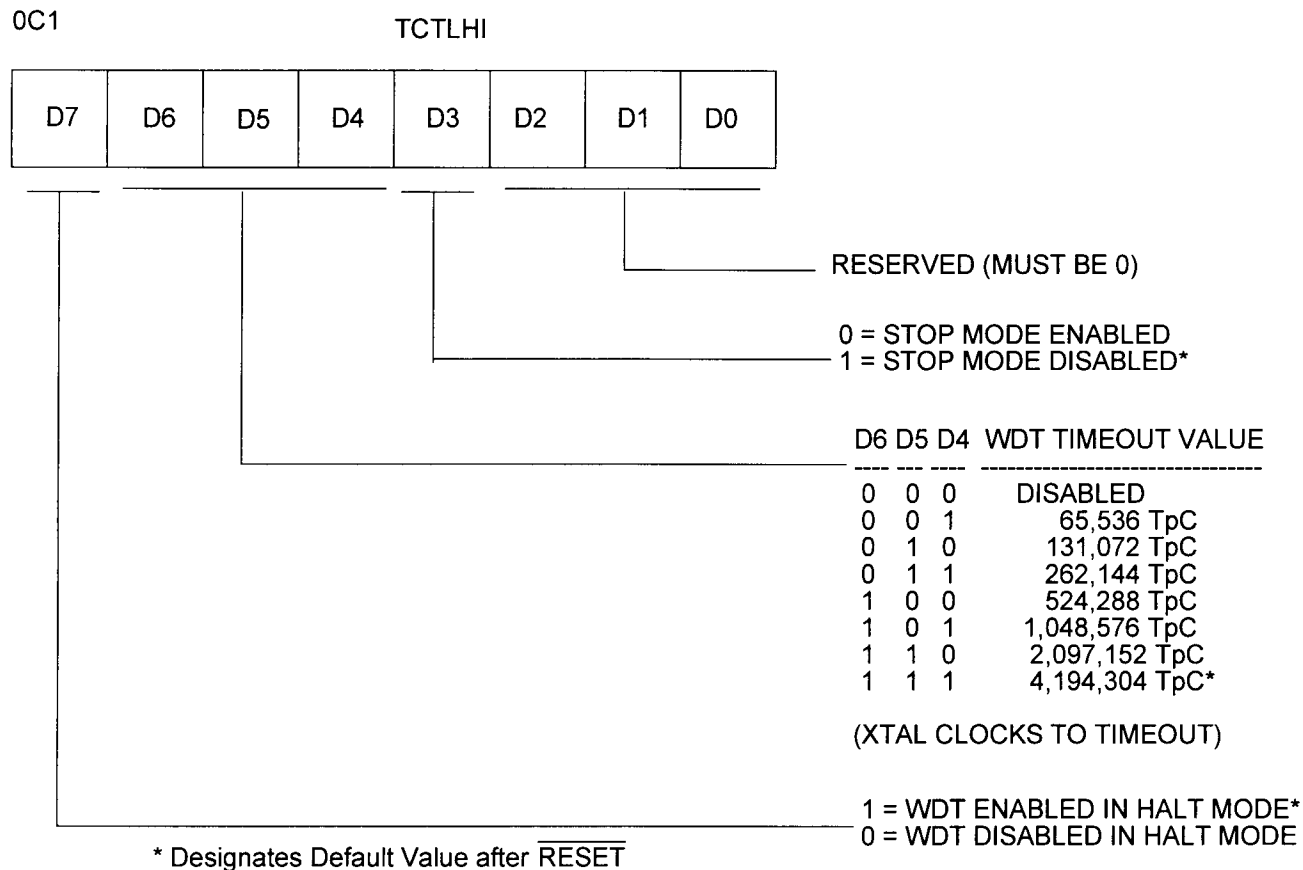


Figure 12. Z8E000 TCTLHI Register for Control of WDT

Note: The WDT can only be disabled via software if the first instruction out of RESET performs this function. Logic within the Z8E000 will detect that it is in the process of executing the first instruction after the part leaves RESET. During the execution of this instruction, the upper five bits of the TCTLHI register can be written. After this first instruction, hardware will not allow the upper five bits of this register to be written.

The TCTLHI bits for control of the WDT are described below:

WDT Time Select (D6, D5, D4). Bits 6, 5, and 4 determine the time-out period. Table 7 indicates the range of time-out values that can be obtained. The default values of D6, D5, and D4 are all 1, thus setting the WDT to its maximum timeout period when coming out of RESET.

Table 7. Time-Out Period of the WDT

D6	D5	D4	Crystal Clocks to Timeout	Time-Out Using a10 MHz Crystal
0	0	0	Disabled	Disabled
0	0	1	65,536 TpC	6.55 ms
0	1	0	131,072 TpC	13.11 ms
0	1	1	262,144 TpC	26.21 ms
1	0	0	524,288 TpC	52.43 ms
1	0	1	1,048,576 TpC	104.86 ms
1	1	0	2,097,152 TpC	209.72 ms
1	1	1	4,194,304 TpC	419.43 ms

Notes:

TpC = XTAL clock cycle.

The default on reset is D6 = D5 = D4 = 1.

WDT During HALT (D7). This bit determines whether or not the WDT is active during HALT Mode. A “1” indicates active during HALT. A “0” prevents the WDT from resetting the part while halted. Coming out of reset, the WDT will be enabled during HALT Mode.

STOP MODE (D3). Coming out of $\overline{\text{RESET}}$, the Z8E000 will have the STOP Mode disabled. If an application re-

quires use of STOP Mode, bit D3 must be cleared immediately upon leaving $\overline{\text{RESET}}$. If bit D3 is set, the STOP instruction will execute as a NOP. If bit D3 is cleared, the STOP instruction will enter Stop Mode. Whenever the Z8E000 wakes up after having been in STOP Mode, the STOP Mode will be disabled once again.

Bits 2, 1 and 0. These bits are reserved and must be 0.

POWER-DOWN MODES

In addition to the standard RUN mode, the Z8E000 MCU supports two Power-Down modes to minimize device cur-

rent consumption. The two modes supported are HALT and STOP.

HALT MODE OPERATION

The HALT Mode suspends instruction execution and turns off the internal CPU clock. The on-chip oscillator circuit remains active, so the internal clock continues to run and is applied to the timers and interrupt logic.

To enter the HALT Mode, the Z8E000 only requires a HALT instruction. It is NOT necessary to execute a NOP instruction immediately before the HALT instruction.

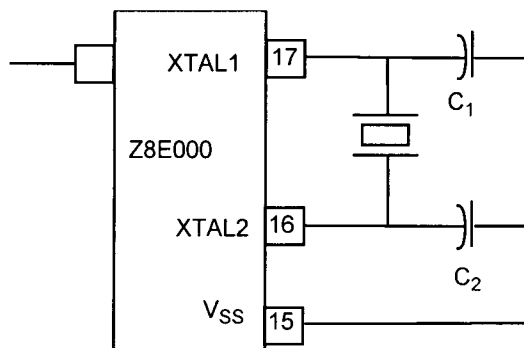
The HALT Mode can be exited by servicing an interrupt (either externally or internally). Upon completion of the interrupt service routine, the user program continues from the instruction after HALT.

The HALT Mode can also be exited via a $\overline{\text{RESET}}$ activation or a Watch-Dog Timer (WDT) timeout. In these cases, program execution will restart at the reset address 0020H.

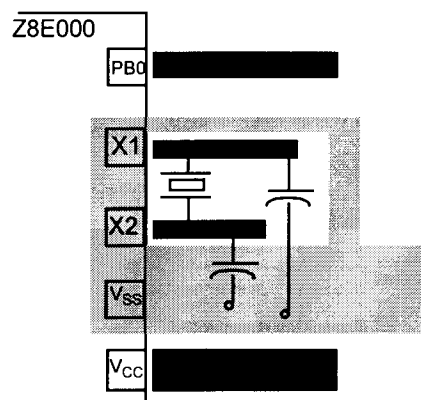
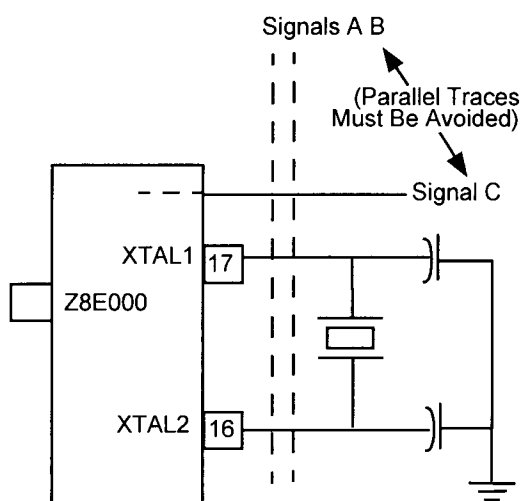
7F HALT ; enter HALT Mode

OSCILLATOR OPERATION (Continued)

- V_{CC} power lines should be separated from the clock oscillator input circuitry.
- Resistance between XTAL1 or XTAL2 and the other pins should be greater than $10\text{ M}\Omega$.



Clock Generator Circuit



Board Design Example
(Top View)

Figure 15. Circuit Board Design Rules

Crystals and Resonators

Crystals and ceramic resonators (Figure 16) should have the following characteristics to ensure proper oscillator operation:

Crystal Cut	AT (crystal only)
Mode	Parallel, Fundamental Mode
Crystal Capacitance	<7pF
Load Capacitance	10pF < CL < 220 pF, 15 typical
Resistance	100 ohms max

Depending on operation frequency, the oscillator can require the addition of capacitors C_1 and C_2 (shown in Figure 17 and Figure 18). The capacitance values are dependent on the manufacturer's crystal specifications.

TIMERS (Continued)

er, when hardware clears a control register bit for a timer that is configured for single-shot operation, the clearing of the control bit will override a software write. Reading either register can be done at any time, and will have no effect on the functionality of the timer.

When defined to operate as a single 16-bit entity, the entire 16-bit value must reach 0 before an interrupt is generated. In this case, a single interrupt will be generated, and the interrupt will correspond to the even 8-bit timer. For example, timers T2 and T3 are cascaded to form a single 16-bit timer, so the interrupt for the combined timer will be defined to be that of timer T2 rather than T3 (Figure 20). When a timer pair is specified to act as a single 16-bit timer, the even timer registers in the pair (timer T2) will be defined to hold the timer's least significant byte. Conversely, the odd timer in the pair (timer T3) will hold the timer's most significant byte.

In parallel with the posting of the interrupt request, the interrupting timer's count value will be initialized by copying

the contents of the auto-initialization value register to the count value register.

Note: Any time that a timer pair is defined to act as a single 16-bit timer, the auto-reload function will be performed automatically. All 16-bit timers will continue counting while their interrupt requests are active, and will operate in a free-running manner.

If interrupts are disabled for a long period of time, it is possible for the timer to decrement to 0 again before its initial interrupt has been responded to. This condition is termed a degenerate case, and hardware is not required to detect it.

When the timer control register is written, all timers that are enabled by the write will begin counting using the value that is held in their count register. In this case, an auto-initialization is not performed. All timers can receive an internal clock source only. Each timer that is enabled will be updated every 8th XTAL clock cycle.

RESET CONDITIONS

After a hardware $\overline{\text{RESET}}$, the timers are disabled. See Table 5 for timer control, value, and auto-initialization register status after $\overline{\text{RESET}}$.

I/O PORTS

The Z8E000 has 13 lines dedicated to input and output. These lines are grouped into two ports known as Port A and Port B. Port A is an 8-bit port that is bit-programmable as either inputs or outputs. Port B can be programmed to provide standard input/output or the following special functions: SMR input and external interrupt inputs.

All ports have push-pull CMOS outputs. In addition, the outputs of Port A, on a bit-wise basis, can be configured for open-drain operation. As such, the register values for “/” at a given bit position only affect the bit in question.

Each port is defined by a set of four control registers. See Figure 21.

Directional Control and Special Function Registers

Each port on the Z8E000 has an associated and dedicated Directional Control Register that determines on a bit-wise basis whether a given port bit will operate as an input or as an output.

Each port on the Z8E000 has a Special Function Register that, in conjunction with the directional control register, implements on a bit-wise basis, and supports special functionality that can be defined for each particular port bit.

Input and Output Value Registers

Each port has an Output Value Register and an Input Value Register. For port bits configured as an input by means of the Directional Control Register, the Input Value Register

for that bit position will contain the current synchronized input value.

REGISTER	ADDRESS	IDENTIFIER
Port B SPECIAL FUNCTION	0D7H	PTBSFR
Port B DIRECTIONAL CONTROL	0D6H	PTBDIR
Port B OUTPUT VALUE	0D5H	PTBOUT
Port B INPUT VALUE	0D4H	PTBIN
Port A SPECIAL FUNCTION	0D3H	PTASFR
Port A DIRECTIONAL CONTROL	0D2H	PTADIR
Port A OUTPUT VALUE	0D1H	PTAOUT
Port A INPUT VALUE	0D0H	PTAIN

Figure 21. Z8E000 I/O Ports Registers

For port bits configured as an output by means of the Directional Control Register, the value held in the corresponding bit of the Output Value Register is driven directly onto the output pin. The opposite register bit for a given pin (the output register bit for an input pin and the input register bit for an output pin) will hold their previous value. They will not be changed by hardware nor will they have any effect on the hardware.

READ/WRITE OPERATIONS

The control for each port is done on a bit-wise basis. All bits are capable of operating as inputs or outputs, depending upon the setting of the port's directional control register. If configured as an input, each bit is provided a Schmitt-trigger. The output of the Schmitt-trigger is latched twice to perform a synchronization function, while the output of the synchronizer is fed to the port input register, which can be read by software.

A write to a port input register has the effect of updating the contents of the input register, but subsequent reads will not necessarily return the same value that was written. If the bit in question is defined as an input, the input register for that bit position will contain the current synchronized input value. Thus, writes to that bit position will be overwritten on the next clock cycle with the newly sampled input data. However, if the particular port bit is programmed as an output, the input register for that bit will retain the software-updated value. The port bits that are programmed as outputs do not sample the value being driven out.

Any bit in either port can be defined as an output by setting the appropriate bit in the directional control register. If such is the case, the value held in the appropriate bit of the port output register is driven directly onto the output pin.

Note: The above result does not necessarily reflect the actual output value. If an external error is holding an output pin

either High or Low against the output driver, the software read will return the *required* value, not the actual state caused by the contention. When a bit is defined as an output, the Schmitt-trigger on the input will be disabled to save power.

Updates to the output register will take effect based upon the timing of the internal instruction pipeline; however, this timing is referenced to the rising edge of the clock. The output register can be read at any time, and will return the current output value that is held. No restrictions are placed on the timing of reads and/or writes to any of the port registers with respect to the others, but care should be taken when updating the directional control and special function registers.

When updating a directional control register, the special function register should first be disabled. If this precaution is not taken, spurious events could take place as a result of the change in port I/O status. This precaution is especially important when defining changes in Port B, as the spurious event referred to above could be one or more interrupts. Clearing of the SFR register should be the first step in configuring the port, and setting the SFR register should be the final step in the port configuration process. To ensure deterministic behavior, the SFR register should not be written until the pins are being driven appropriately and all initialization has been completed.

PORT A

Port A is a general-purpose port (Figure 23). Each of its lines can be independently programmed as input or output via the Port A Directional Control Register (PTADIR at 0D2H) as seen in Figure 22. A bit set to a “1” in PTADIR configures the corresponding bit in Port A as an output, while a bit cleared to “0” configures the corresponding bit in Port A as an input.

The input buffers are Schmitt-triggered. Bits programmed as outputs can be individually programmed as either push-pull or open drain by setting the corresponding bit in the Special Function Register (PTASFR, Figure 27.)

Register 0D2H
PTADIR Register

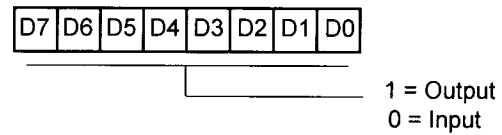


Figure 22. Port A Directional Control Register

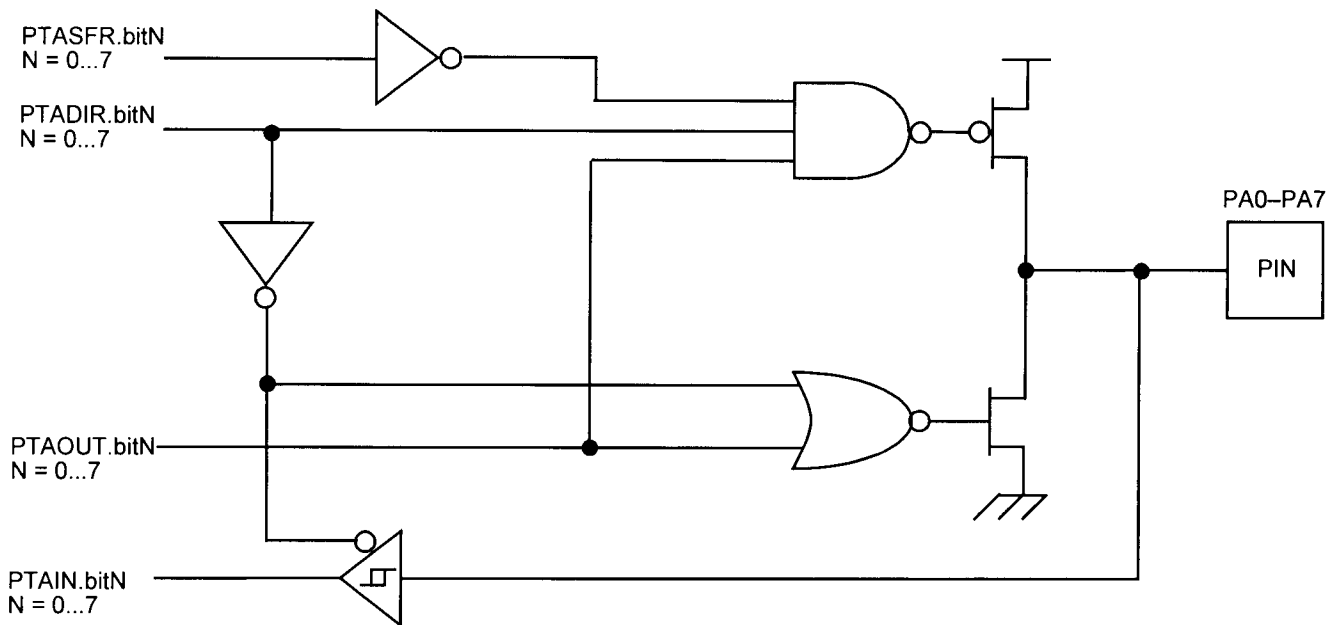


Figure 23. Port A Configuration with Open-Drain Capability and Schmitt-Trigger

Register 0D2H

PTADIR

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

1 = BIT N SET AS AN OUTPUT

0 = BIT N SET AS AN INPUT

Figure 26. Port A Directional Control Register

Register 0D3H

PTASFR

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

1 = BIT N IN OPEN-DRAIN MODE

0 = BIT N IN PUSH-PULL MODE

Figure 27. Port A Special Function Register

PORT B

Port B Description

Port B is a 5-bit, bidirectional, CMOS-compatible I/O port. These five I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered. See Figure 29 through Figure 33 for diagrams of all five Port B pins.

In addition to standard input/output capability on all five pins of Port B, each pin provides special functionality as indicated in Table 8:

Table 8. Port B Special Functions

Port Pin	Input Special Function	Output Special Function
PB0	Stop Mode Recovery Input	None
PB1	None	None
PB2	IRQ3	None
PB3	None	None
PB4	IRQ1/IRQ4	None

Special functionality is invoked via the Port B Special Function Register. See Figure 28 for the arrangement and control conventions for this register.

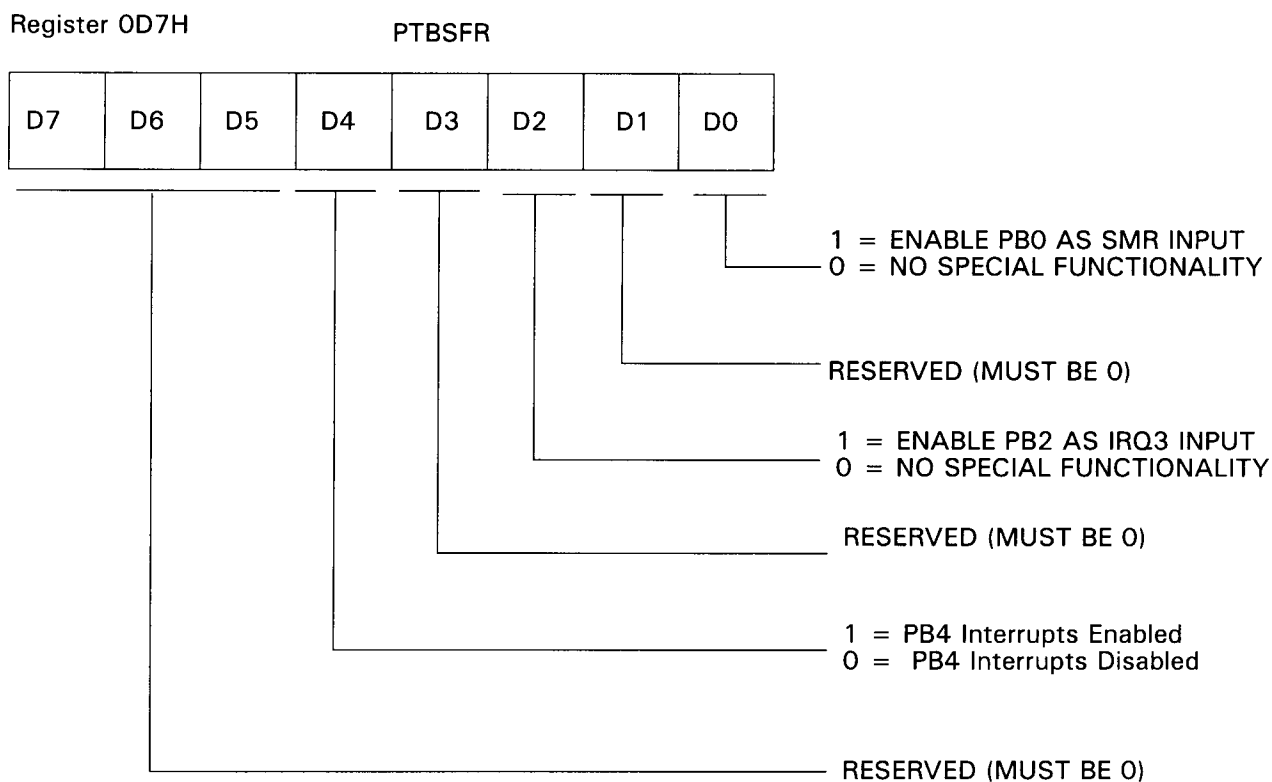


Figure 28. Port B Special Function Register

PORT B CONTROL REGISTER DEFINITIONS (Continued)

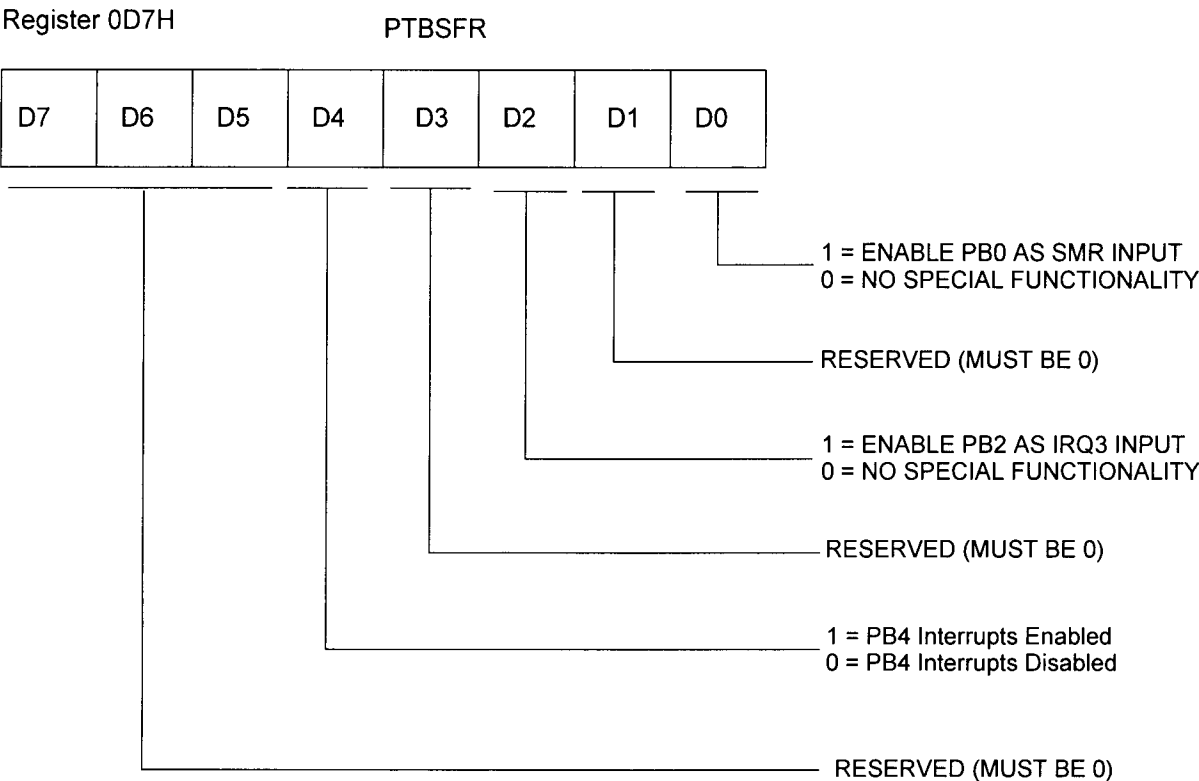


Figure 36. Port B Special Function Register

I/O PORT RESET CONDITIONS

Full Reset

Port A and Port B output value registers are not affected by RESET.

On $\overline{\text{RESET}}$, the Port A and Port B directional control registers will be cleared to all zeros, which will define all pins in both ports as inputs.

On $\overline{\text{RESET}}$, the directional control registers redefine all pins as inputs, and the Port A and Port B input value registers

will overwrite the previously held data with the current sample of the input pins.

On $\overline{\text{RESET}}$, the Port A and Port B special function registers will be cleared to all zeros, which will deactivate all port special functions.

Note: The SMR and WDT timeout events are NOT full device resets. None of the port control registers is affected by either of these events.

INPUT PROTECTION

All I/O pins on the Z8E000 have diode input protection. There is a diode from the I/O pad to V_{CC} and to V_{SS} . See Figure 37.

However, on the Z8E000, the $\overline{\text{RESET}}$ pin has only the input protection diode from the pad to V_{SS} . See Figure 38.

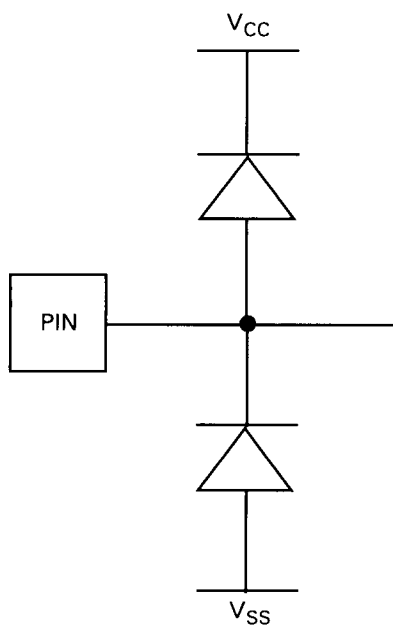


Figure 37. I/O Pin Diode Input Protection

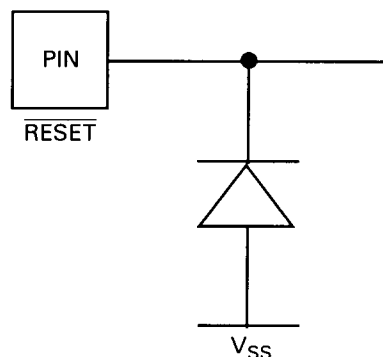
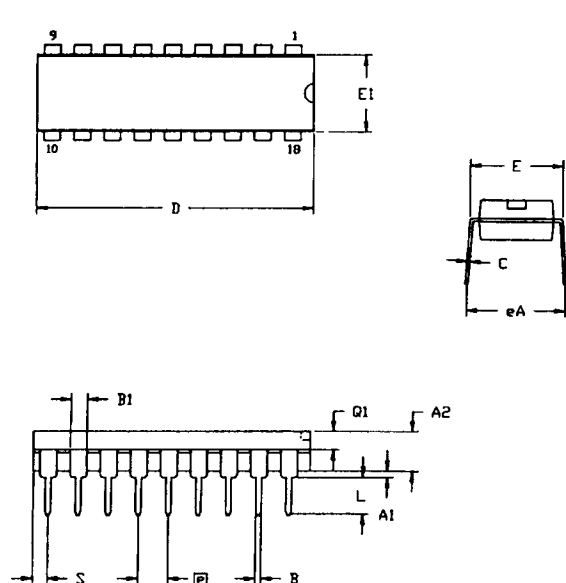


Figure 38. $\overline{\text{RESET}}$ Pin Input Protection

The High-side input protection diode was removed on this pin to allow the application of high voltage during the OTP programming mode.

For better noise immunity in applications that are exposed to system EMI, a clamping diode to V_{CC} from this pin is required to prevent entering the OTP programming mode, or to prevent high voltage from damaging this pin.

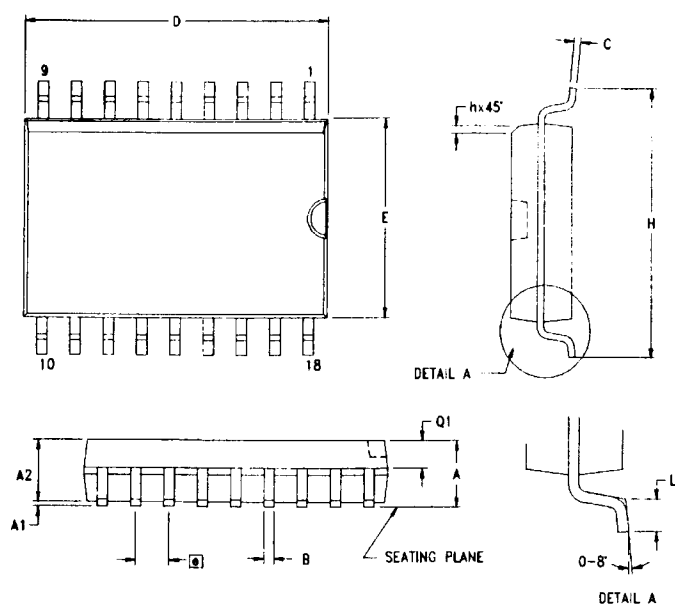
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
⌀	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

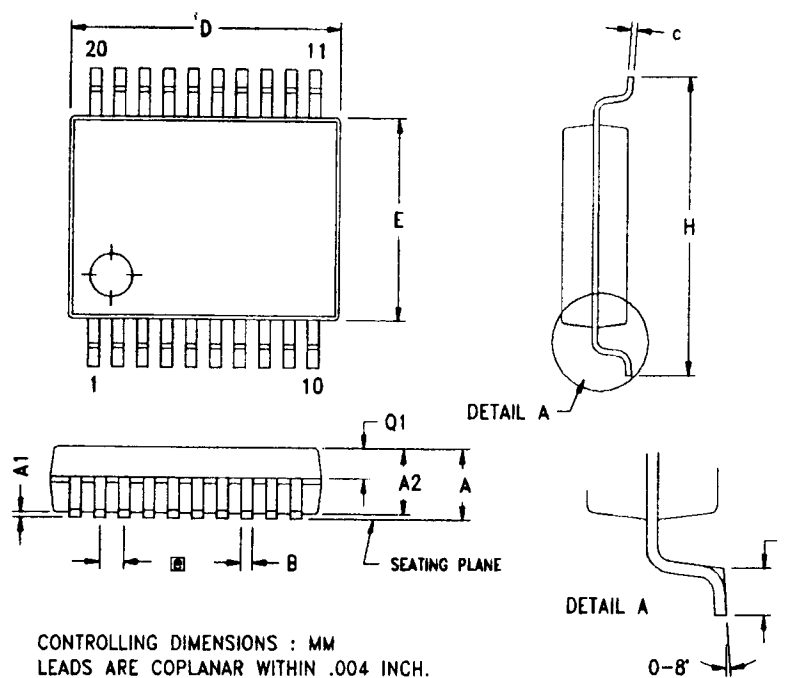
Figure 39. 18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
⌀	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 40. 18-Pin SOIC Package Diagram



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
B	0.25	0.30	0.38	0.010	0.012	0.015
C	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
ⓐ	0.65 TYP			0.0256 TYP		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032

Figure 41. 20-Pin SSOP Package Diagram