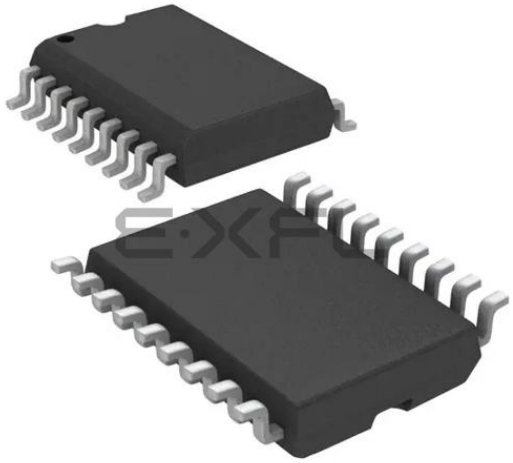

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	WDT
Number of I/O	13
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	32 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8e00010seg

GENERAL DESCRIPTION (Continued)

Note: All signals with an overline, "‾", are active Low. For example, B/$\overline{W}$ (WORD is active Low, only); $\overline{B}$/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

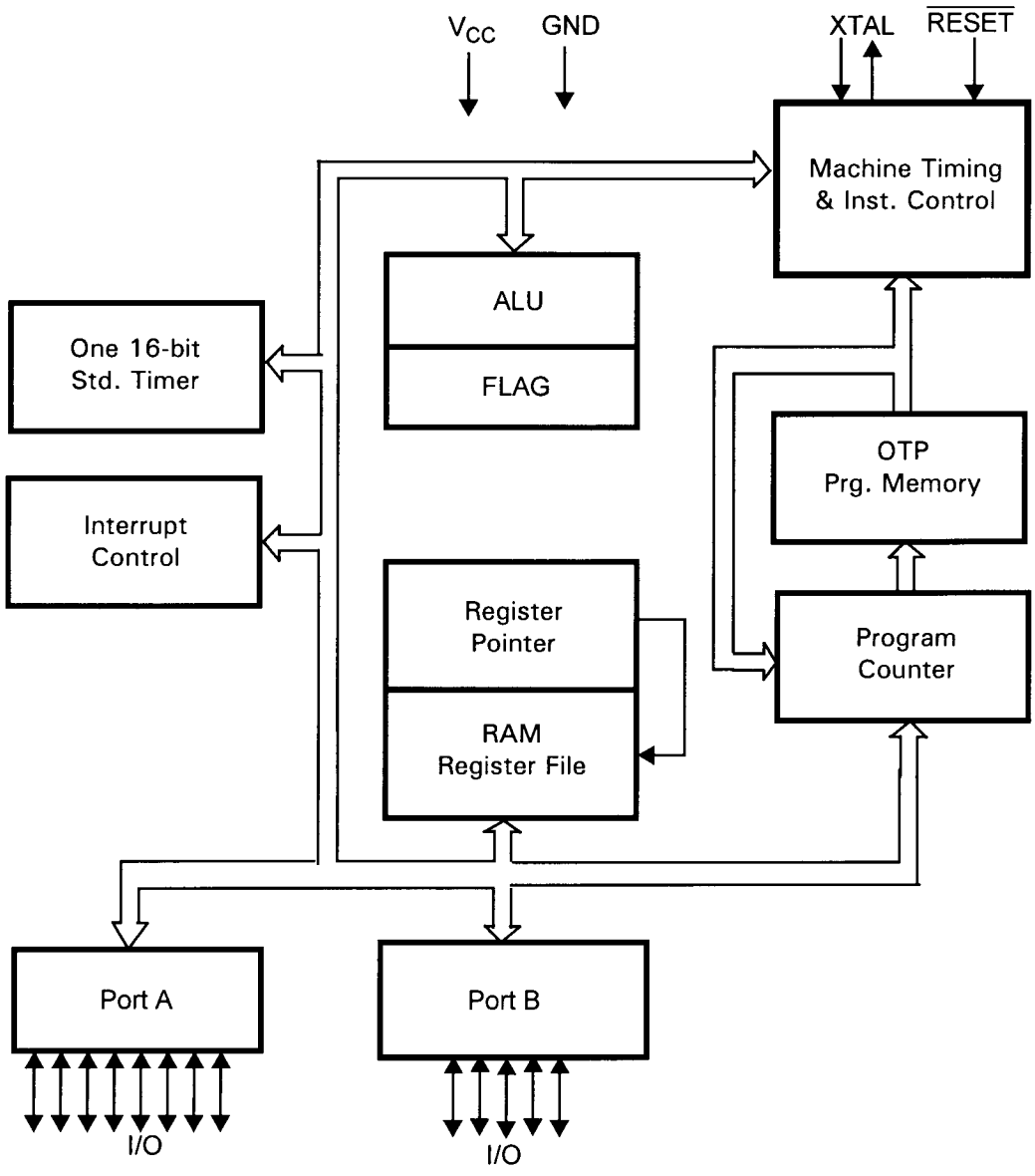


Figure 1. Functional Block Diagram

PIN DESCRIPTION

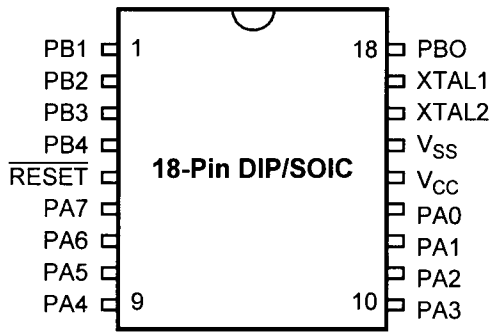


Figure 3. 18-Pin DIP/SOIC Pin Identification

Table 1. 18-Pin DIP/SOIC Pin Assignments

Standard Mode			
Pin #	**Symbol**	**Function**	**Direction**
1–4	PB1–PB4	Port B, Pins 1,2,3,4	In/Output
5	$\overline{\text{RESET}}$	Reset	Input
6–9	PA7–PA4	Port A, Pins 7,6,5,4	In/Output
10–13	PA3–PA0	Port A, Pins 3,2,1,0	In/Output
14	V_{CC}	Power Supply	
15	V_{SS}	Ground	
16	XTAL2	Crystal Oscillator Clock	Output
17	XTAL1	Crystal Oscillator Clock	Input
18	PB0	Port B, Pin 0	In/Output

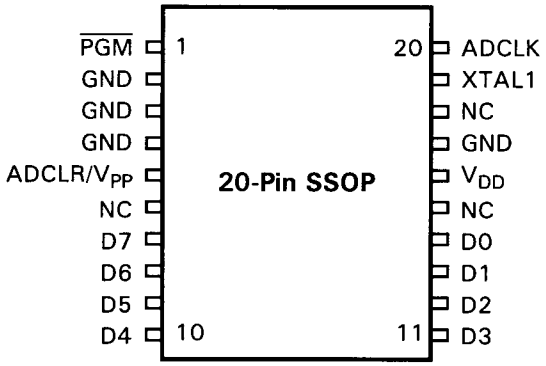


Figure 6. 20-Pin SSOP Pin Identification; EPROM Programming Mode

Table 4. 20-Pin SSOP Pin Assignments; EPROM Programming Mode

EPROM Programming Mode

Pin #	Symbol	Function	Direction
1	$\overline{PGM}$	Program Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clock/Program Voltage	Input
6	NC	No Connection	
7–10	D7–D4	Data 7,6,5,4	In/Output
11–14	D3–D0	Data 3,2,1,0	In/Output
15	NC	No Connection	
16	V_{DD}	Power Supply	
17	GND	Ground	
18	NC	No Connection	
19	XTAL1	1 MHz Clock	Input
20	ADCLK	Address Clock	Input

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on $\overline{RESET}$ Pin with Respect to V_{SS}	–0.6	V_{DD}+1	V	2
Total Power Dissipation		880	mW	
Maximum Allowable Current out of V_{SS}		80	mA	
Maximum Allowable Current into V_{DD}		80	mA	
Maximum Allowable Current into an Input Pin	–600	+600	mA	3
Maximum Allowable Current into an Open-Drain Pin	–600	+600	mA	4
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sunk by Port A		40	mA	
Maximum Allowable Output Current Sourced by Port A		40	mA	
Maximum Allowable Output Current Sunk by Port B		40	mA	
Maximum Allowable Output Current Sourced by Port B		40	mA	

Notes:
1. Applies to all pins except the $\overline{RESET}$ pin and where otherwise noted.
2. There is no input protection diode from pin to V_{DD}.
3. Excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings can cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period can affect device reliability. Total power dissipation should not exceed 880 mW for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})] + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{0L} \times I_{0L})$$

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 7).

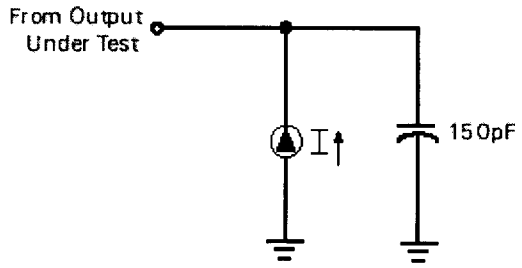


Figure 7. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

		T_A = –40°C to +105°C						
Sym	Parameter	V_{CC} [1]	Min	Max	Typical @ 25°C [2]	Units	Conditions	Notes
I_{CC2}	Standby Current	4.5V		700	250	nA	STOP Mode V_{IN} = 0V, V_{CC}	5
		5.5V		700	250	nA	STOP Mode V_{IN} = 0V, V_{CC}	5

Notes:

1. The V_{CC} voltage specification of 4.5 V and 5.5 V guarantees 5.0 V ±0.5 V.
2. Typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V.
3. All outputs unloaded, I/O pins floating, and all inputs are at V_{CC} or V_{SS} level.
4. CL1 = CL2 = 22 pF.
5. Same as note 3 except inputs at V_{CC}.

RESET PIN OPERATION (Continued)

Table 6. Control and Peripheral Register Reset Values

Register		Bits								
(HEX)	Register Name	7	6	5	4	3	2	1	0	Comments
D4	PortB Input	U	U	U	U	U	U	U	U	Current sample of the input pin following $\overline{\text{RESET}}$
D3	PortA Spec. Func.	0	0	0	0	0	0	0	0	Deactivates all port special functions after $\overline{\text{RESET}}$
D2	PortA Directional Control	0	0	0	0	0	0	0	0	Defines all bits as inputs in PortA after $\overline{\text{RESET}}$
D1	PortA Output	U	U	U	U	U	U	U	U	Output register not affected by $\overline{\text{RESET}}$
D0	PortA Input	U	U	U	U	U	U	U	U	Current sample of the input pin following $\overline{\text{RESET}}$
CF	Reserved									
CE	Reserved									
CD	Reserved									
CC	Reserved									
CB	T3VAL	U	U	U	U	U	U	U	U	
CA	T2VAL	U	U	U	U	U	U	U	U	
C9	T3AR	U	U	U	U	U	U	U	U	
C8	T2AR	U	U	U	U	U	U	U	U	
C7	Reserved									
C6	Reserved									
C5	Reserved									
C4	Reserved									
C3	WDTHI	1	1	1	1	1	1	1	1	
C2	WDTLO	1	1	1	1	1	1	1	1	
C1	TCTLHI	1	1	1	1	1	0	0	0	WDT Enabled in HALT Mode, WDT timeout at maximum value, STOP Mode disabled
C0	TCTLLO	0	0	0	0	0	0	0	0	Standard timer is disabled

Note: *The SMR and WDT flags are set indicating the source of the RESET, as shown below:

D1	D0	Reset Source
0	0	$\overline{\text{RESET}}$ Pin
0	1	SMR Recovery
1	0	WDT Reset
1	1	Reserved

RESET PIN OPERATION (Continued)

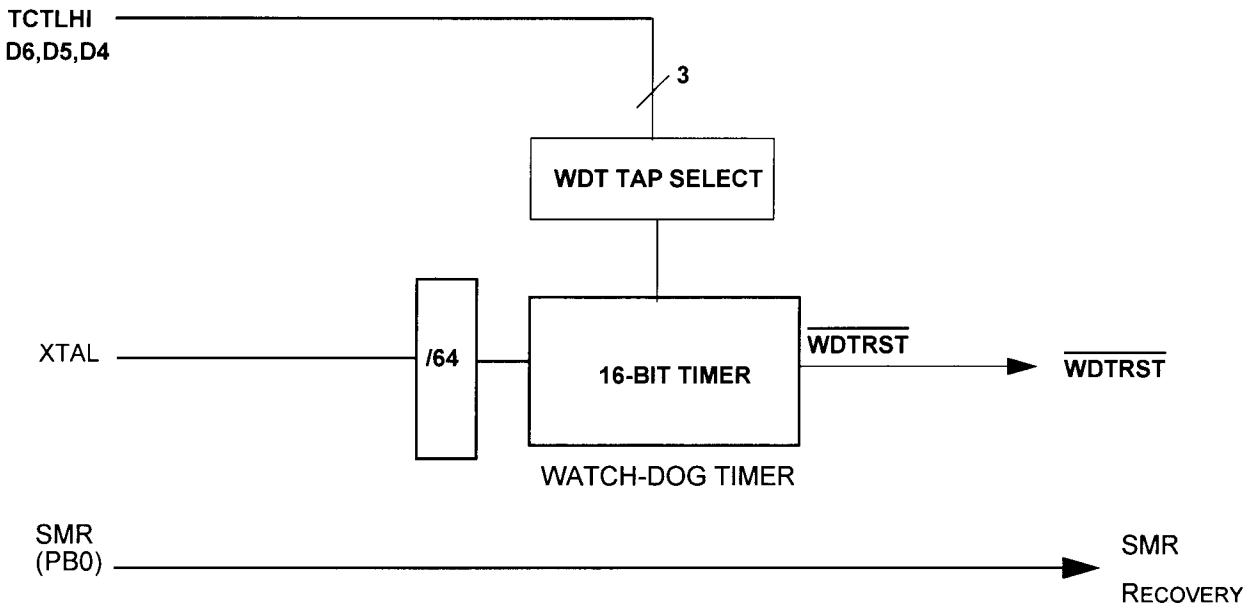


Figure 11. Z8E000 Reset Circuitry with WDT and SMR

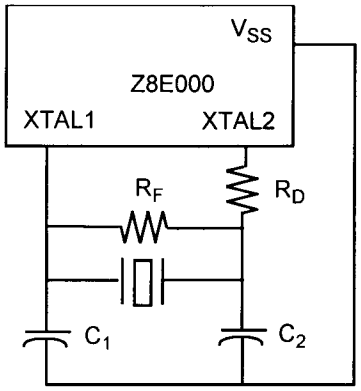


Figure 16. Crystal/Ceramic Resonator Oscillator

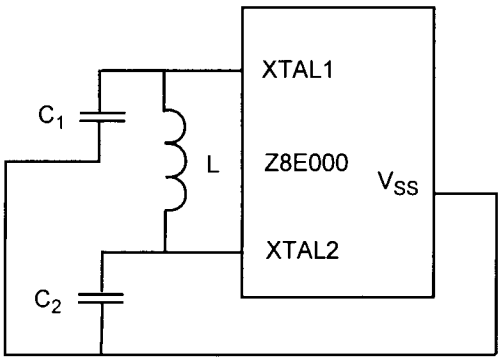


Figure 17. LC Clock

In most cases, the R_D is zero ohms (0Ω), and R_F is infinite. The set value is determined and specified by the crystal/ceramic resonator manufacturer. R_D can be increased to decrease the amount of drive from the oscillator output to the crystal. R_D can also be used as an adjustment to avoid clipping of the oscillator signal to reduce noise. R_F can be used to improve the start-up of the crystal/ceramic resonator. The Z8E000 oscillator already has an internal shunt resistor in parallel to the crystal/ceramic resonator.

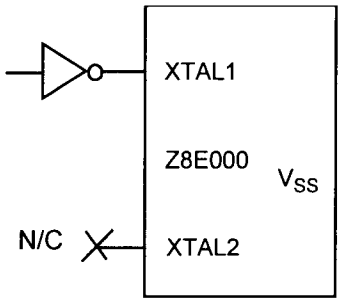


Figure 18. External Clock

Figure 16, Figure 17, and Figure 18 recommend that the load capacitor ground trace connect directly to the V_{SS} (GND) pin of the Z8E000, thereby ensuring that no system noise is injected into the Z8E000 clock. This trace should not be shared with any other components except at the V_{SS} pin of the Z8E000.

Note: A parallel resonant crystal or resonator data sheet will specify a load capacitor value that is the series combination of C_1 and C_2, including all parasitics (PCB and holder).

LC OSCILLATOR

The Z8E000 oscillator can use a LC network to generate a XTAL clock (Figure 18).

The frequency stays stable over V_{CC} and temperature. The oscillation frequency is determined by the equation:

$$\text{Frequency} = \frac{1}{2\pi (LC_T)^{1/2}}$$

where L is the total inductance including parasitics and C_T is the total series capacitance including the parasitics.

Simple series capacitance is calculated using the following equation:

$1/C_T$	$= 1/C_1 + 1/C_2$
If C_1	$= C_2$
$1/C_T$	$= 2\ C_1$
C_1	$= 2\ C_T$

A sample calculation of capacitance C_1 and C_2 for 5.83-MHz frequency and inductance value of 27 uH is illustrated as follows:

$$5.83\ (10\text{^}6) = \frac{1}{2\pi\ [2.7\ (10^{-6})\ C_T]\ 1/2}$$

$$C_T = 27.6\ \text{pf}$$

Thus C_1 = 55.2 pf and C_2 = 55.2 pf.

TIMERS

Two 8-bit timers (T2 and T3), are provided but can only operate in cascade to function as a 16-bit standard timer (Figure 19).

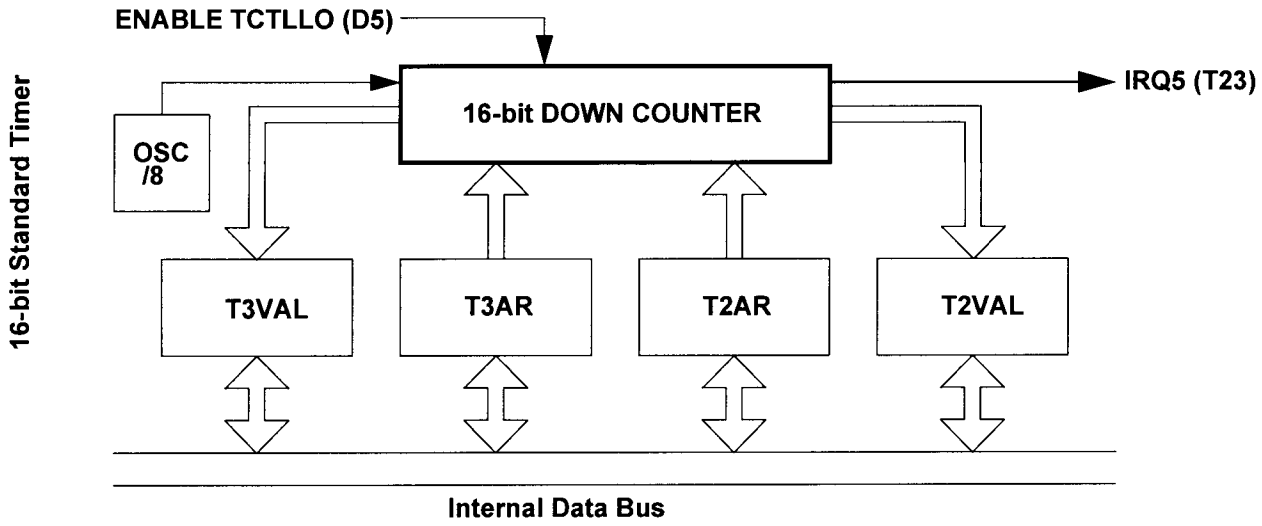
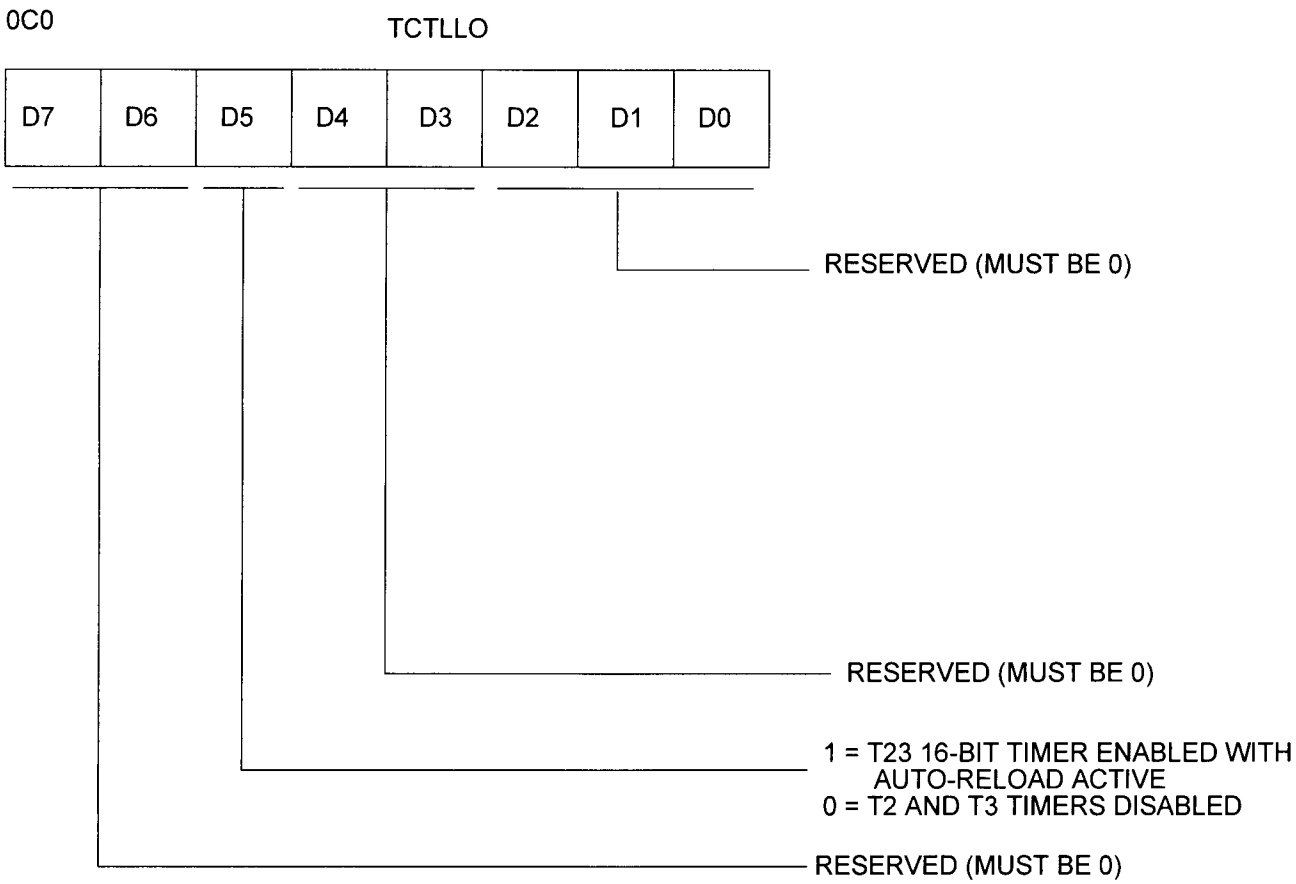


Figure 19. Timer Block Diagram



Note: Timer T23 is a standard 16-bit timer formed by cascading 8-bit timers t3(msb) and t2(lsb).

Figure 20. TCTLLO Register

Each 8-bit timer is equipped with a pair of readable and writable registers, which are both readable and writable. One of the registers is defined to contain the auto-initialization value for the timer, while the second register contains the current value for the timer. When a timer is enabled, the timer will decrement whatever value is currently held in its count register. From that point, the timer continues decrementing until it reaches 0, at which time an interrupt will be generated and the contents of the auto-initialization register are optionally copied into the count value register. If auto-initialization is not enabled, the timer will stop counting upon reaching 0, and control logic will clear the appropriate control register bit to disable the timer. This operation is referred to as a "single-shot". If auto-initialization is enabled, the timer will continue counting from the initialization value. Software should not attempt to use registers that are defined as having timer functionality for any other purpose.

Software is allowed to write to any register at any time, but care should be taken if timer registers are updated while the timer is enabled. If software updates the count value while the timer is in operation, the timer will continue counting based upon the software-updated value. Strange behavior can result if the software update occurred at exactly the point that the timer was reaching 0 to trigger an interrupt and/or reload.

Similarly, if software updates the initialization value register while the timer is active, the next time that the timer reaches 0, it will be initialized using the updated value. Again, strange behavior could result if the initialization value register is being written while the timer is in the process of being initialized. Whether initialization is done with the new or old value is a function of the exact timing of the write operation. In all cases, the Z8E000 will prioritize the software write above that of a decrementer writeback. Howev-

READ/WRITE OPERATIONS

The control for each port is done on a bit-wise basis. All bits are capable of operating as inputs or outputs, depending upon the setting of the port's directional control register. If configured as an input, each bit is provided a Schmitt-trigger. The output of the Schmitt-trigger is latched twice to perform a synchronization function, while the output of the synchronizer is fed to the port input register, which can be read by software.

A write to a port input register has the effect of updating the contents of the input register, but subsequent reads will not necessarily return the same value that was written. If the bit in question is defined as an input, the input register for that bit position will contain the current synchronized input value. Thus, writes to that bit position will be overwritten on the next clock cycle with the newly sampled input data. However, if the particular port bit is programmed as an output, the input register for that bit will retain the software-updated value. The port bits that are programmed as outputs do not sample the value being driven out.

Any bit in either port can be defined as an output by setting the appropriate bit in the directional control register. If such is the case, the value held in the appropriate bit of the port output register is driven directly onto the output pin.

Note: The above result does not necessarily reflect the actual output value. If an external error is holding an output pin either High or Low against the output driver, the software read will return the *required* value, not the actual state caused by the contention. When a bit is defined as an output, the Schmitt-trigger on the input will be disabled to save power.

Updates to the output register will take effect based upon the timing of the internal instruction pipeline; however, this timing is referenced to the rising edge of the clock. The output register can be read at any time, and will return the current output value that is held. No restrictions are placed on the timing of reads and/or writes to any of the port registers with respect to the others, but care should be taken when updating the directional control and special function registers.

When updating a directional control register, the special function register should first be disabled. If this precaution is not taken, spurious events could take place as a result of the change in port I/O status. This precaution is especially important when defining changes in Port B, as the spurious event referred to above could be one or more interrupts. Clearing of the SFR register should be the first step in configuring the port, and setting the SFR register should be the final step in the port configuration process. To ensure deterministic behavior, the SFR register should not be written until the pins are being driven appropriately and all initialization has been completed.

PORT A

Port A is a general-purpose port (Figure 23). Each of its lines can be independently programmed as input or output via the Port A Directional Control Register (PTADIR at 0D2H) as seen in Figure 22. A bit set to a "1" in PTADIR configures the corresponding bit in Port A as an output, while a bit cleared to "0" configures the corresponding bit in Port A as an input.

The input buffers are Schmitt-triggered. Bits programmed as outputs can be individually programmed as either push-pull or open drain by setting the corresponding bit in the Special Function Register (PTASFR, Figure 27.)

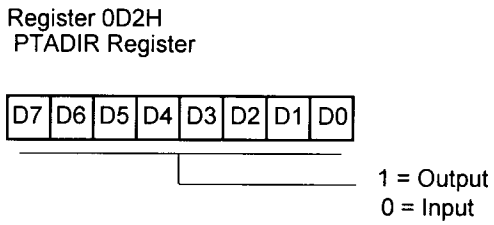


Figure 22. Port A Directional Control Register

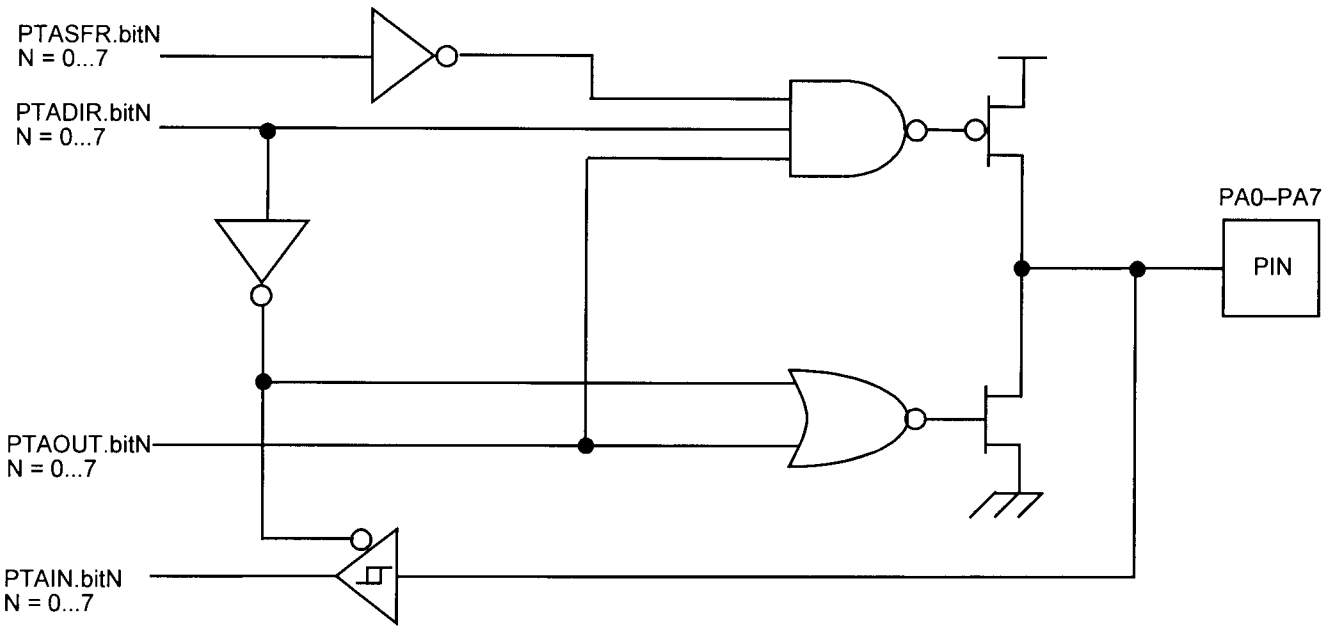


Figure 23. Port A Configuration with Open-Drain Capability and Schmitt-Trigger

PORT A REGISTER DEFINITIONS

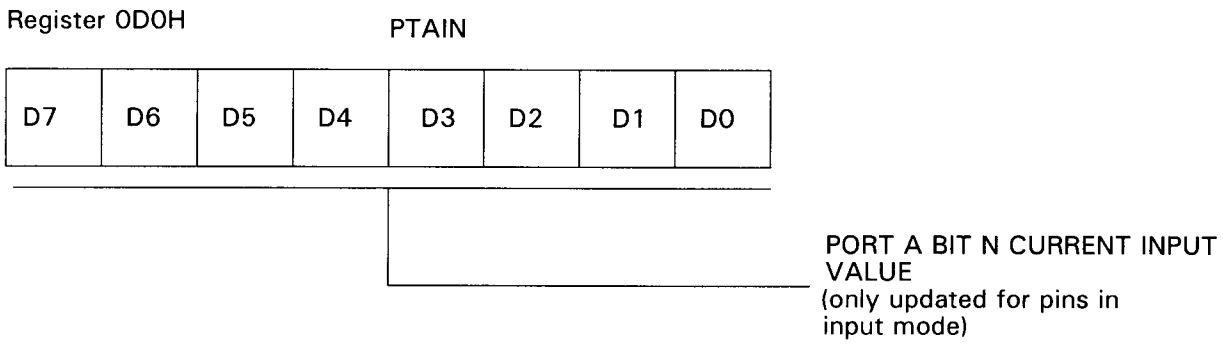


Figure 24. Port A Input Value Register

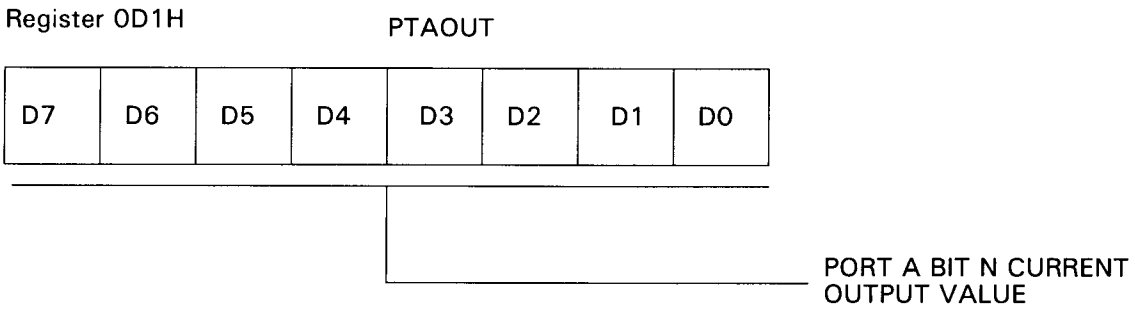


Figure 25. Port A Output Value Register

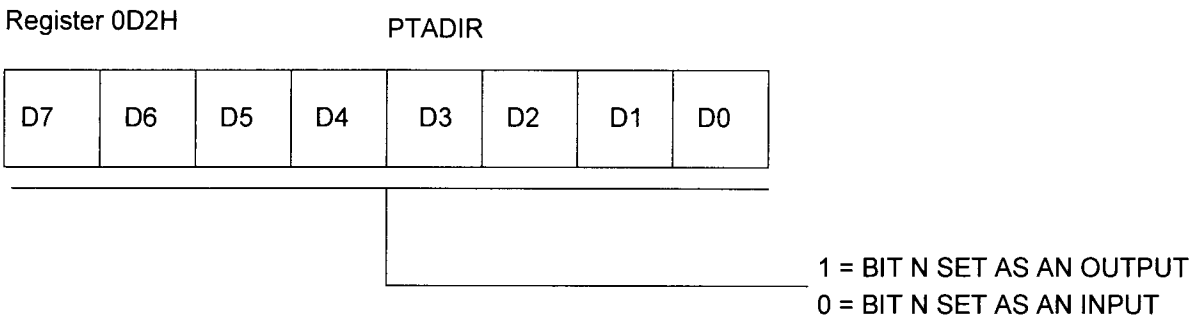


Figure 26. Port A Directional Control Register

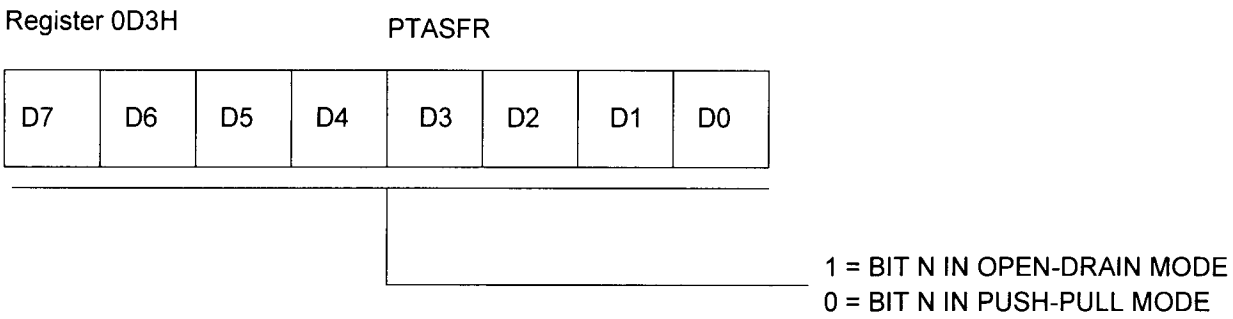


Figure 27. Port A Special Function Register

PORT B

Port B Description

Port B is a 5-bit, bidirectional, CMOS-compatible I/O port. These five I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered. See Figure 29 through Figure 33 for diagrams of all five Port B pins.

In addition to standard input/output capability on all five pins of Port B, each pin provides special functionality as indicated in Table 8:

Table 8. Port B Special Functions

Port Pin	Input Special Function	Output Special Function
PB0	Stop Mode Recovery Input	None
PB1	None	None
PB2	IRQ3	None
PB3	None	None
PB4	IRQ1/IRQ4	None

Special functionality is invoked via the Port B Special Function Register. See Figure 28 for the arrangement and control conventions for this register.

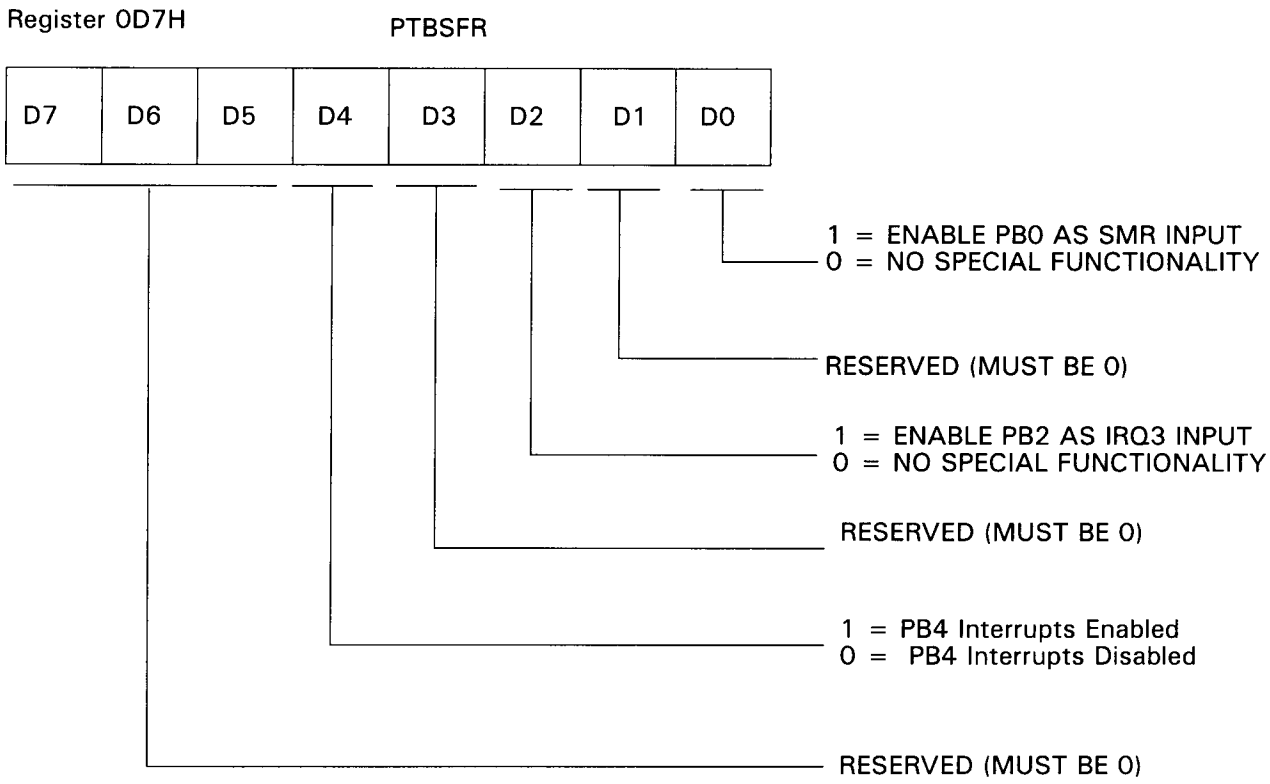


Figure 28. Port B Special Function Register

PORT B—PIN 1 CONFIGURATION

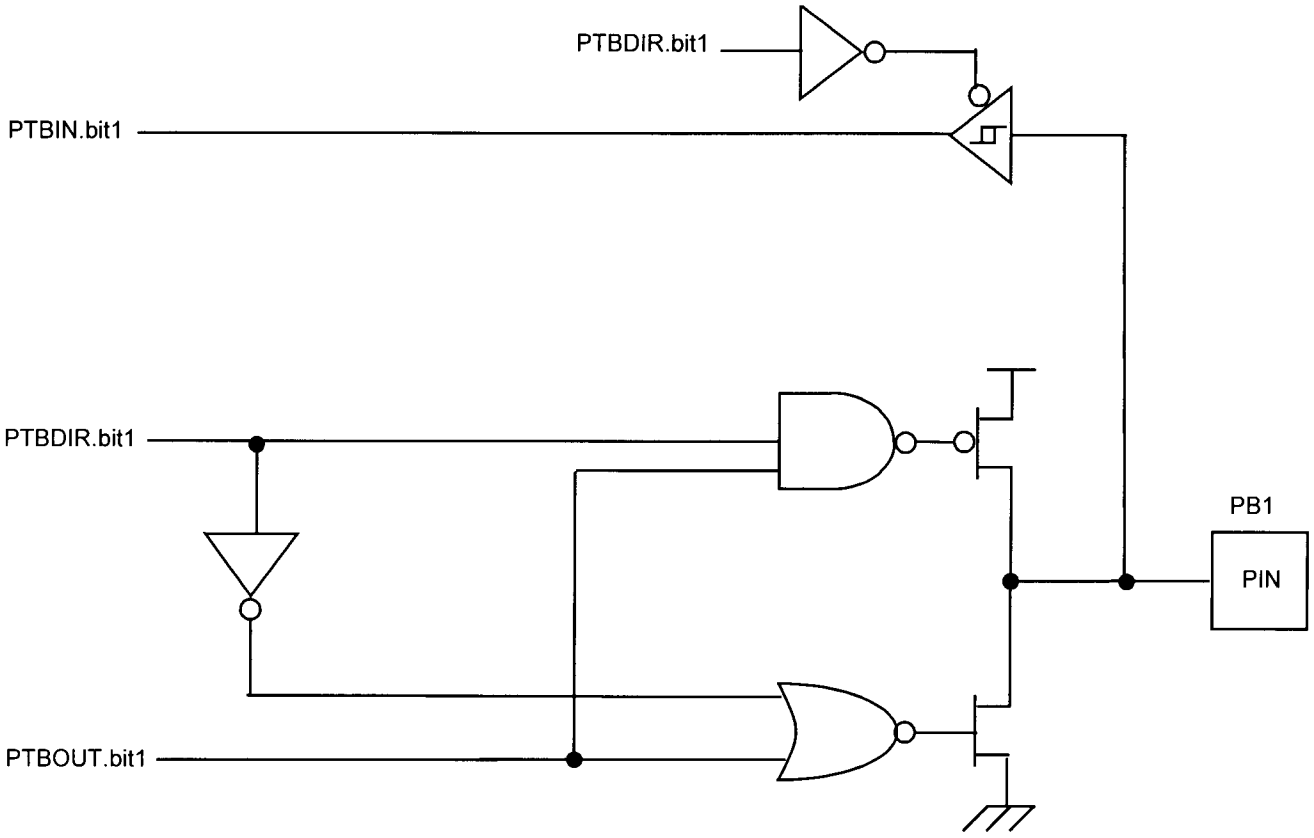


Figure 30. Port B Pin 1 Diagram

PORT B—PIN 2 CONFIGURATION

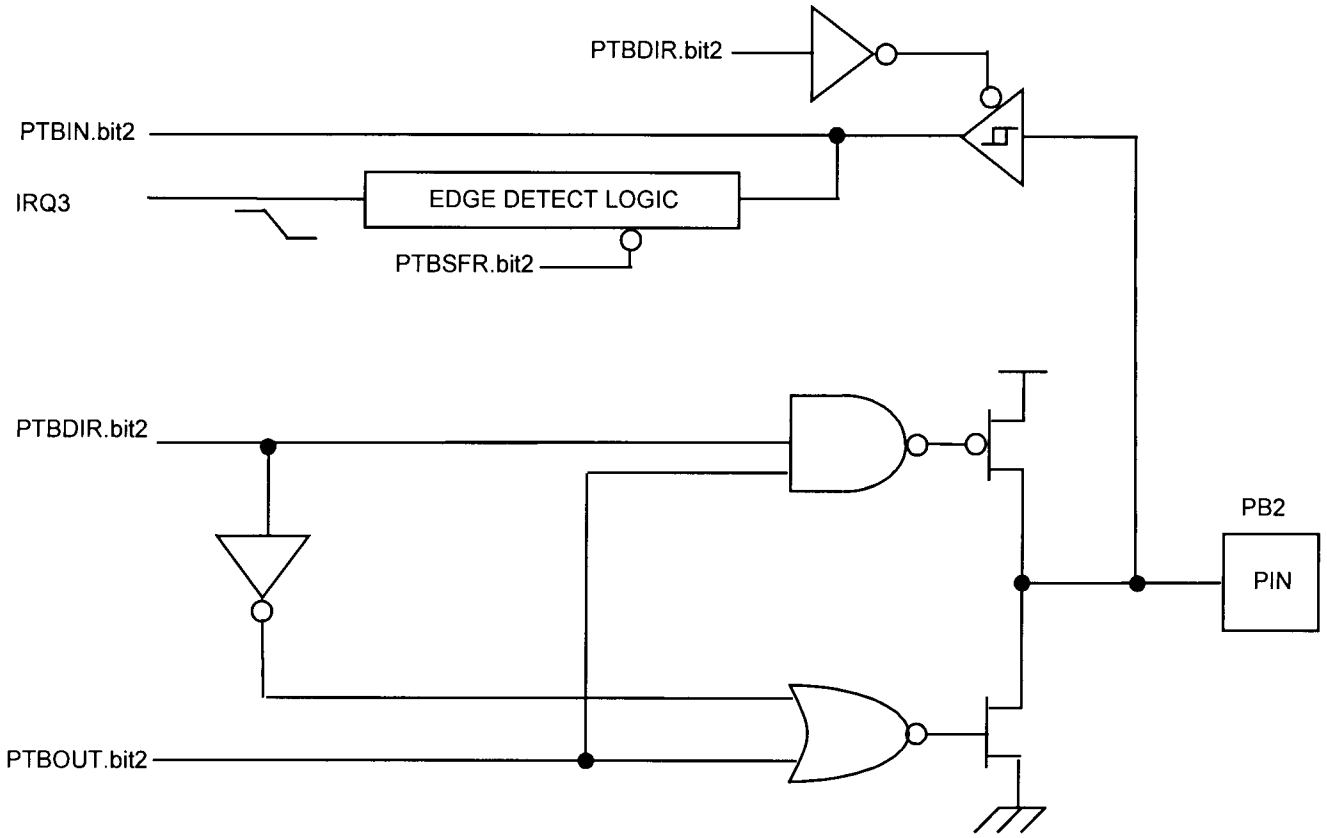


Figure 31. Port B Pin 2 Diagram

ORDERING INFORMATION

Standard Temperature		
18-Pin DIP	**18-Pin SOIC**	**20-Pin SSOP**
Z8E00010PSC	Z8E00010SSC	Z8E00010HSC

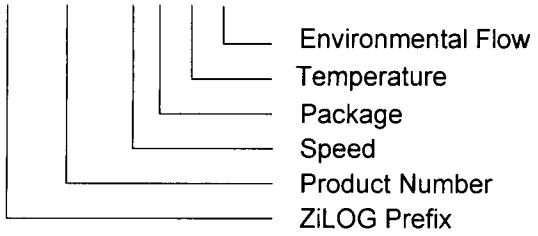
Extended Temperature		
18-Pin DIP	**18-Pin SOIC**	**20-Pin SSOP**
Z8E00010PEC	Z8E00010SEC	Z8E00010HEC

For fast results, contact your local ZiLOG sales office for assistance in ordering the part(s) required.

Codes	
Preferred Package	P = Plastic DIP
Longer Lead Time	S = SOIC
	H = SSOP
Preferred Temperature	S = 0°C to +70°C
	E = –40°C to +105°C
Speed	10 = 10 MHz
Environmental	C = Plastic Standard

Example:

Z 8E000 10 P S C is a Z86E000, 10 MHz, DIP, 0° to +70°C, Plastic Standard Flow



Pre-Characterization Product:

The product represented by this data sheet is newly introduced and ZiLOG has not completed the full characterization of the product. The data sheet states what ZiLOG knows about this product at this time, but additional features or nonconformance with some aspects of the data sheet may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

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