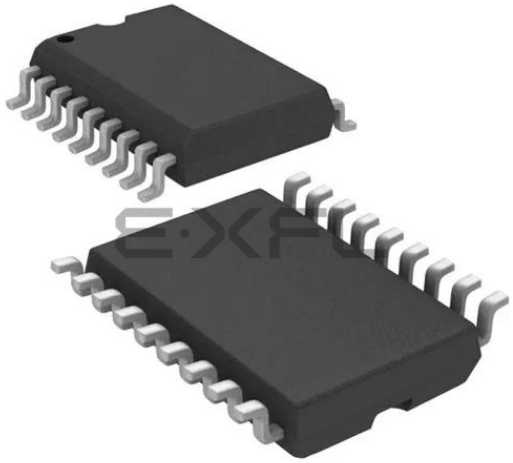

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	WDT
Number of I/O	13
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	32 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8e00010ssc

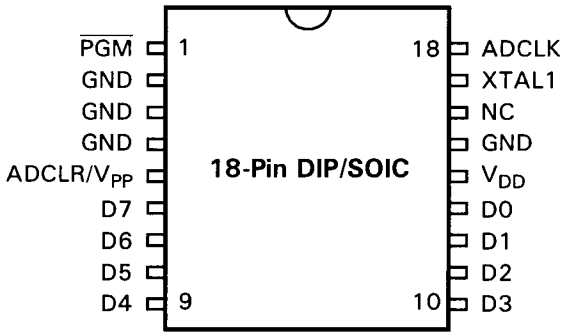


Figure 4. 18-Pin DIP/SOIC Pin Identification; EPROM Programming Mode

Table 2. 18-Pin DIP/SOIC Pin Assignments; EPROM Programmable Mode

EPROM Programming Mode			
Pin #	**Symbol**	**Function**	**Direction**
1	$\overline{PGM}$	Program Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clock/Program Voltage	Input
6–9	D7–D4	Data 7,6,5,4	In/Output
10–13	D3–D0	Data 3,2,1,0	In/Output
14	V_{DD}	Power Supply	
15	GND	Ground	
16	NC	No Connection	
17	XTAL1	1 MHz Clock	Input
18	ADCLK	Address Clock	Input

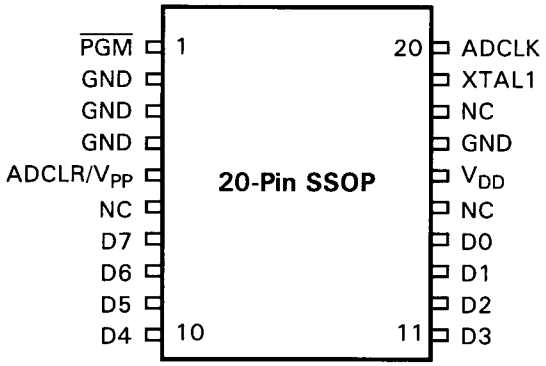


Figure 6. 20-Pin SSOP Pin Identification; EPROM Programming Mode

Table 4. 20-Pin SSOP Pin Assignments; EPROM Programming Mode

EPROM Programming Mode

Pin #	Symbol	Function	Direction
1	$\overline{PGM}$	Program Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clock/Program Voltage	Input
6	NC	No Connection	
7–10	D7–D4	Data 7,6,5,4	In/Output
11–14	D3–D0	Data 3,2,1,0	In/Output
15	NC	No Connection	
16	V_{DD}	Power Supply	
17	GND	Ground	
18	NC	No Connection	
19	XTAL1	1 MHz Clock	Input
20	ADCLK	Address Clock	Input

DC ELECTRICAL CHARACTERISTICS (Continued)

			T_A = –40°C to +105°C					
Sym	Parameter	V_{CC} [1]	Min	Max	Typical @ 25°C [2]	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	4.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL} = +4.0 mA	
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	
V_{OL2}	Output Low Voltage	4.5V		1.2	0.5	V	I_{OL} = +12 mA,	
		5.5V		1.2	0.5	V	I_{OL} = +12 mA,	
V_{RH}	Reset Input High Voltage	4.5V	0.5V_{CC}	V_{CC}	1.1	V		
		5.5V	0.5V_{CC}	V_{CC}	2.2	V		
I_{IL}	Input Leakage	4.5V	–1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V	–1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	4.5V	–18	–180	–112	mA		
		5.5V	–18	–180	–112	mA		
I_{CC}	Supply Current	4.5V		7.0	4.0	mA	@ 10 MHz	3,4
		5.5V		7.0	4.0	mA	@ 10 MHz	3,4
I_{CC1}	Standby Current	4.5V		2.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 10 MHz	3,4
		5.5V		2.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 10 MHz	3,4

		T_A = –40°C to +105°C						
Sym	Parameter	V_{CC} [1]	Min	Max	Typical @ 25°C [2]	Units	Conditions	Notes
I_{CC2}	Standby Current	4.5V		700	250	nA	STOP Mode V_{IN} = 0V, V_{CC}	5
		5.5V		700	250	nA	STOP Mode V_{IN} = 0V, V_{CC}	5

Notes:

1. The V_{CC} voltage specification of 4.5 V and 5.5 V guarantees 5.0 V ±0.5 V.
2. Typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V.
3. All outputs unloaded, I/O pins floating, and all inputs are at V_{CC} or V_{SS} level.
4. CL1 = CL2 = 22 pF.
5. Same as note 3 except inputs at V_{CC}.

AC ELECTRICAL CHARACTERISTICS

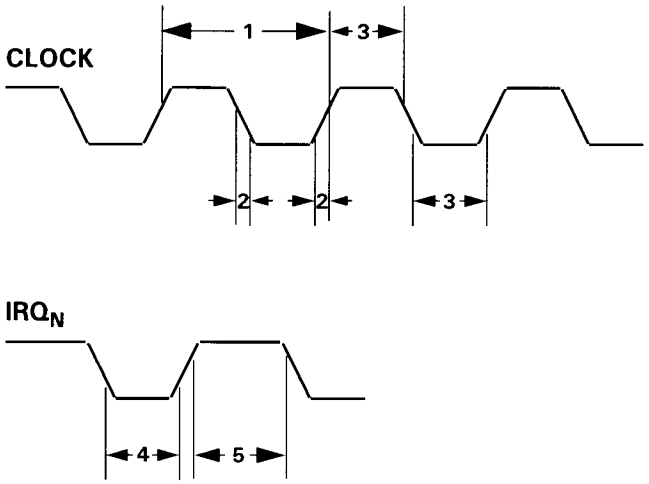


Figure 8. AC Electrical Timing Diagram

Table 5. Additional Timings

				T_A = –40°C to +105°C @ 10 MHz			
No	**Symbol**	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	3.5V	100	DC	ns	2
			5.5V	100	DC	ns	2
2	TrC,TfC	Clock Input Rise and Fall Times	3.5V		15	ns	2
			5.5V		15	ns	2
3	TwC	Input Clock Width	3.5V	50		ns	2
			5.5V	50		ns	2
4	TwIL	Int. Request Input Low Time	3.5V	70		ns	2
			5.5V	70		ns	2
5	TwIH	Int. Request Input High Time	3.5V	5TpC			2
			5.5V	5TpC			2
6	Twsm	STOP Mode Recovery Width Spec.	3.5V	12		ns	
			5.5V	12		ns	
7	Tost	Oscillator Start-Up Time	3.5V		5TpC		
			5.5V		5TpC		

Notes:
1. The V_{DD} voltage specification of 3.5V guarantees 3.5V. The V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

RESET PIN OPERATION (Continued)

Table 6. Control and Peripheral Register Reset Values

Register		Bits								
(HEX)	Register Name	7	6	5	4	3	2	1	0	Comments
D4	PortB Input	U	U	U	U	U	U	U	U	Current sample of the input pin following $\overline{\text{RESET}}$
D3	PortA Spec. Func.	0	0	0	0	0	0	0	0	Deactivates all port special functions after $\overline{\text{RESET}}$
D2	PortA Directional Control	0	0	0	0	0	0	0	0	Defines all bits as inputs in PortA after $\overline{\text{RESET}}$
D1	PortA Output	U	U	U	U	U	U	U	U	Output register not affected by $\overline{\text{RESET}}$
D0	PortA Input	U	U	U	U	U	U	U	U	Current sample of the input pin following $\overline{\text{RESET}}$
CF	Reserved									
CE	Reserved									
CD	Reserved									
CC	Reserved									
CB	T3VAL	U	U	U	U	U	U	U	U	
CA	T2VAL	U	U	U	U	U	U	U	U	
C9	T3AR	U	U	U	U	U	U	U	U	
C8	T2AR	U	U	U	U	U	U	U	U	
C7	Reserved									
C6	Reserved									
C5	Reserved									
C4	Reserved									
C3	WDTHI	1	1	1	1	1	1	1	1	
C2	WDTLO	1	1	1	1	1	1	1	1	
C1	TCTLHI	1	1	1	1	1	0	0	0	WDT Enabled in HALT Mode, WDT timeout at maximum value, STOP Mode disabled
C0	TCTLLO	0	0	0	0	0	0	0	0	Standard timer is disabled

Note: *The SMR and WDT flags are set indicating the source of the RESET, as shown below:

D1	D0	Reset Source
0	0	$\overline{\text{RESET}}$ Pin
0	1	SMR Recovery
1	0	WDT Reset
1	1	Reserved

RESET PIN OPERATION (Continued)

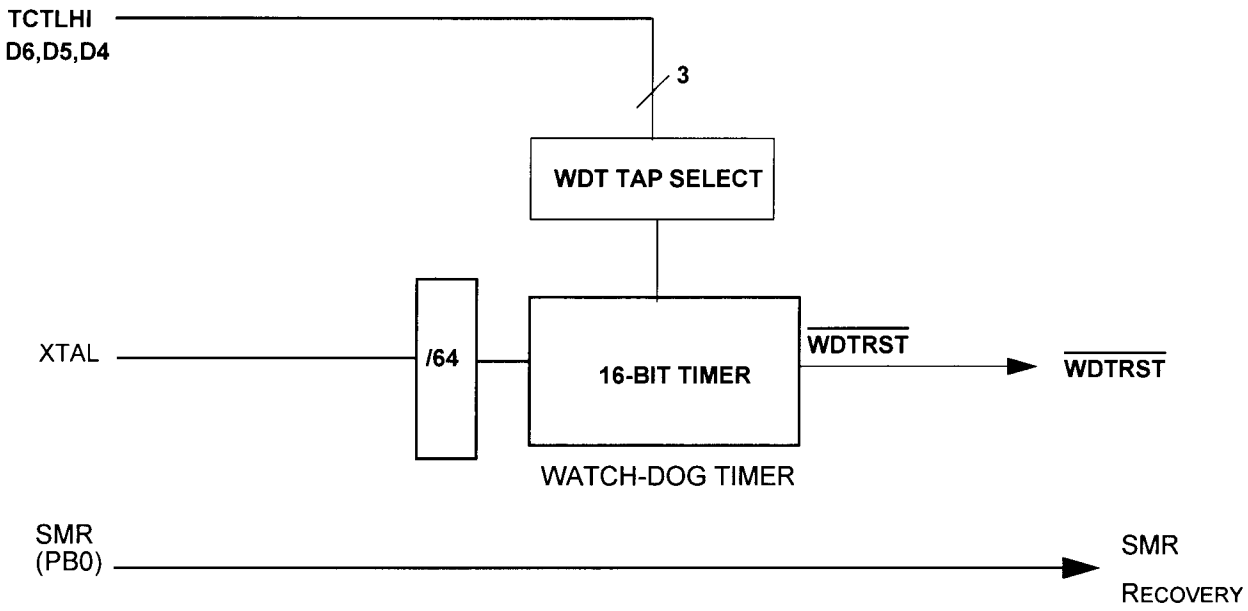


Figure 11. Z8E000 Reset Circuitry with WDT and SMR

Z8E000 WATCH-DOG TIMER (WDT) (Continued)

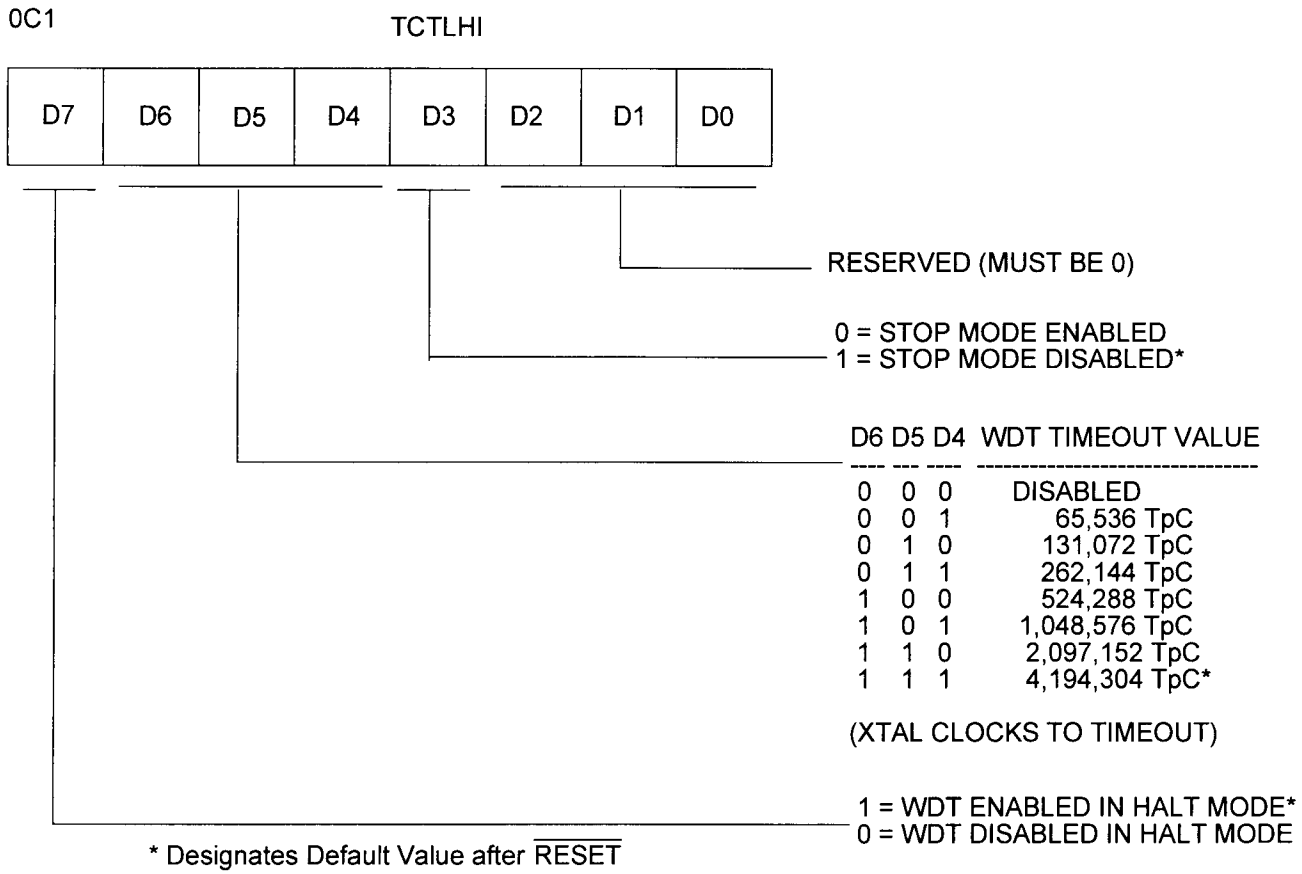


Figure 12. Z8E000 TCTLHI Register for Control of WDT

Note: The WDT can only be disabled via software if the first instruction out of RESET performs this function. Logic within the Z8E000 will detect that it is in the process of executing the first instruction after the part leaves RESET. During the execution of this instruction, the upper five bits of the TCTLHI register can be written. After this first instruction, hardware will not allow the upper five bits of this register to be written.

The TCTLHI bits for control of the WDT are described below:

WDT Time Select (D6, D5, D4). Bits 6, 5, and 4 determine the time-out period. Table 7 indicates the range of timeout values that can be obtained. The default values of D6, D5, and D4 are all 1, thus setting the WDT to its maximum timeout period when coming out of RESET.

Table 7. Time-Out Period of the WDT

D6	D5	D4	Crystal Clocks to Timeout	Time-Out Using a10 MHz Crystal
0	0	0	Disabled	Disabled
0	0	1	65,536 TpC	6.55 ms
0	1	0	131,072 TpC	13.11 ms
0	1	1	262,144 TpC	26.21 ms
1	0	0	524,288 TpC	52.43 ms
1	0	1	1,048,576 TpC	104.86 ms
1	1	0	2,097,152 TpC	209.72 ms
1	1	1	4,194,304 TpC	419.43 ms

Notes:
TpC = XTAL clock cycle.
The default on reset is D6 = D5 = D4 = 1.

WDT During HALT (D7). This bit determines whether or not the WDT is active during HALT Mode. A "1" indicates active during HALT. A "0" prevents the WDT from resetting the part while halted.Coming out of reset, the WDT will be enabled during HALT Mode.

STOP MODE (D3). Coming out of $\overline{\text{RESET}}$, the Z8E000 will have the STOP Mode disabled. If an application requires use of STOP Mode, bit D3 must be cleared immediately upon leaving $\overline{\text{RESET}}$. If bit D3 is set, the STOP instruction will execute as a NOP. If bit D3 is cleared, the STOP instruction will enter Stop Mode. Whenever the Z8E000 wakes up after having been in STOP Mode, the STOP Mode will be disabled once again.

Bits 2, 1 and 0. These bits are reserved and must be 0.

POWER-DOWN MODES

In addition to the standard RUN mode, the Z8E000 MCU supports two Power-Down modes to minimize device current consumption. The two modes supported are HALT and STOP.

HALT MODE OPERATION

The HALT Mode suspends instruction execution and turns off the internal CPU clock. The on-chip oscillator circuit remains active, so the internal clock continues to run and is applied to the timers and interrupt logic.

To enter the HALT Mode, the Z8E000 only requires a HALT instruction. It is NOT necessary to execute a NOP instruction immediately before the HALT instruction.

```
7F    HALT    ; enter HALT Mode
```

The HALT Mode can be exited by servicing an interrupt (either externally or internally). Upon completion of the interrupt service routine, the user program continues from the instruction after HALT.

The HALT Mode can also be exited via a $\overline{\text{RESET}}$ activation or a Watch-Dog Timer (WDT) timeout. In these cases, program execution will restart at the reset address 0020H.

STOP MODE OPERATION

The STOP Mode provides the lowest possible device stand-by current. This instruction turns off the on-chip oscillator and internal system clock.

To enter the STOP Mode, the Z8E000 only requires a STOP instruction. It is NOT necessary to execute a NOP instruction immediately before the STOP instruction.

```
6F    STOP    ;enter STOP Mode
```

The STOP Mode is exited by any one of the following resets: $\overline{\text{RESET}}$ pin or a STOP-Mode Recovery source. Upon reset generation, the processor will always restart the application program at address 0020H, thereby setting the STOP Mode Flag. Reading the STOP-Mode flag does not clear it. The user must clear the STOP-Mode flag with software.

Note: Failure to clear the STOP-Mode flag can result in undefined behavior.

The Z8E000 provides a dedicated STOP Mode Recovery (SMR) circuit. In this case, a low level applied to input pin PB0 will trigger a SMR. To use this mode, pin PB0 (I/O Port B, bit 0) must be configured as an input before the STOP Mode is entered. The low level on PB0 must be held for a minimum pulse width T_{WSM}, in addition to any oscillator startup time. Program execution starts at address 0020H after PBO is raised back to a high level.

Notes: Use of the PB0 input for the STOP mode recovery does not initialize the control registers.

The STOP Mode current (I_{CC2}) will be minimized when:

- V_{CC} is at the low end of the device's operating range.
- Output current sourcing is minimized.
- All inputs (digital and analog) are at the Low or High rail voltages.

CLOCK

The Z8E000 MCU derives its timing from on-board clock circuitry connected to pins XTAL1 and XTAL2. The clock circuitry consists of an oscillator, a glitch filter, a divide-by-two shaping circuit, a divide-by-four shaping circuit, and a divide-by-eight shaping circuit. Figure 13 illustrates the clock circuitry. The oscillator's input is XTAL1 and its output is XTAL2. The clock can be driven by a crystal, a ceramic resonator, LC clock, or an external clock source.

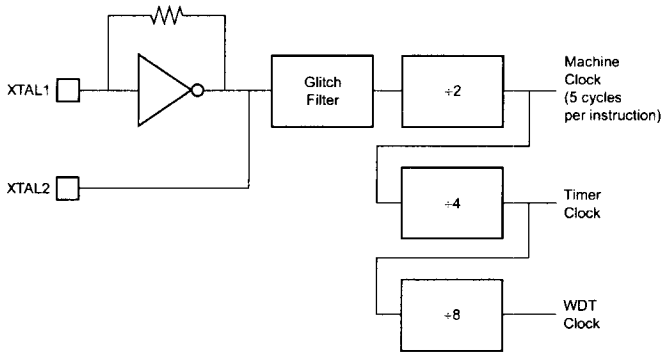


Figure 13. Z8E000 Clock Circuit

OSCILLATOR OPERATION

The Z8E000 MCU uses a Pierce oscillator with an internal feedback circuit (Figure 14). The advantages of this circuit are low cost, large output signal, low power level in the crystal, stability with respect to V_{CC} and temperature, and low impedances (not disturbed by stray effects).

One draw back to the oscillator is the requirement for high gain in the amplifier to compensate for feedback path losses. The oscillator amplifies its own noise at start-up until it settles at the frequency that satisfies the gain/phase requirements ($A \times B = 1$, where $A = V_o/V_i$ is the gain of the amplifier and $B = V_i/V_o$ is the gain of the feedback element). The total phase shift around the loop is forced to zero (360 degrees). VIN must be in phase with itself. The amplifier/inverter thereby provides a 180-degree phase shift, forcing the feedback element to provide the other 180 degrees of phase shift.

R_I is a resistive component placed from output to input of the amplifier. The purpose of this feedback is to bias the amplifier in its linear region and to provide the start-up transition.

Capacitor C_2, combined with the amplifier output resistance, provides a small phase shift. It will also provide some attenuation of overtones.

Capacitor C_1, combined with the crystal resistance, provides additional phase shift.

C_1 and C_2 can affect the start-up time if they increase dramatically in size. As C_1 and C_2 increase, the start-up time increases until the oscillator reaches a point where it does not start up any more.

It is recommended for fast and reliable oscillator start-up (over the manufacturing process range) that the load capacitors be sized as low as possible without resulting in overtone operation.

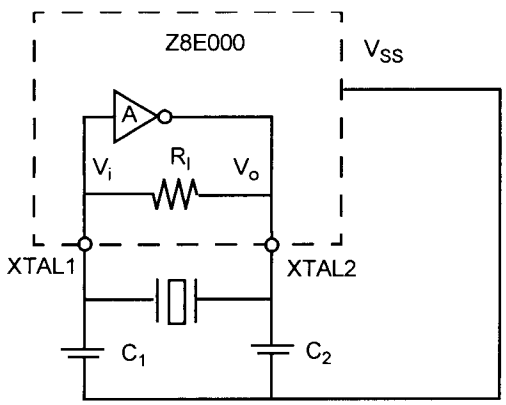


Figure 14. Pierce Oscillator with Internal Feedback Circuit

Layout

Traces connecting crystal, caps, and the Z8E000 oscillator pins should be as short and wide as possible, to reduce parasitic inductance and resistance. The components (caps, crystal, resistors) should be placed as close as possible to the oscillator pins of the Z8E000.

The traces from the oscillator pins of the IC and the ground side of the lead caps should be guarded from all other traces (clock, V_{CC}, address/data lines, system ground) to reduce cross talk and noise injection. Guarding is usually accomplished by keeping other traces and system ground trace planes away from the oscillator circuit, and by placing a Z8E000 device V_{SS} ground ring around the traces/components. The ground side of the oscillator lead caps should be connected to a single trace of the Z8E000 V_{SS} (GND) pin. The ground side of these caps should not be shared with any other system ground trace or components except at the Z8E000 device V_{SS} pin. The objective is to prevent differential system ground noise injection into the oscillator (Figure 15).

Indications of an Unreliable Design

There are two major indicators that are used in working designs to determine their reliability over full lot and temperature variations. They are:

Start-up Time. If start-up time is excessive, or varies widely from unit to unit, there is probably a gain problem. C_1 and C_2 require reduction if the amplifier gain is not adequate at frequency, or crystal R's are too large.

Output Level. The signal at the amplifier output should swing from ground to V_{CC} to indicate adequate gain in the amplifier. As the oscillator starts up, the signal amplitude grows until clipping occurs. At this point, the loop gain is effectively reduced to unity, and constant oscillation is achieved. A signal of less than 2.5 volts peak-to-peak is an indication that low gain can be a problem. Either C_1 or C_2 should be made smaller or a low-resistance crystal should be used.

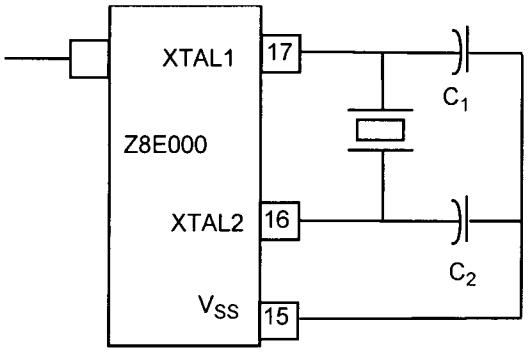
Circuit Board Design Rules

The following circuit board design rules are suggested:

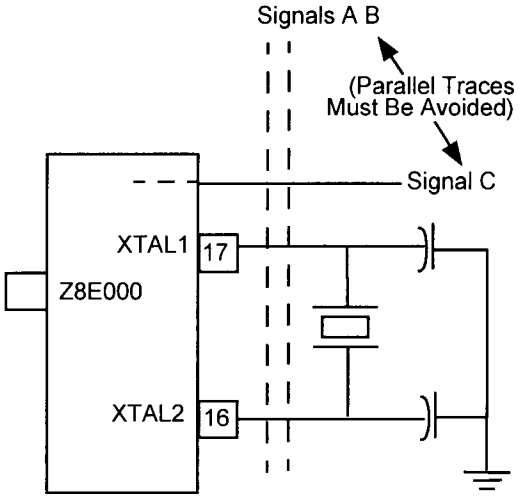
- To prevent induced noise, the crystal and load capacitors should be physically located as close to the Z8E000 as possible.
- Signal lines should not run parallel to the clock oscillator inputs. In particular, the crystal input circuitry and the internal system clock output should be separated as much as possible.

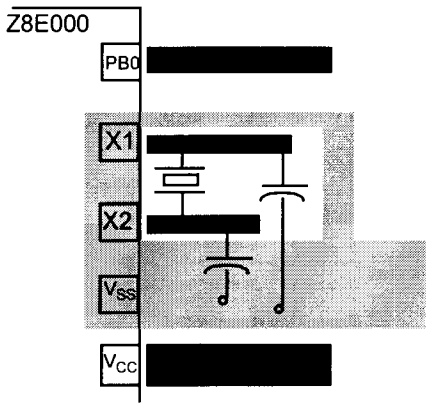
OSCILLATOR OPERATION (Continued)

- V_{CC} power lines should be separated from the clock oscillator input circuitry.
- Resistance between XTAL1 or XTAL2 and the other pins should be greater than 10 MΩ.



Clock Generator Circuit





Board Design Example
(Top View)

Figure 15. Circuit Board Design Rules

Crystals and Resonators

Crystals and ceramic resonators (Figure 16) should have the following characteristics to ensure proper oscillator operation:

Crystal Cut	AT (crystal only)
Mode	Parallel, Fundamental Mode
Crystal Capacitance	<7pF
Load Capacitance	10pF < CL < 220 pF, 15 typical
Resistance	100 ohms max

Depending on operation frequency, the oscillator can require the addition of capacitors C_1 and C_2 (shown in Figure 17 and Figure 18). The capacitance values are dependent on the manufacturer's crystal specifications.

LC OSCILLATOR

The Z8E000 oscillator can use a LC network to generate a XTAL clock (Figure 18).

The frequency stays stable over V_{CC} and temperature. The oscillation frequency is determined by the equation:

$$\text{Frequency} = \frac{1}{2\pi (LC_T)^{1/2}}$$

where L is the total inductance including parasitics and C_T is the total series capacitance including the parasitics.

Simple series capacitance is calculated using the following equation:

$1/C_T$	$= 1/C_1 + 1/C_2$
If C_1	$= C_2$
$1/C_T$	$= 2\ C_1$
C_1	$= 2\ C_T$

A sample calculation of capacitance C_1 and C_2 for 5.83-MHz frequency and inductance value of 27 uH is illustrated as follows:

$$5.83\ (10\text{^}6) = \frac{1}{2\pi\ [2.7\ (10^{-6})\ C_T]\ 1/2}$$

$$C_T = 27.6\ \text{pf}$$

Thus C_1 = 55.2 pf and C_2 = 55.2 pf.

TIMERS

Two 8-bit timers (T2 and T3), are provided but can only operate in cascade to function as a 16-bit standard timer (Figure 19).

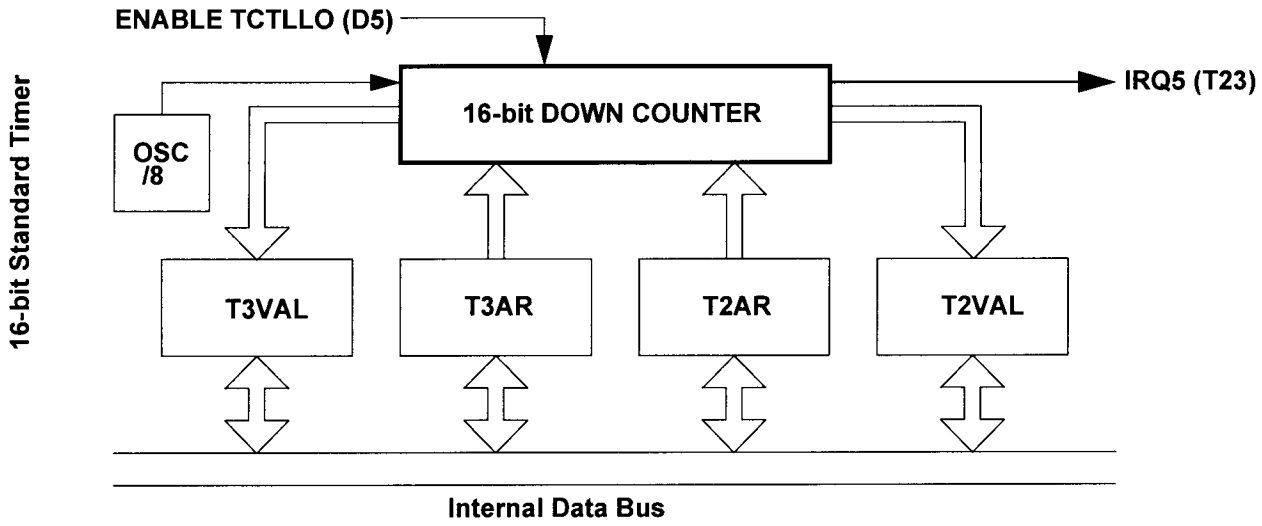
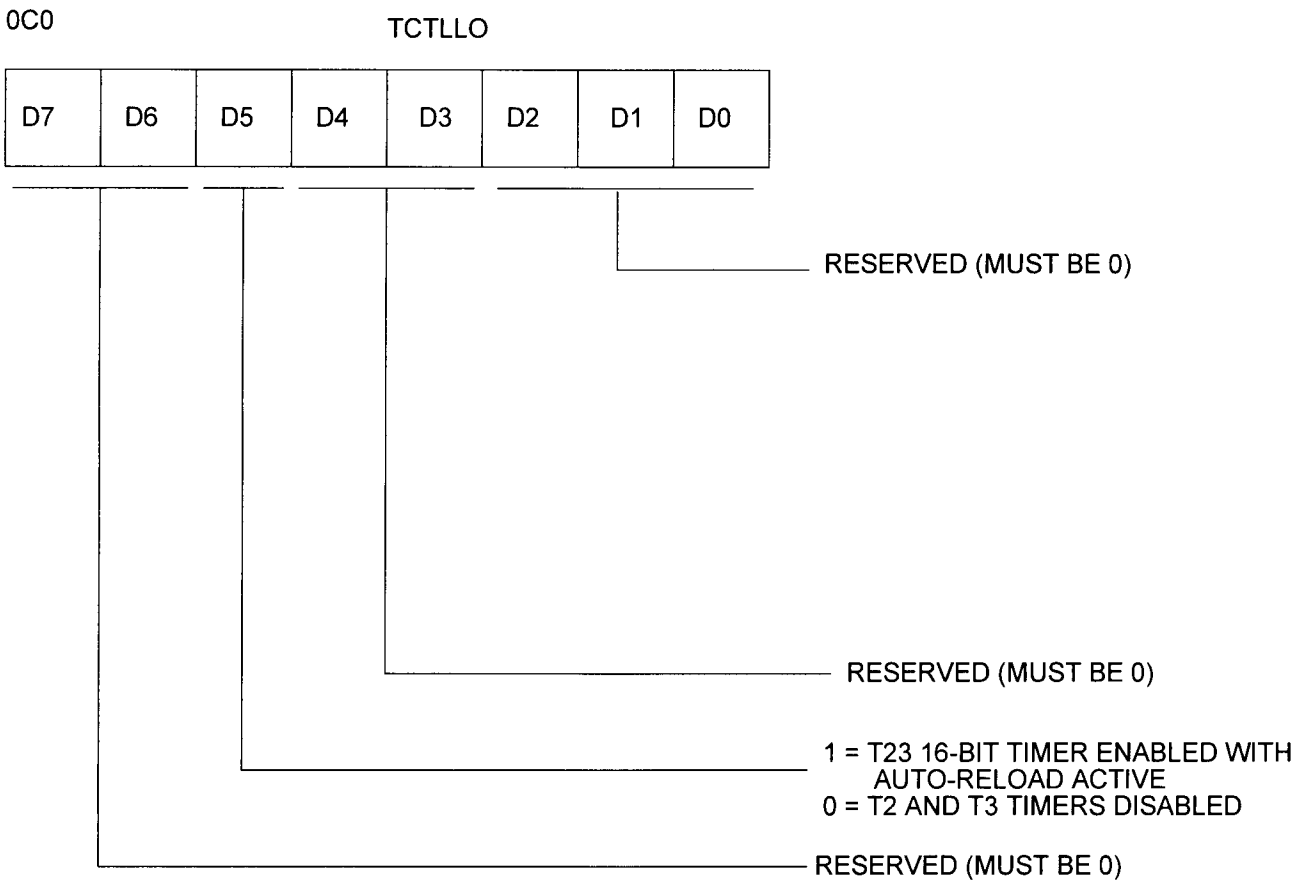


Figure 19. Timer Block Diagram



Note: Timer T23 is a standard 16-bit timer formed by cascading 8-bit timers t3(msb) and t2(lsb).

Figure 20. TCTLLO Register

Each 8-bit timer is equipped with a pair of readable and writable registers, which are both readable and writable. One of the registers is defined to contain the auto-initialization value for the timer, while the second register contains the current value for the timer. When a timer is enabled, the timer will decrement whatever value is currently held in its count register. From that point, the timer continues decrementing until it reaches 0, at which time an interrupt will be generated and the contents of the auto-initialization register are optionally copied into the count value register. If auto-initialization is not enabled, the timer will stop counting upon reaching 0, and control logic will clear the appropriate control register bit to disable the timer. This operation is referred to as a "single-shot". If auto-initialization is enabled, the timer will continue counting from the initialization value. Software should not attempt to use registers that are defined as having timer functionality for any other purpose.

Software is allowed to write to any register at any time, but care should be taken if timer registers are updated while the timer is enabled. If software updates the count value while the timer is in operation, the timer will continue counting based upon the software-updated value. Strange behavior can result if the software update occurred at exactly the point that the timer was reaching 0 to trigger an interrupt and/or reload.

Similarly, if software updates the initialization value register while the timer is active, the next time that the timer reaches 0, it will be initialized using the updated value. Again, strange behavior could result if the initialization value register is being written while the timer is in the process of being initialized. Whether initialization is done with the new or old value is a function of the exact timing of the write operation. In all cases, the Z8E000 will prioritize the software write above that of a decrementer writeback. Howev-

READ/WRITE OPERATIONS

The control for each port is done on a bit-wise basis. All bits are capable of operating as inputs or outputs, depending upon the setting of the port's directional control register. If configured as an input, each bit is provided a Schmitt-trigger. The output of the Schmitt-trigger is latched twice to perform a synchronization function, while the output of the synchronizer is fed to the port input register, which can be read by software.

A write to a port input register has the effect of updating the contents of the input register, but subsequent reads will not necessarily return the same value that was written. If the bit in question is defined as an input, the input register for that bit position will contain the current synchronized input value. Thus, writes to that bit position will be overwritten on the next clock cycle with the newly sampled input data. However, if the particular port bit is programmed as an output, the input register for that bit will retain the software-updated value. The port bits that are programmed as outputs do not sample the value being driven out.

Any bit in either port can be defined as an output by setting the appropriate bit in the directional control register. If such is the case, the value held in the appropriate bit of the port output register is driven directly onto the output pin.

Note: The above result does not necessarily reflect the actual output value. If an external error is holding an output pin either High or Low against the output driver, the software read will return the *required* value, not the actual state caused by the contention. When a bit is defined as an output, the Schmitt-trigger on the input will be disabled to save power.

Updates to the output register will take effect based upon the timing of the internal instruction pipeline; however, this timing is referenced to the rising edge of the clock. The output register can be read at any time, and will return the current output value that is held. No restrictions are placed on the timing of reads and/or writes to any of the port registers with respect to the others, but care should be taken when updating the directional control and special function registers.

When updating a directional control register, the special function register should first be disabled. If this precaution is not taken, spurious events could take place as a result of the change in port I/O status. This precaution is especially important when defining changes in Port B, as the spurious event referred to above could be one or more interrupts. Clearing of the SFR register should be the first step in configuring the port, and setting the SFR register should be the final step in the port configuration process. To ensure deterministic behavior, the SFR register should not be written until the pins are being driven appropriately and all initialization has been completed.

PORT B—PIN 1 CONFIGURATION

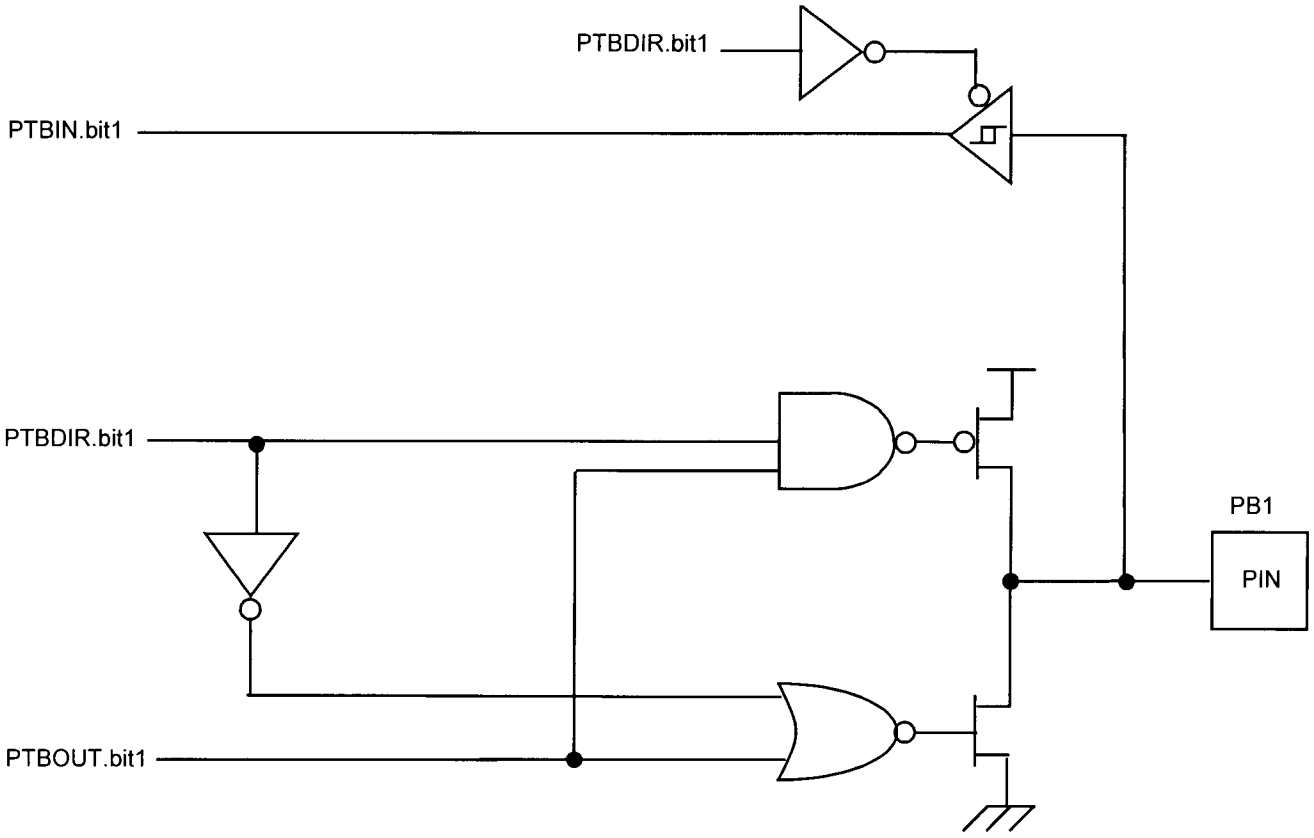


Figure 30. Port B Pin 1 Diagram

PORT B—PIN 2 CONFIGURATION

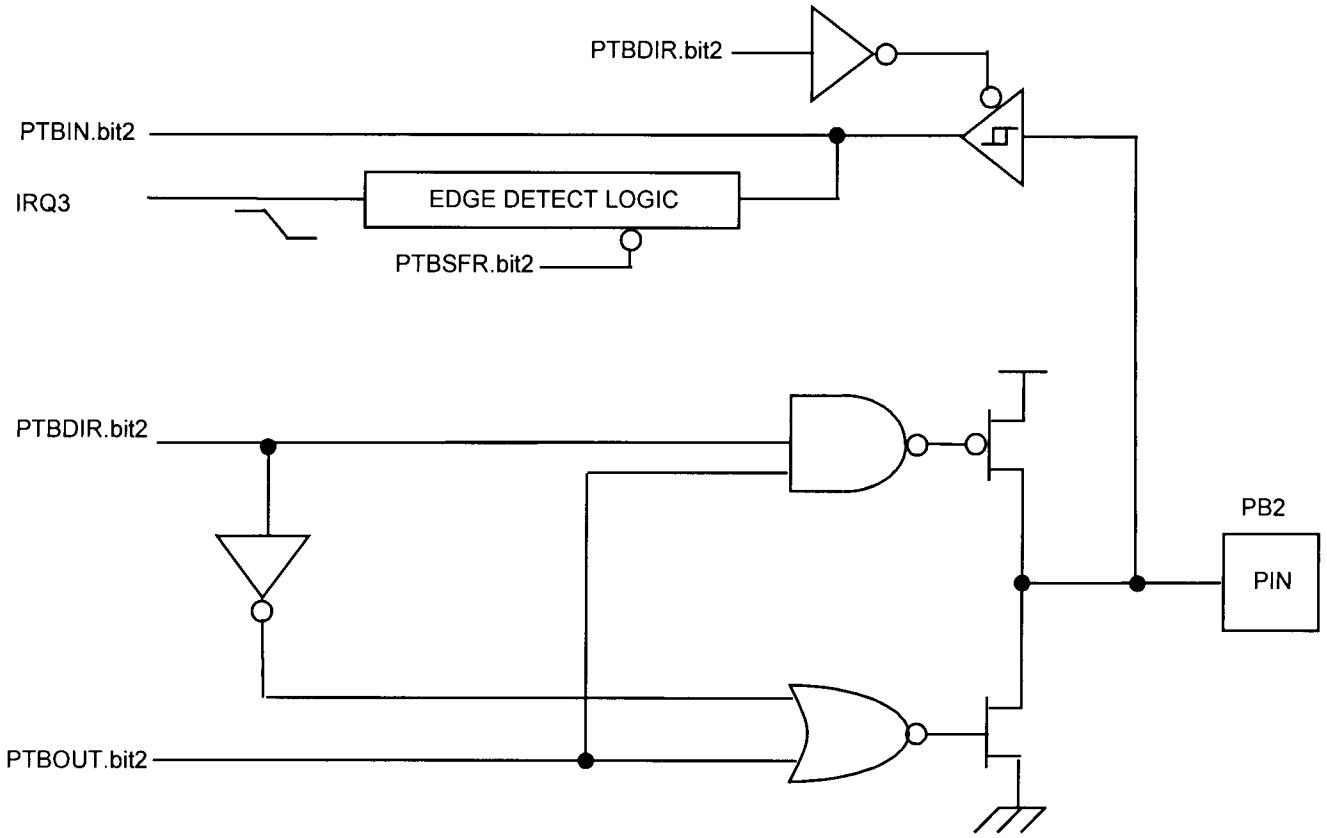


Figure 31. Port B Pin 2 Diagram

PORT B—PINS 3 AND 4 CONFIGURATION

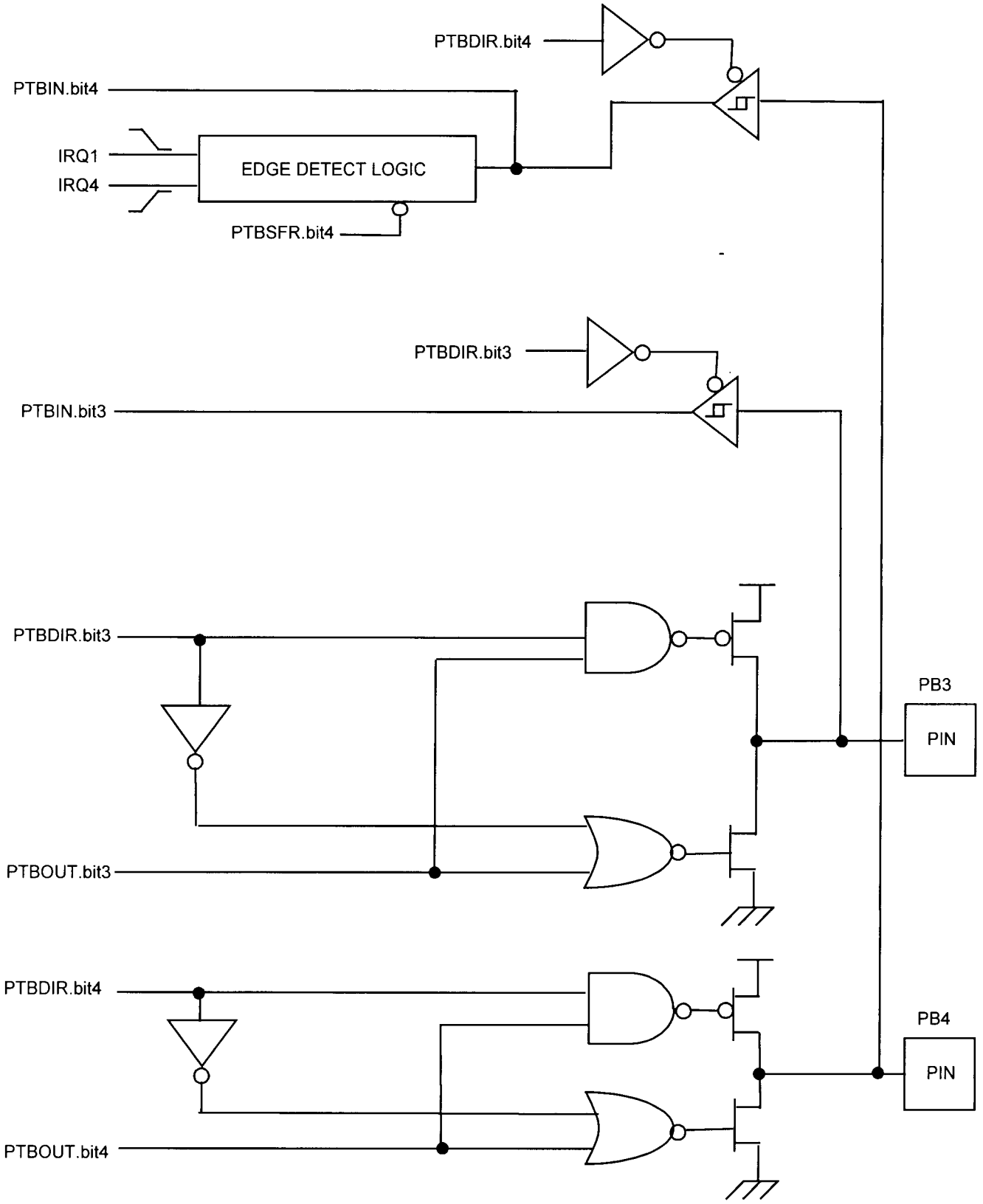


Figure 32. Port B Pins 3 and 4 Diagram

PORT B CONTROL REGISTER DEFINITIONS (Continued)

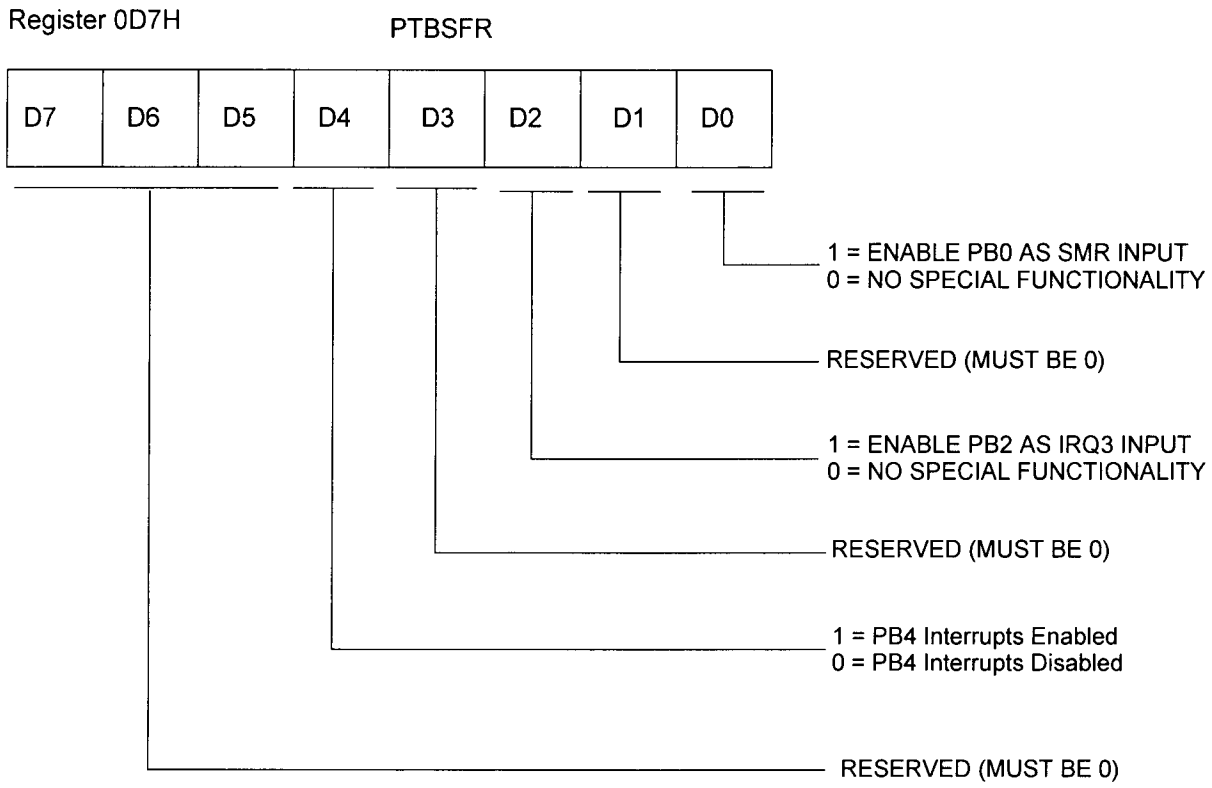


Figure 36. Port B Special Function Register

ORDERING INFORMATION

Standard Temperature		
18-Pin DIP	**18-Pin SOIC**	**20-Pin SSOP**
Z8E00010PSC	Z8E00010SSC	Z8E00010HSC

Extended Temperature		
18-Pin DIP	**18-Pin SOIC**	**20-Pin SSOP**
Z8E00010PEC	Z8E00010SEC	Z8E00010HEC

For fast results, contact your local ZiLOG sales office for assistance in ordering the part(s) required.

Codes	
Preferred Package	P = Plastic DIP
Longer Lead Time	S = SOIC
	H = SSOP
Preferred Temperature	S = 0°C to +70°C
	E = –40°C to +105°C
Speed	10 = 10 MHz
Environmental	C = Plastic Standard

Example:

Z 8E000 10 P S C is a Z86E000, 10 MHz, DIP, 0° to +70°C, Plastic Standard Flow