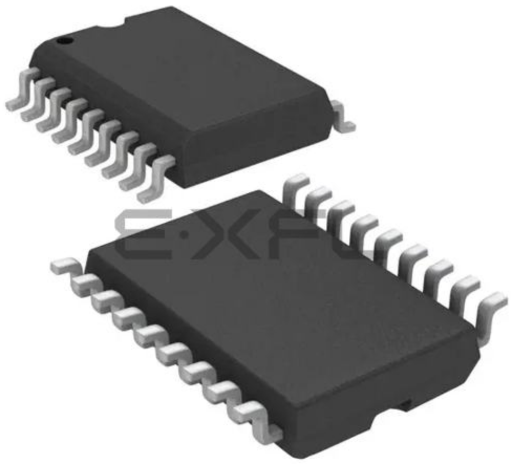

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	WDT
Number of I/O	13
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	32 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8e00010ssc00tr

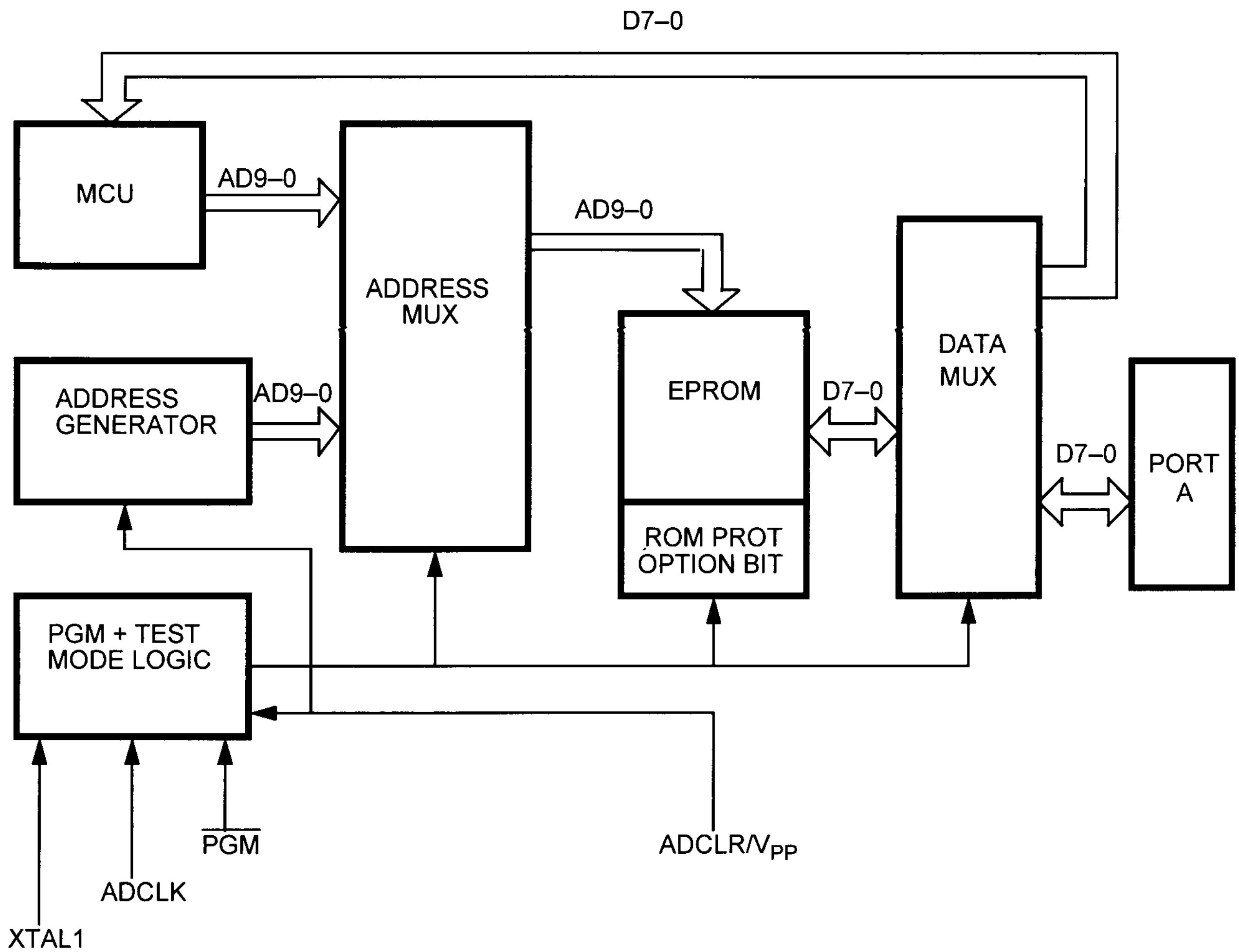


Figure 2. EPROM Programming Mode Block Diagram

PIN DESCRIPTION

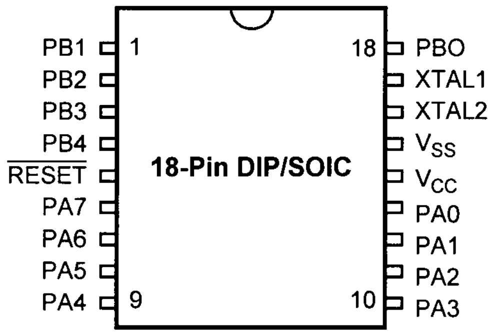


Figure 3. 18-Pin DIP/SOIC Pin Identification

Table 1. 18-Pin DIP/SOIC Pin Assignments

Standard Mode			
Pin #	**Symbol**	**Function**	**Direction**
1–4	PB1–PB4	Port B, Pins 1,2,3,4	In/Output
5	$\overline{\text{RESET}}$	Reset	Input
6–9	PA7–PA4	Port A, Pins 7,6,5,4	In/Output
10–13	PA3–PA0	Port A, Pins 3,2,1,0	In/Output
14	V_{CC}	Power Supply	
15	V_{SS}	Ground	
16	XTAL2	Crystal Oscillator Clock	Output
17	XTAL1	Crystal Oscillator Clock	Input
18	PB0	Port B, Pin 0	In/Output

PIN DESCRIPTION (Continued)

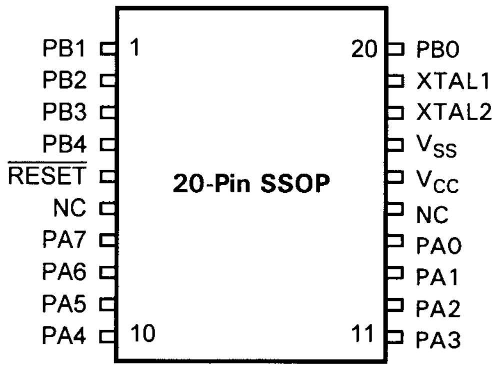


Figure 5. 20-Pin SSOP Pin Identification

Table 3. 20-Pin SSOP Pin Assignments

Standard Mode

Pin #	Symbol	Function	Direction
1–4	PB1–PB4	Port B, Pins 1,2,3,4	In/Output
5	$\overline{RESET}$	Reset	Input
6	NC	No Connection	
7–10	PA7–PA4	Port A, Pins 7,6,5,4	In/Output
11–14	PA3–PA0	Port A, Pins 3,2,1,0	In/Output
15	NC	No Connection	
16	V_{CC}	Power Supply	
17	V_{SS}	Ground	
18	XTAL2	Crystal Oscillator Clock	Output
19	XTAL1	Crystal Oscillator Clock	Input
20	PB0	Port B, Pin 0	In/Output

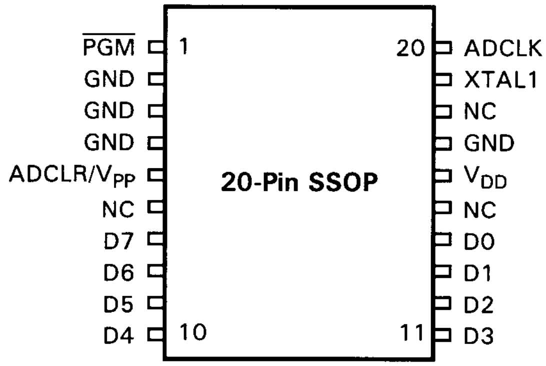


Figure 6. 20-Pin SSOP Pin Identification; EPROM Programming Mode

Table 4. 20-Pin SSOP Pin Assignments; EPROM Programming Mode

EPROM Programming Mode			
Pin #	**Symbol**	**Function**	**Direction**
1	$\overline{PGM}$	Program Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clock/Program Voltage	Input
6	NC	No Connection	
7–10	D7–D4	Data 7,6,5,4	In/Output
11–14	D3–D0	Data 3,2,1,0	In/Output
15	NC	No Connection	
16	V_{DD}	Power Supply	
17	GND	Ground	
18	NC	No Connection	
19	XTAL1	1 MHz Clock	Input
20	ADCLK	Address Clock	Input

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on $\overline{RESET}$ Pin with Respect to V_{SS}	–0.6	V_{DD}+1	V	2
Total Power Dissipation		880	mW	
Maximum Allowable Current out of V_{SS}		80	mA	
Maximum Allowable Current into V_{DD}		80	mA	
Maximum Allowable Current into an Input Pin	–600	+600	mA	3
Maximum Allowable Current into an Open-Drain Pin	–600	+600	mA	4
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sunk by Port A		40	mA	
Maximum Allowable Output Current Sourced by Port A		40	mA	
Maximum Allowable Output Current Sunk by Port B		40	mA	
Maximum Allowable Output Current Sourced by Port B		40	mA	

Notes:
1. Applies to all pins except the $\overline{RESET}$ pin and where otherwise noted.
2. There is no input protection diode from pin to V_{DD}.
3. Excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings can cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period can affect device reliability. Total power dissipation should not exceed 880 mW for the package. Power dissipation is calculated as follows:

Total Power Dissipation $= V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})]$
$+ \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}]$
$+ \text{sum of } (V_{0L} \times I_{0L})$

			T_A = –40°C to +105°C					
Sym	Parameter	V_{CC}[1]	Min	Max	Typical @ 25°C[2]	Units	Conditions	Notes
I_{CC2}	Standby Current	4.5V		700	250	nA	STOP Mode V_{IN} = 0V, V_{CC}	5
		5.5V		700	250	nA	STOP Mode V_{IN} = 0V, V_{CC}	5

Notes:
1. The V_{CC} voltage specification of 4.5 V and 5.5 V guarantees 5.0 V ±0.5 V.
2. Typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V.
3. All outputs unloaded, I/O pins floating, and all inputs are at V_{CC} or V_{SS} level.
4. CL1 = CL2 = 22 pF.
5. Same as note 3 except inputs at V_{CC}.

AC ELECTRICAL CHARACTERISTICS

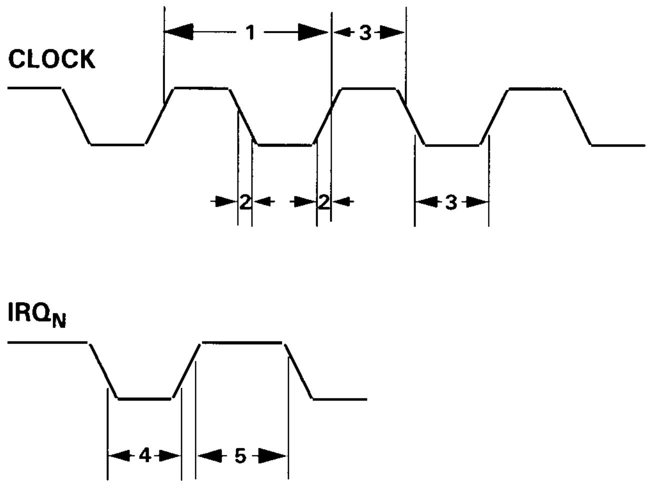


Figure 8. AC Electrical Timing Diagram

Table 5. Additional Timings

No	Symbol	Parameter	V_{CC}[1]	Min (T_A = –40°C to +105°C @ 10 MHz)	Max	Units	Notes
1	TpC	Input Clock Period	3.5V	100	DC	ns	2
			5.5V	100	DC	ns	2
2	TrC,TfC	Clock Input Rise and Fall Times	3.5V		15	ns	2
			5.5V		15	ns	2
3	TwC	Input Clock Width	3.5V	50		ns	2
			5.5V	50		ns	2
4	TwIL	Int. Request Input Low Time	3.5V	70		ns	2
			5.5V	70		ns	2
5	TwIH	Int. Request Input High Time	3.5V	5TpC			2
			5.5V	5TpC			2
6	Twsm	STOP Mode Recovery Width Spec.	3.5V	12		ns	
			5.5V	12		ns	
7	Tost	Oscillator Start-Up Time	3.5V		5TpC		
			5.5V		5TpC		

Notes:
1. The V_{DD} voltage specification of 3.5V guarantees 3.5V. The V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

RESET PIN OPERATION (Continued)

Table 6. Control and Peripheral Register Reset Values

Register (HEX)	Register Name	7	6	5	4	3	2	1	0	Comments
D4	PortB Input	U	U	U	U	U	U	U	U	Current sample of the input pin following RESET
D3	PortA Spec. Func.	0	0	0	0	0	0	0	0	Deactivates all port special functions after RESET
D2	PortA Directional Control	0	0	0	0	0	0	0	0	Defines all bits as inputs in PortA after RESET
D1	PortA Output	U	U	U	U	U	U	U	U	Output register not affected by RESET
D0	PortA Input	U	U	U	U	U	U	U	U	Current sample of the input pin following RESET
CF	Reserved									
CE	Reserved									
CD	Reserved									
CC	Reserved									
CB	T3VAL	U	U	U	U	U	U	U	U	
CA	T2VAL	U	U	U	U	U	U	U	U	
C9	T3AR	U	U	U	U	U	U	U	U	
C8	T2AR	U	U	U	U	U	U	U	U	
C7	Reserved									
C6	Reserved									
C5	Reserved									
C4	Reserved									
C3	WDTHI	1	1	1	1	1	1	1	1	
C2	WDTLO	1	1	1	1	1	1	1	1	
C1	TCTLHI	1	1	1	1	1	0	0	0	WDT Enabled in HALT Mode, WDT timeout at maximum value, STOP Mode disabled
C0	TCTLLO	0	0	0	0	0	0	0	0	Standard timer is disabled

Note: *The SMR and WDT flags are set indicating the source of the RESET, as shown below:

D1	D0	Reset Source
0	0	RESET Pin
0	1	SMR Recovery
1	0	WDT Reset
1	1	Reserved

RESET PIN OPERATION (Continued)

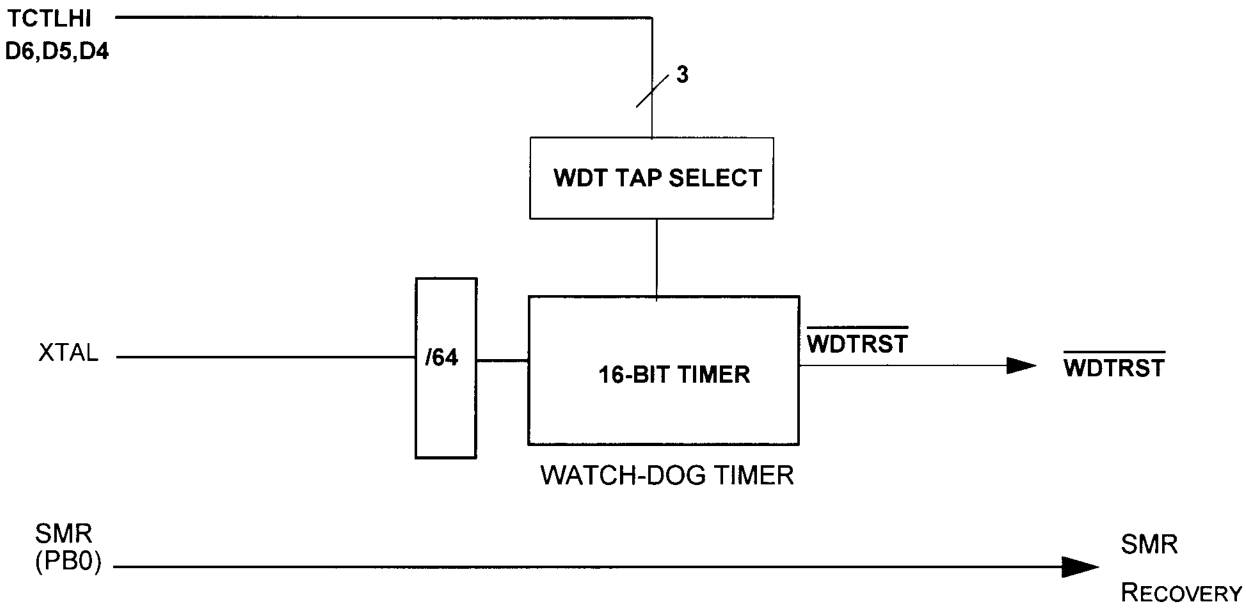


Figure 11. Z8E000 Reset Circuitry with WDT and SMR

OSCILLATOR OPERATION

The Z8E000 MCU uses a Pierce oscillator with an internal feedback circuit (Figure 14). The advantages of this circuit are low cost, large output signal, low power level in the crystal, stability with respect to V_{CC} and temperature, and low impedances (not disturbed by stray effects).

One draw back to the oscillator is the requirement for high gain in the amplifier to compensate for feedback path losses. The oscillator amplifies its own noise at start-up until it settles at the frequency that satisfies the gain/phase requirements ($A \times B = 1$, where $A = V_o/V_i$ is the gain of the amplifier and $B = V_i/V_o$ is the gain of the feedback element). The total phase shift around the loop is forced to zero (360 degrees). VIN must be in phase with itself. The amplifier/inverter thereby provides a 180-degree phase shift, forcing the feedback element to provide the other 180 degrees of phase shift.

R_I is a resistive component placed from output to input of the amplifier. The purpose of this feedback is to bias the amplifier in its linear region and to provide the start-up transition.

Capacitor C_2, combined with the amplifier output resistance, provides a small phase shift. It will also provide some attenuation of overtones.

Capacitor C_1, combined with the crystal resistance, provides additional phase shift.

C_1 and C_2 can affect the start-up time if they increase dramatically in size. As C_1 and C_2 increase, the start-up time increases until the oscillator reaches a point where it does not start up any more.

It is recommended for fast and reliable oscillator start-up (over the manufacturing process range) that the load capacitors be sized as low as possible without resulting in overtone operation.

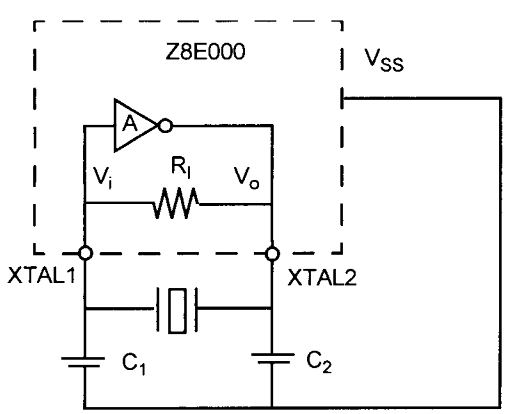


Figure 14. Pierce Oscillator with Internal Feedback Circuit

Layout

Traces connecting crystal, caps, and the Z8E000 oscillator pins should be as short and wide as possible, to reduce parasitic inductance and resistance. The components (caps, crystal, resistors) should be placed as close as possible to the oscillator pins of the Z8E000.

The traces from the oscillator pins of the IC and the ground side of the lead caps should be guarded from all other traces (clock, V_{CC}, address/data lines, system ground) to reduce cross talk and noise injection. Guarding is usually accomplished by keeping other traces and system ground trace planes away from the oscillator circuit, and by placing a Z8E000 device V_{SS} ground ring around the traces/components. The ground side of the oscillator lead caps should be connected to a single trace of the Z8E000 V_{SS} (GND) pin. The ground side of these caps should not be shared with any other system ground trace or components except at the Z8E000 device V_{SS} pin. The objective is to prevent differential system ground noise injection into the oscillator (Figure 15).

Indications of an Unreliable Design

There are two major indicators that are used in working designs to determine their reliability over full lot and temperature variations. They are:

Start-up Time. If start-up time is excessive, or varies widely from unit to unit, there is probably a gain problem. C_1 and C_2 require reduction if the amplifier gain is not adequate at frequency, or crystal R's are too large.

Output Level. The signal at the amplifier output should swing from ground to V_{CC} to indicate adequate gain in the amplifier. As the oscillator starts up, the signal amplitude grows until clipping occurs. At this point, the loop gain is effectively reduced to unity, and constant oscillation is achieved. A signal of less than 2.5 volts peak-to-peak is an indication that low gain can be a problem. Either C_1 or C_2 should be made smaller or a low-resistance crystal should be used.

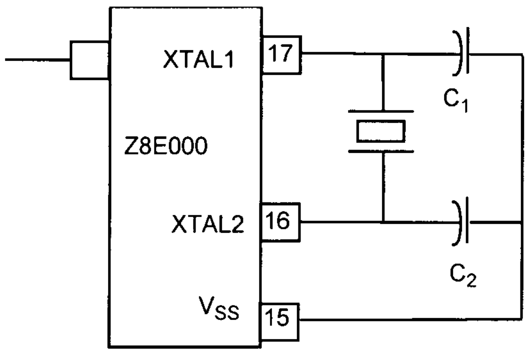
Circuit Board Design Rules

The following circuit board design rules are suggested:

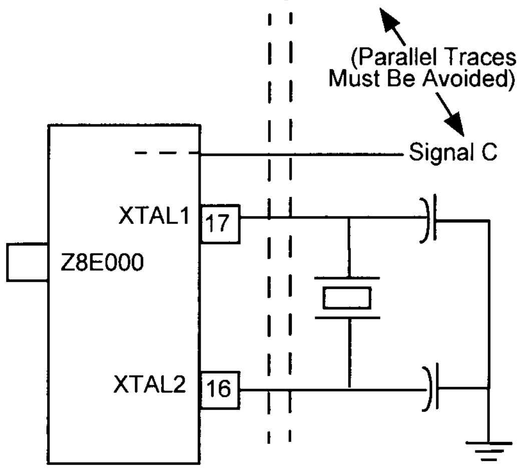
- To prevent induced noise, the crystal and load capacitors should be physically located as close to the Z8E000 as possible.
- Signal lines should not run parallel to the clock oscillator inputs. In particular, the crystal input circuitry and the internal system clock output should be separated as much as possible.

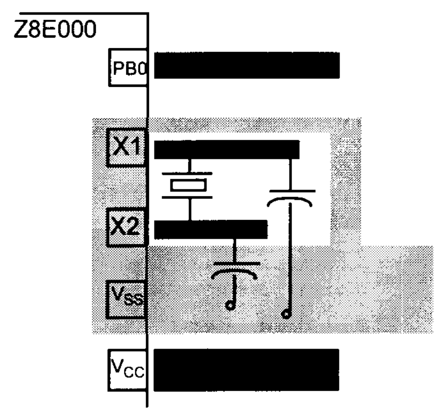
OSCILLATOR OPERATION (Continued)

- V_{CC} power lines should be separated from the clock oscillator input circuitry.
- Resistance between XTAL1 or XTAL2 and the other pins should be greater than 10 MΩ.



Clock Generator Circuit





Board Design Example

(Top View)

Figure 15. Circuit Board Design Rules

Crystals and Resonators

Crystals and ceramic resonators (Figure 16) should have the following characteristics to ensure proper oscillator operation:

Crystal Cut	AT (crystal only)
Mode	Parallel, Fundamental Mode
Crystal Capacitance	<7pF
Load Capacitance	10pF < CL < 220 pF, 15 typical
Resistance	100 ohms max

Depending on operation frequency, the oscillator can require the addition of capacitors C_1 and C_2 (shown in Figure 17 and Figure 18). The capacitance values are dependent on the manufacturer's crystal specifications.

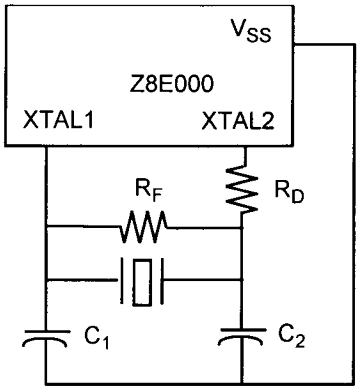


Figure 16. Crystal/Ceramic Resonator Oscillator

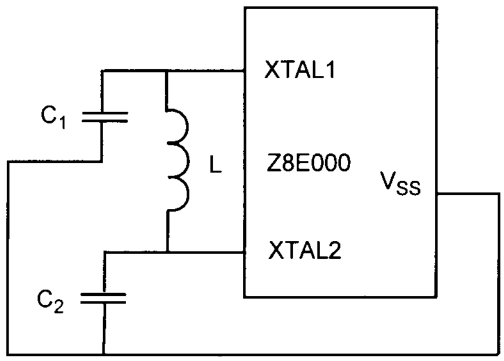


Figure 17. LC Clock

In most cases, the R_D is zero ohms (0Ω), and R_F is infinite. The set value is determined and specified by the crystal/ceramic resonator manufacturer. R_D can be increased to decrease the amount of drive from the oscillator output to the crystal. R_D can also be used as an adjustment to avoid clipping of the oscillator signal to reduce noise. R_F can be used to improve the start-up of the crystal/ceramic resonator. The Z8E000 oscillator already has an internal shunt resistor in parallel to the crystal/ceramic resonator.

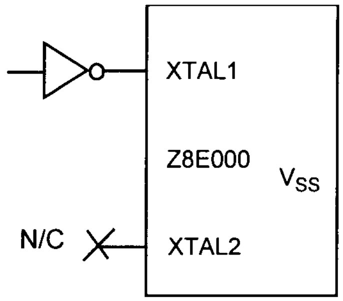


Figure 18. External Clock

Figure 16, Figure 17, and Figure 18 recommend that the load capacitor ground trace connect directly to the V_{SS} (GND) pin of the Z8E000, thereby ensuring that no system noise is injected into the Z8E000 clock. This trace should not be shared with any other components except at the V_{SS} pin of the Z8E000.

Note: A parallel resonant crystal or resonator data sheet will specify a load capacitor value that is the series combination of C_1 and C_2, including all parasitics (PCB and holder).

TIMERS (Continued)

er, when hardware clears a control register bit for a timer that is configured for single-shot operation, the clearing of the control bit will override a software write. Reading either register can be done at any time, and will have no effect on the functionality of the timer.

When defined to operate as a single 16-bit entity, the entire 16-bit value must reach 0 before an interrupt is generated. In this case, a single interrupt will be generated, and the interrupt will correspond to the even 8-bit timer. For example, timers T2 and T3 are cascaded to form a single 16-bit timer, so the interrupt for the combined timer will be defined to be that of timer T2 rather than T3 (Figure 20). When a timer pair is specified to act as a single 16-bit timer, the even timer registers in the pair (timer T2) will be defined to hold the timer's least significant byte. Conversely, the odd timer in the pair (timer T3) will hold the timer's most significant byte.

In parallel with the posting of the interrupt request, the interrupting timer's count value will be initialized by copying the contents of the auto-initialization value register to the count value register.

Note: Any time that a timer pair is defined to act as a single 16-bit timer, the auto-reload function will be performed automatically. All 16-bit timers will continue counting while their interrupt requests are active, and will operate in a free-running manner.

If interrupts are disabled for a long period of time, it is possible for the timer to decrement to 0 again before its initial interrupt has been responded to. This condition is termed a degenerate case, and hardware is not required to detect it.

When the timer control register is written, all timers that are enabled by the write will begin counting using the value that is held in their count register. In this case, an auto-initialization is not performed. All timers can receive an internal clock source only. Each timer that is enabled will be updated every 8th XTAL clock cycle.

RESET CONDITIONS

After a hardware $\overline{\text{RESET}}$, the timers are disabled. See Table 5 for timer control, value, and auto-initialization register status after $\overline{\text{RESET}}$.

I/O PORTS

The Z8E000 has 13 lines dedicated to input and output. These lines are grouped into two ports known as Port A and Port B. Port A is an 8-bit port that is bit-programmable as either inputs or outputs. Port B can be programmed to provide standard input/output or the following special functions: SMR input and external interrupt inputs.

All ports have push-pull CMOS outputs. In addition, the outputs of Port A, on a bit-wise basis, can be configured for open-drain operation. As such, the register values for "/" at a given bit position only affect the bit in question.

Each port is defined by a set of four control registers. See Figure 21.

Directional Control and Special Function Registers

Each port on the Z8E000 has an associated and dedicated Directional Control Register that determines on a bit-wise basis whether a given port bit will operate as an input or as an output.

Each port on the Z8E000 has a Special Function Register that, in conjunction with the directional control register, implements on a bit-wise basis, and supports special functionality that can be defined for each particular port bit.

Input and Output Value Registers

Each port has an Output Value Register and an Input Value Register. For port bits configured as an input by means of the Directional Control Register, the Input Value Register for that bit position will contain the current synchronized input value.

REGISTER	ADDRESS	IDENTIFIER
Port B SPECIAL FUNCTION	0D7H	PTBSFR
Port B DIRECTIONAL CONTROL	0D6H	PTBDIR
Port B OUTPUT VALUE	0D5H	PTBOUT
Port B INPUT VALUE	0D4H	PTBIN
Port A SPECIAL FUNCTION	0D3H	PTASFR
Port A DIRECTIONAL CONTROL	0D2H	PTADIR
Port A OUTPUT VALUE	0D1H	PTAOUT
Port A INPUT VALUE	0D0H	PTAIN

Figure 21. Z8E000 I/O Ports Registers

For port bits configured as an output by means of the Directional Control Register, the value held in the corresponding bit of the Output Value Register is driven directly onto the output pin. The opposite register bit for a given pin (the output register bit for an input pin and the input register bit for an output pin) will hold their previous value. They will not be changed by hardware nor will they have any effect on the hardware.

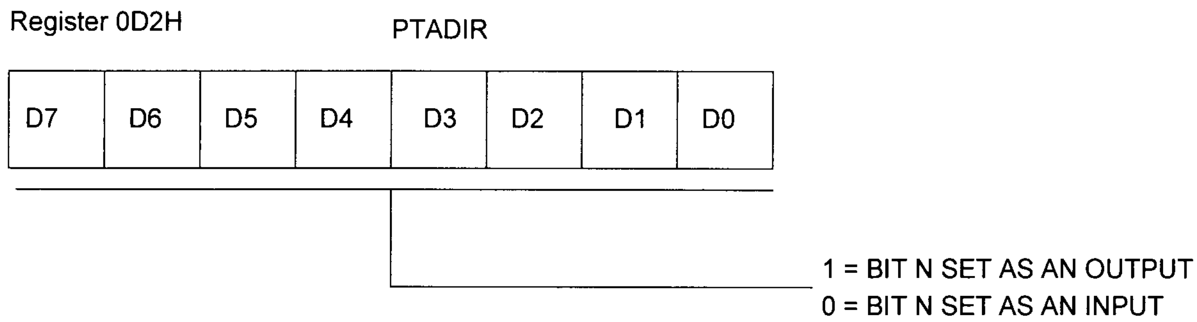


Figure 26. Port A Directional Control Register

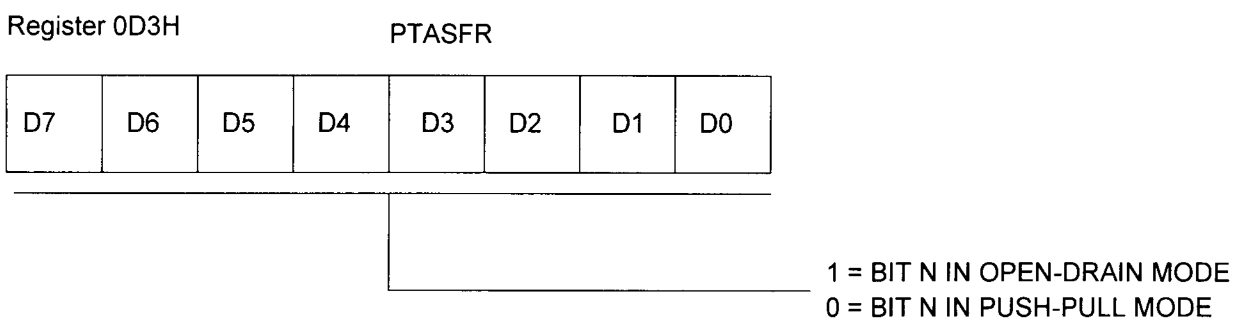


Figure 27. Port A Special Function Register

PORT B—PIN 0 CONFIGURATION

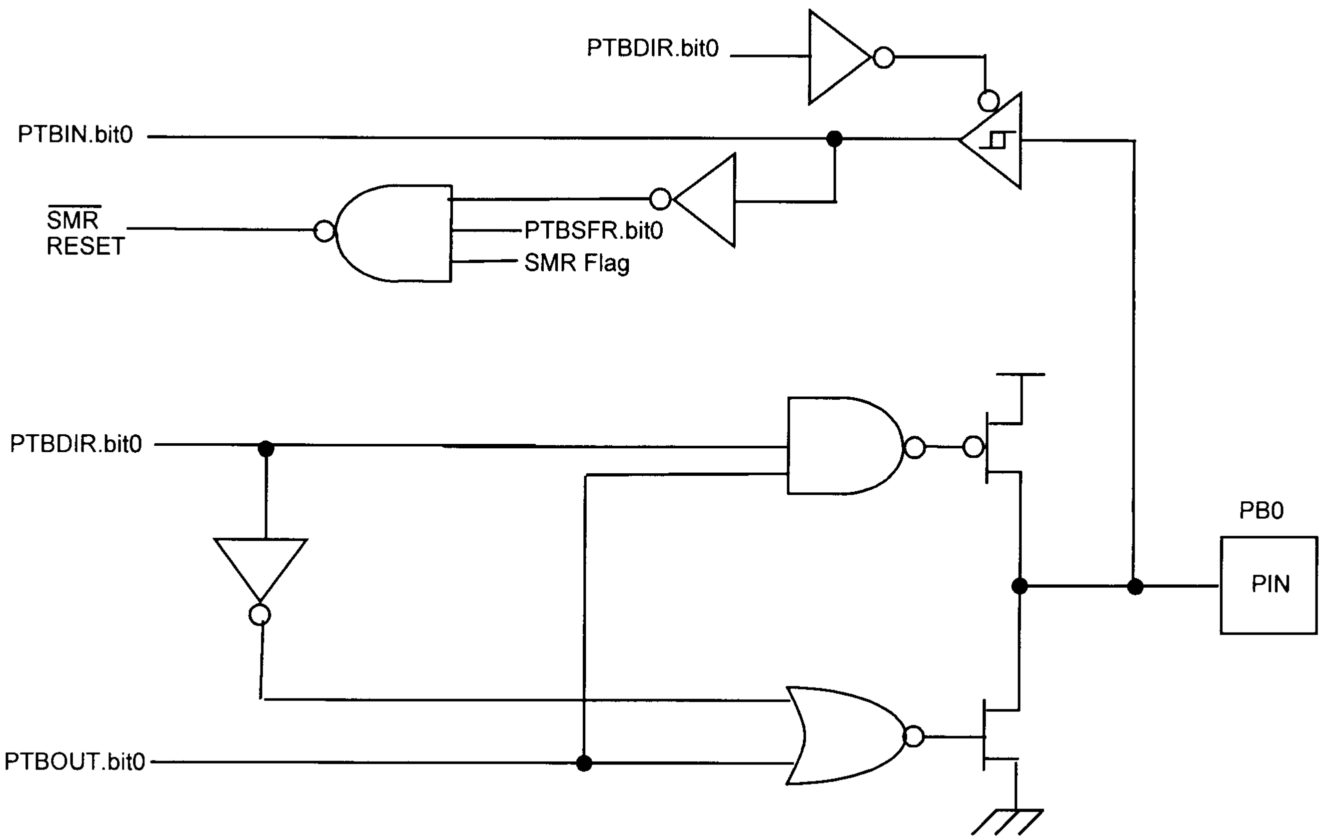


Figure 29. Port B Pin 0 Diagram

PORT B CONTROL REGISTER DEFINITIONS

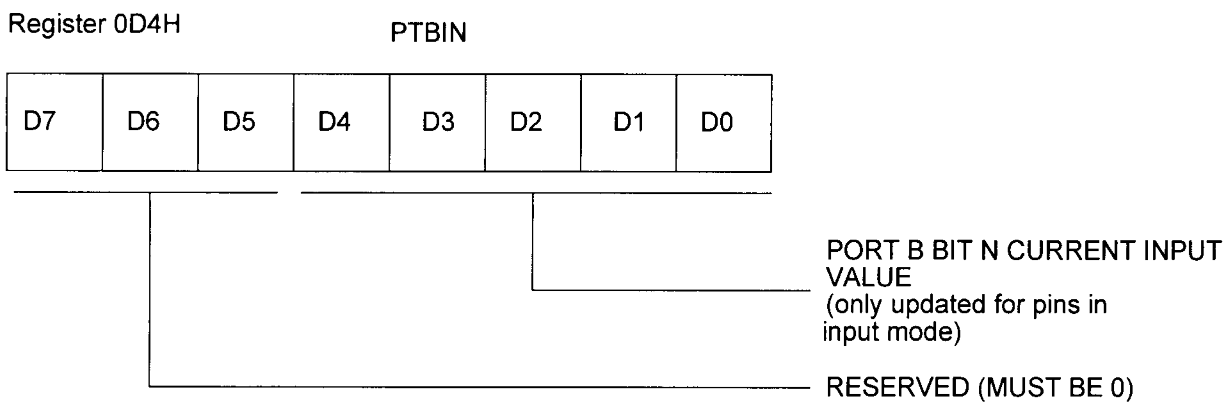


Figure 33. Port B Input Value Register

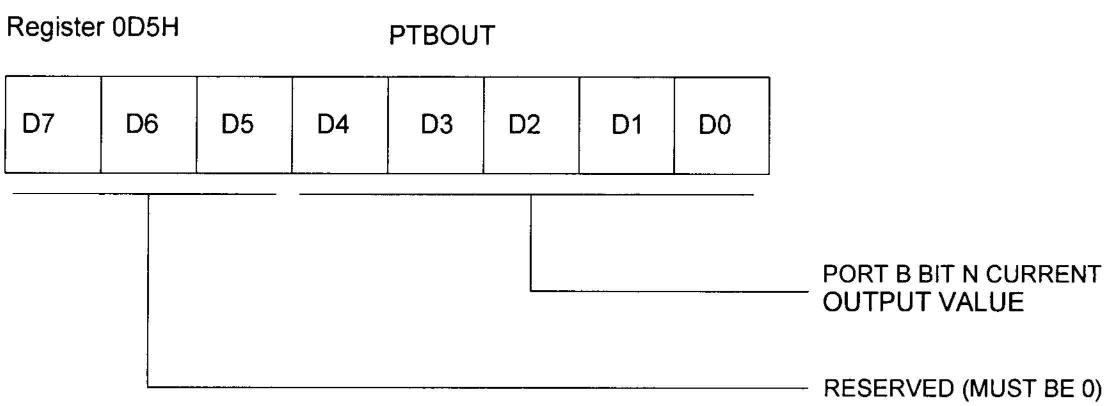


Figure 34. Port B Output Value Register

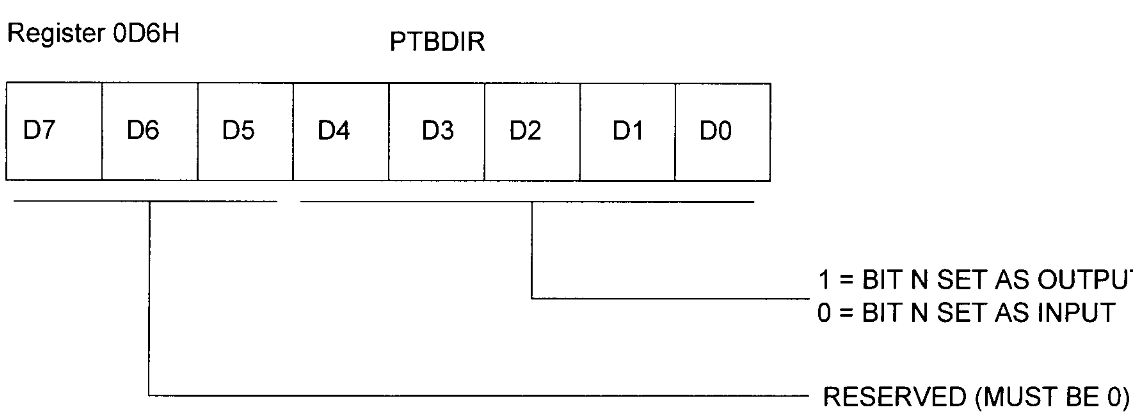


Figure 35. Port B Directional Control Register

PORT B CONTROL REGISTER DEFINITIONS (Continued)

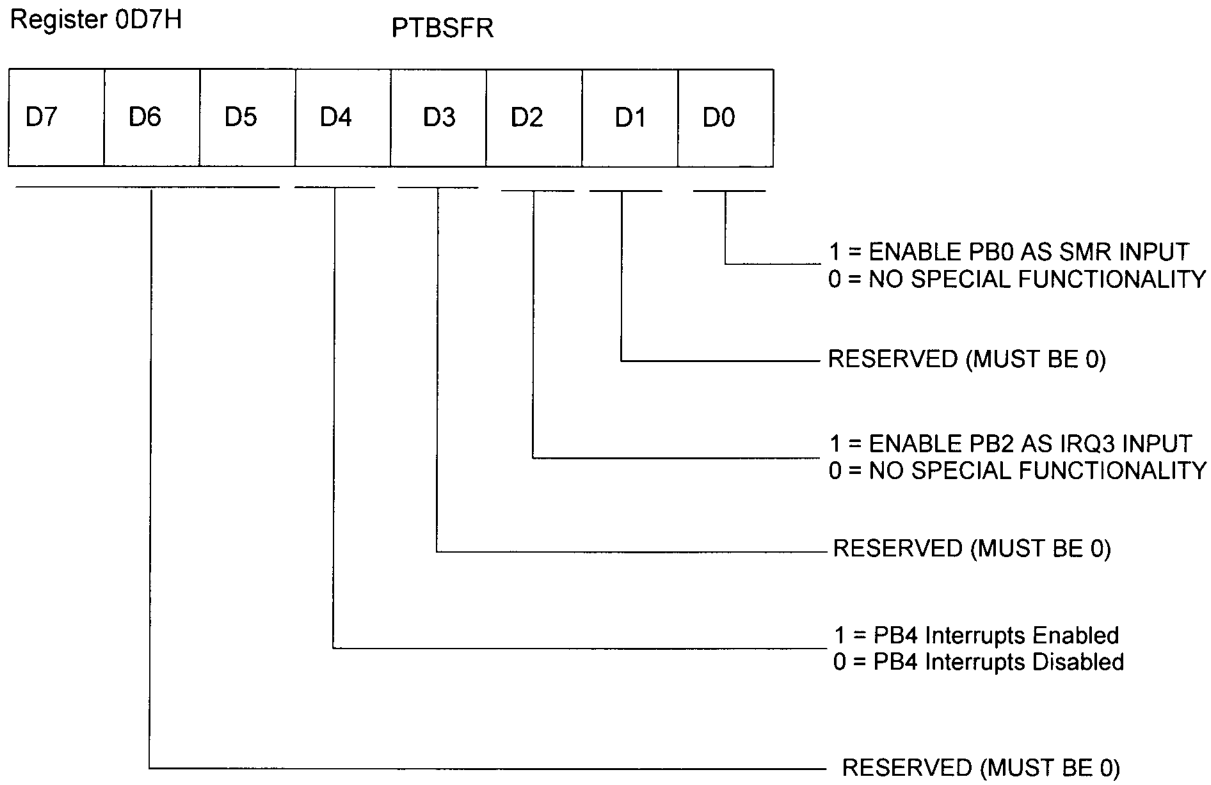
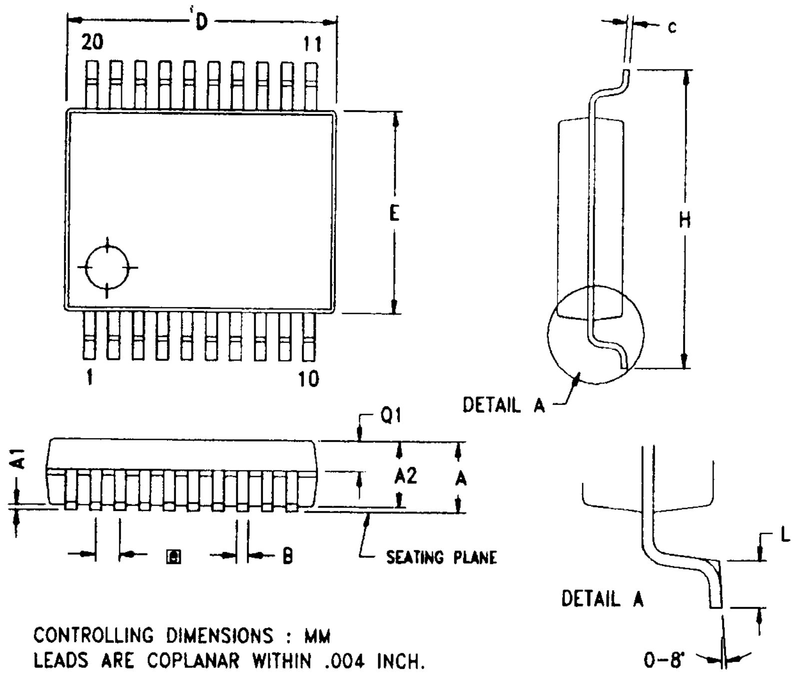


Figure 36. Port B Special Function Register



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
B	0.25	0.30	0.38	0.010	0.012	0.015
C	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 TYP			0.0256 TYP		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032

Figure 41. 20-Pin SSOP Package Diagram

ORDERING INFORMATION

Standard Temperature		
18-Pin DIP	**18-Pin SOIC**	**20-Pin SSOP**
Z8E00010PSC	Z8E00010SSC	Z8E00010HSC

Extended Temperature		
18-Pin DIP	**18-Pin SOIC**	**20-Pin SSOP**
Z8E00010PEC	Z8E00010SEC	Z8E00010HEC

For fast results, contact your local ZiLOG sales office for assistance in ordering the part(s) required.

Codes	
Preferred Package	P = Plastic DIP
Longer Lead Time	S = SOIC
	H = SSOP
Preferred Temperature	S = 0°C to +70°C
	E = –40°C to +105°C
Speed	10 = 10 MHz
Environmental	C = Plastic Standard

Example:

Z 8E000 10 P S C is a Z86E000, 10 MHz, DIP, 0° to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 10 — Speed
- 8E000 — Product Number
- Z — ZiLOG Prefix