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What is "Embedded - Microcontrollers"?

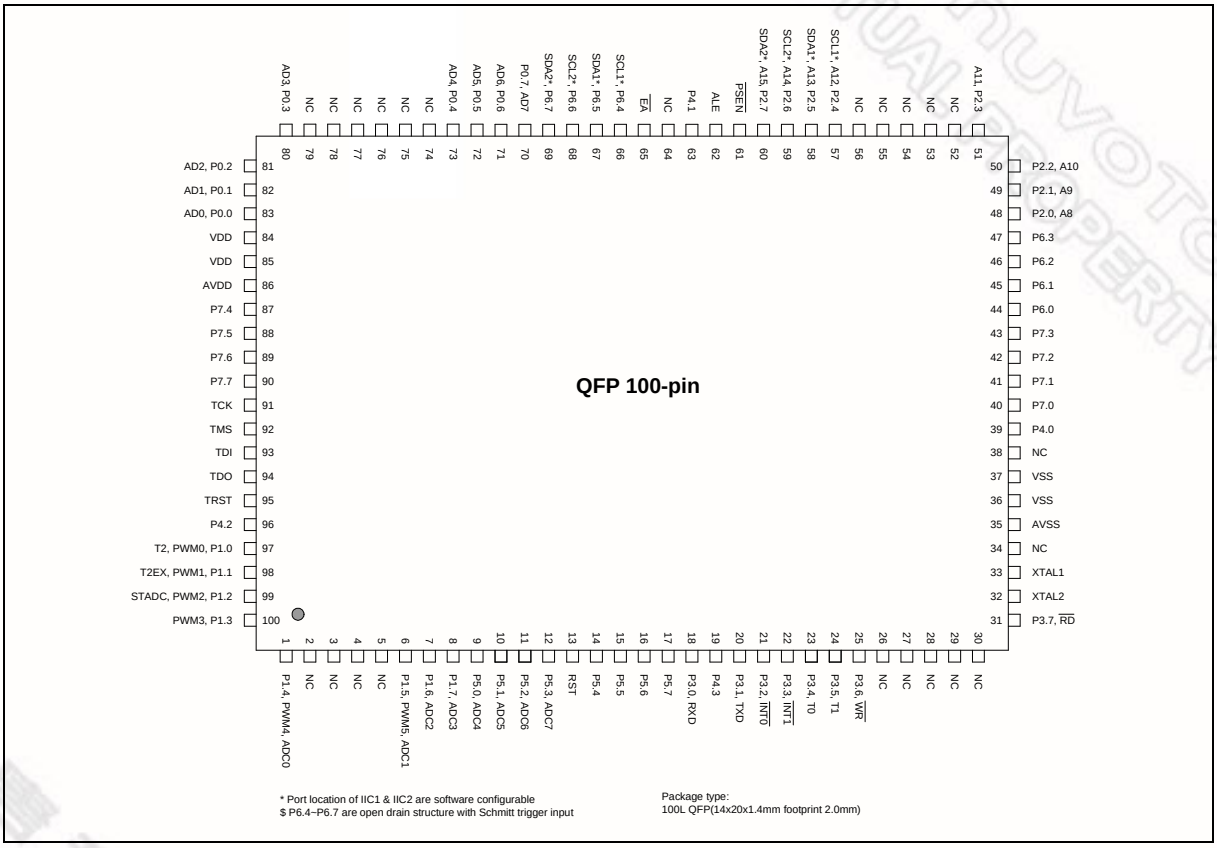
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, I²C, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	60
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e658a40fl

DEVICE	OPERATING FREQUENCY	OPERATING VOLTAGE	PACKAGE
			LEAD FREE(ROHS)
W79E658A40FL	up to 40MHz	4.5V ~ 5.5V	QFP100
W79L658A25FL	up to 25MHz	3.0V ~ 4.5V	QFP100

3. Pin Configuration



* Port location of IIC1 & IIC2 are software configurable
$ P6.4~P6.7 are open drain structure with Schmitt trigger input

Package type:
100L QFP(14x20x1.4mm footprint 2.0mm)

Table 6-3 Special Function Registers, continued

SYMBOL	DEFINITION	ADDRESS	MSB BIT_ADDRESS, SYMBOL LSB								RESET
PWM4	PWM4 Output	CFH									0000 0000B
PWMCON2	PWM Control Register 2	CEH	-	-	-	-	PWM5OE	PWM4OE	ENPWM5	ENPWM4	0000 0000B
TH2	T2 reg. High	CDH									0000 0000B
TL2	T2 reg. Low	CCH									0000 0000B
RCAP2H	T2 Capture Low	CBH									0000 0000B
RCAP2L	T2 Capture High	CAH									0000 0000B
T2MOD	Timer 2 Mode	C9H	-	-	-	-	T2CR	-	-	DCEN	xxxx 0xx0B
T2CON	Timer 2 Control	C8H	(CF) TF2	(CE) EXF2	(CD) RCLK	(CC) TCLK	(CB) EXEN2	(CA) TR2	(C9) C/T2	(C8) CP/RL2	0000 0000B
TA	Time Access Register	C7H									0000 0000B
ADCPS	ADC Input Pin Switch	C6H	ADCPS.7	ADCPS.6	ADCPS.5	ADCPS.4	ADCPS.3	ADCPS.2	ADCPS.1	ADCPS.0	0000 0000B
STATUS	Status Register	C5H	-	HIP	LIP	-	-	-	-	-	x00x xxxxB
PMR	Power Management Register	C4H	-	-	-	-	-	ALEOFF	-	DME0	xxxx x0x0B
PWM5	PWM5 Output	C3H									0000 0000B
ADCH	ADC converter Result High Byte	C2H	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2	xxxx xxxxxB
ADCL	ADC converter Result Low Byte	C1H	ADCLK1	ADCLK0	-	-	-	-	ADC.1	ADC.0	00xx xxxxxB
ADCCON	ADC Control Register	C0H	ADCEN	-	ADCEX	ADCI	ADCS	AADR2	AADR1	AADR0	0x000000B
SADEN	Slave Address Mask	B9H									0000 0000B
IP	Interrupt Priority	B8H	(BF) -	(BE) PADC	(BD) PT2	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	x000 0000B
P7	Port 7	B3H									1111 1111B
P6	Port 6	B2H									1111 1111B
P5	Port 5	B1H									1111 1111B
P3	Port 3	B0H	(B7) RD	(B6) WR	(B5) T1	(B4) T0	(B3) INT1	(B2) INT0	(B1) TXD	(B0) RXD	1111 1111B
SFRCN	F/W Flash Control	AFH	BANK	WFWIN	NOE	NCE	CTRL3	CTRL2	CTRL1	CTRL0	0011 1111B
SFRFD	F/W Flash Data	AEH									xxxx xxxxxB
SFRAH	F/W Flash High Address	ADH									0000 0000B
SFRAL	F/W Flash Low Address	ACH									0000 0000B
ROMCON	ROM Control	ABH	-	-	-	-	EN128K	DCP12	DCP11	DCP10	00000111B
SADDR	Slave Address	A9H									0000 0000B
IE	Interrupt Enable	A8H	(AF) EA	(AE) EADC	(AD) ET2	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	0000 0000B

P4.2 Base Address Low Byte Register

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: P42AL Address: 9Ah

P4.2 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: P42AH Address: 9Bh

P4.3 Base Address Low Byte Register

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: P43AL Address: 9Ch

P4.3 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: P43AH Address: 9Dh

ISP Control Register

Bit:	7	6	5	4	3	2	1	0
	SWRST /HWB	-	LD/AP	-	-	-	LDSEL	ENP

Mnemonic: CHPCON Address: 9Fh

BIT	NAME	FUNCTION
7	W:SWRST R:HWB	Write access to this bit is different from read access. Set this bit to reset the device. This has the same effect as asserting the RST pin. The microcontroller returns to its initial state, and this bit is cleared automatically. Reading this bit indicates whether or not the device is in ISP hardware reboot mode.
6	-	Reserved
5	LD/AP (read-only)	0: CPU is executing AR Flash EPROM 1: CPU is executing LD Flash EPROM
4-2	-	Reserved
1	LDSEL (write-only)	Load ROM Location Selection. This bit should be set before entering ISP mode. 1: Run the program in LD Flash EPROM. 0: Run the program in AP Flash EPROM.

TIMER 2 CAPTURE LSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0

Mnemonic: RCAP2L Address: CAh

RCAP2L (Capture mode) This register captures the LSB of Timer 2 (TL2). (Auto-reload mode) This register is the LSB of the 16-bit reload value.

TIMER 2 CAPTURE MSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0

Mnemonic: RCAP2H Address: CBh

RCAP2H (Capture mode) This register captures the MSB of Timer 2 (TH2). (Auto-reload mode) This register is the MSB of the 16-bit reload value.

TIMER 2 LSB

Bit:	7	6	5	4	3	2	1	0
	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0

Mnemonic: TL2 Address: CCh

TL2 Timer 2 LSB

TIMER 2 MSB

Bit:	7	6	5	4	3	2	1	0
	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0

Mnemonic: TH2 Address: CDh

TH2 Timer 2 MSB

PWM Control Register2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	PWM5OE	PWM4OE	ENPWM5	ENPWM4

Mnemonic: PWMCON2 Address: CEh

BIT	NAME	FUNCTION
7~4	-	Reserved.
3	PWM5OE	Output enable for PWM5 0: Disable PWM5 Output. 1: Enable PWM5 Output.
2	PWM4OE	Output enable for PWM4 0: Disable PWM4 Output. 1: Enable PWM4 Output.
1	ENPWM5	Enable PWM5 0: Disable PWM5. 1: Enable PWM5.
0	ENPWM4	Enable PWM4 0: Disable PWM4. 1: Enable PWM4.

Continued

BIT	NAME	FUNCTION
3	PWM1OE	Output enable for PWM1 0: Disable PWM1 Output. 1: Enable PWM1 Output.
2	PWM0OE	Output enable for PWM0 0: Disable PWM0 Output. 1: Enable PWM0 Output.
1	ENPWM1	Enable PWM1 0: Disable PWM1. 1: Enable PWM1.
0	ENPWM0	Enable PWM0 0: Disable PWM0. 1: Enable PWM0.

PWM2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-

Mnemonic: PWM2 Address: DDh

PWM2.7-0 Adjust PWM2 duty cycle.

PWM3

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-

Mnemonic: PWM3 Address: DEh

PWM3.7-0 Adjust PWM3 duty cycle.

ACCUMULATOR

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

ACC.7-0 The A (or ACC) register is the standard 8051/52 accumulator.

EXTENDED INTERRUPT ENABLE

Bit:	7	6	5	4	3	2	1	0
	-	-	-	EWDI	-	-	EI2C2	EI2C1

Mnemonic: EIE Address: E8h

EWDI Enable Watchdog timer interrupt

EI2C2 Enable I2C channel 2 interrupt

EI2C1 Enable I2C channel 1 interrupt

I2C Control Register Channel 1

Bit:	7	6	5	4	3	2	1	0
	-	ENS1	STA	STO	SI	AA	-	PSEL1

Mnemonic: I2CON Address: E9h

ENS1 Enable channel 1 of I2C serial function block. When ENS1=1 the channel 1 of I2C serial function enables. The port latches of SDA1 and SCL1 must be set to logic high.

STA I2C START Flag. Setting STA to logic 1 to enter master mode, the I2C hardware sends a START or repeat START condition to bus when the bus is free.

STO I2C STOP Flag. In master mode, setting STO to transmit a STOP condition to bus then I2C hardware checks the bus condition, if a STOP condition is detected this flag will be cleared by hardware automatically. In a slave mode, setting STO resets I2C hardware to the defined "not addressed" slave mode.

SI I2C Port 1 Interrupt Flag. When a new SIO1 state is present in the S1STA register, the SI flag is set by hardware, and if the EA and EI2C1 bits are both set, the I2C1 interrupt is requested. SI must be cleared by software.

AA Assert Acknowledge Flag. If AA is set to logic 1, an acknowledged signal (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line. If AA is cleared, a non-acknowledged signal (high level to SDA) will be returned during the acknowledge clock pulse on the SCL line.

PSEL1 I2C Port1 Select bit. I2C port1 pair of SCL1 and SDA1, can be configured to pair of P2.4 and P2.5 if PSEL1=0 or to pair of P6.4 and P6.5 if PSEL1=1. The default value of bit PSEL1 is logic 0. Note that pin from P6.4 to P6.7 are open drain type.

I2C Channel 1 Address Register 0

Bit:	7	6	5	4	3	2	1	0
	I2ADDR.7	I2ADDR.6	I2ADDR.5	I2ADDR.4	I2ADDR.3	I2ADDR.2	I2ADDR.1	GC

Mnemonic: I2ADDR10 Address: EAh

I2ADDR10.7-1 I2C1 Slave Address0. The 8051 uC can read from and write to this 8-bit, directly addressable SFR. The contents of the register are irrelevant when I2C is in master mode. In the slave mode, the seven most significant bits must be loaded with the MCU's own slave address. The I2C hardware will react if the contents of I2ADDR10 are matched with the received slave address.

GC Enable General Call Function. The GC bit is set the I2C port1 hardware will respond to General Call address (00H). Clear GC bit to disable general call function.

I2C Channel 1 Address Register 1

Bit:	7	6	5	4	3	2	1	0
	I2ADDR.7	I2ADDR.6	I2ADDR.5	I2ADDR.4	I2ADDR.3	I2ADDR.2	I2ADDR.1	-

Mnemonic: I2ADDR11 Address: EBh

I2ADDR11.7-1 I2C1 Slave Address1. The 8051 uC can read from and write to this 8-bit, directly addressable SFR. The contents of the register are irrelevant when I2C is in master mode. In the slave mode, the seven most significant bits must be loaded with the MCU's own slave address. The I2C hardware will react if the contents of I2ADDR11 are matched with the received slave address.

Bit0 Reserved

B.7-0 The B register is the standard 8051/52 register that serves as a second accumulator

EXTENDED INTERRUPT PRIORITY

Bit:	7	6	5	4	3	2	1	0
	-	-	-	PWDI	-	-	PI2C2	PI2C1

Mnemonic: EIP Address: F8h

PWDI Watchdog Timer Interrupt priority.

PI2C2 I2C Channel 2 Interrupt priority.

PI2C1 I2C Channel 1 Interrupt priority.

I2C Control Register Channel 2

Bit:	7	6	5	4	3	2	1	0
	-	ENS2	STA	STO	SI	AA	-	PSEL2

Mnemonic: I2CON2 Address: F9h

ENS2 Enable channel 2 of I2C serial function block. When ENS2=1 the channel 2 of I2C serial function enables. The port latches of SDA2 and SCL2 must be set to logic high.

STA I2C START Flag. Setting STA to logic 1 to enter master mode, the I2C hardware sends a START or repeat START condition to bus when the bus is free.

STO I2C STOP Flag. In master mode, setting STO to transmit a STOP condition to bus then I2C hardware will check the bus condition if a STOP condition is detected this flag will be cleared by hardware automatically. In a slave mode, setting STO resets I2C hardware to the defined “not addressed” slave mode.

SI I2C Port 2 Interrupt Flag. When a new SIO2 state is present in the S1STA register, the SI flag is set by hardware, and if the EA and EI2C2 bits are both set, the I2C2 interrupt is requested. SI must be cleared by software.

AA Assert Acknowledge Flag. If AA is set to logic 1, an acknowledged signal (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line. If AA is cleared, a non-acknowledged signal (high level to SDA) will be returned during the acknowledge clock pulse on the SCL line.

PSEL2 I2C Port2 Select bit. I2C port2 pair of SCL2 and SDA2, can be configured to pair of P2.6 and P2.7 if PSEL2=0 or to pair of P6.6 and P6.7 if PSEL2=1. The default value of bit PSEL2 is logic 0. Note that the pins from P6.4 to P6.7 are in open drain type.

I2C Channel 2 Address Register 0

Bit:	7	6	5	4	3	2	1	0
	I2ADDR.7	I2ADDR.6	I2ADDR.5	I2ADDR.4	I2ADDR.3	I2ADDR.2	I2ADDR.1	GC

Mnemonic: I2ADDR20 Address: FAh

I2ADDR20.7-1 I2C2 Slave Address. The 8051 uC can read from and write to this 8-bit, directly addressable SFR. The contents of the register are irrelevant when I2C is in master mode. In the slave mode, the seven most significant bits must be loaded with the MCU’s own slave address. The I2C hardware will react if the contents of I2ADDR20 are matched with the received slave address.

GC Enable General Call Function. The GC bit is set the I2C port1 hardware will respond to General Call address (00H). Clear GC bit to disable general call function.

I2C Timer Counter Register Channel 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	ENTI2	DIV42	TIF2

Mnemonic: I2TIMER2 Address: FFh

ENTI2 Enable I2C 14-bits Time-out Counter. Setting ENTI to logic high will firstly reset the time-out counter and then start up counting. Clearing ENTI disables the 14-bit time-out counter. ENTI can be set to logic high only when SI=0.

DIV42 I2C Time-out Counter Clock Frequency Selection. DIV42= 0 the clock frequency is coherent to the system clock Fosc. DIV42 = 1 the clock frequency is Fosc/4.

TIF2 I2C Time-out Flag. When the time-out counter overflows hardware will set this flag and request the I2C2 interrupt if I2C2 interrupt is enabled (EI2C1=1). This bit must be cleared by software.

OP-CODE	HEX CODE	BYTES	W79E658 MACHINE CYCLE	W79E658 CLOCK CYCLES	8032 CLOCK CYCLES	W79E658 VS. 8032 SPEED RATIO
MOV direct, R3	8B	2	2	8	12	1.5
MOV direct, R4	8C	2	2	8	12	1.5
MOV direct, R5	8D	2	2	8	12	1.5
MOV direct, R6	8E	2	2	8	12	1.5
MOV direct, R7	8F	2	2	8	12	1.5
MOV direct, @R0	86	2	2	8	12	1.5
MOV direct, @R1	87	2	2	8	12	1.5
MOV direct, direct	85	3	3	12	24	2
MOV direct, #data	75	3	3	12	24	2
MOV DPTR, #data 16	90	3	3	12	24	2
MOVC A, @A+DPTR	93	1	2	8	24	3
MOVC A, @A+PC	83	1	2	8	24	3
MOVX A, @R0	E2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @R1	E3	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @DPTR	E0	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R0, A	F2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R1, A	F3	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @DPTR, A	F0	1	2 - 9	8 - 36	24	3 - 0.66
PUSH direct	C0	2	2	8	24	3
POP direct	D0	2	2	8	24	3
XCH A, R0	C8	1	1	4	12	3
XCH A, R1	C9	1	1	4	12	3
XCH A, R2	CA	1	1	4	12	3
XCH A, R3	CB	1	1	4	12	3
XCH A, R4	CC	1	1	4	12	3
XCH A, R5	CD	1	1	4	12	3
XCH A, R6	CE	1	1	4	12	3
XCH A, R7	CF	1	1	4	12	3
XCH A, @R0	C6	1	1	4	12	3
XCH A, @R1	C7	1	1	4	12	3
XCHD A, @R0	D6	1	1	4	12	3
XCHD A, @R1	D7	1	1	4	12	3
XCH A, direct	C5	2	2	8	12	1.5
CLR C	C3	1	1	4	12	3

OP-CODE	HEX CODE	BYTES	W79E658 MACHINE CYCLE	W79E658 CLOCK CYCLES	8032 CLOCK CYCLES	W79E658 VS. 8032 SPEED RATIO
CJNE R2, #data, rel	BA	3	4	16	24	1.5
CJNE R3, #data, rel	BB	3	4	16	24	1.5
CJNE R4, #data, rel	BC	3	4	16	24	1.5
CJNE R5, #data, rel	BD	3	4	16	24	1.5
CJNE R6, #data, rel	BE	3	4	16	24	1.5
CJNE R7, #data, rel	BF	3	4	16	24	1.5
DJNZ R0, rel	D8	2	3	12	24	2
DJNZ R1, rel	D9	2	3	12	24	2
DJNZ R5, rel	DD	2	3	12	24	2
DJNZ R2, rel	DA	2	3	12	24	2
DJNZ R3, rel	DB	2	3	12	24	2
DJNZ R4, rel	DC	2	3	12	24	2
DJNZ R6, rel	DE	2	3	12	24	2
DJNZ R7, rel	DF	2	3	12	24	2
DJNZ direct, rel	D5	3	4	16	24	1.5

Stretching only affects the MOVX instruction. There is no effect on any other instruction or its timing, it is as if the state of the CPU is held for the desired period. The timing waveforms when the stretch value is zero, one, and two are shown below.

Table 7-2 Data Memory Cycle Stretch Values

M2	M1	M0	MACHINE CYCLES	$\overline{RD}$ OR $\overline{WR}$ STROBE WIDTH IN CLOCKS	$\overline{RD}$ OR $\overline{WR}$ STROBE WIDTH @ 25 MHZ	$\overline{RD}$ OR $\overline{WR}$ STROBE WIDTH @ 40 MHZ
0	0	0	2	2	80 nS	50 nS
0	0	1	3 (default)	4	160 nS	100 nS
0	1	0	4	8	320 nS	200 nS
0	1	1	5	12	480 nS	300 nS
1	0	0	6	16	640 nS	400 nS
1	0	1	7	20	800 nS	500 nS
1	1	0	8	24	960 nS	600 nS
1	1	1	9	28	1120 nS	700 nS

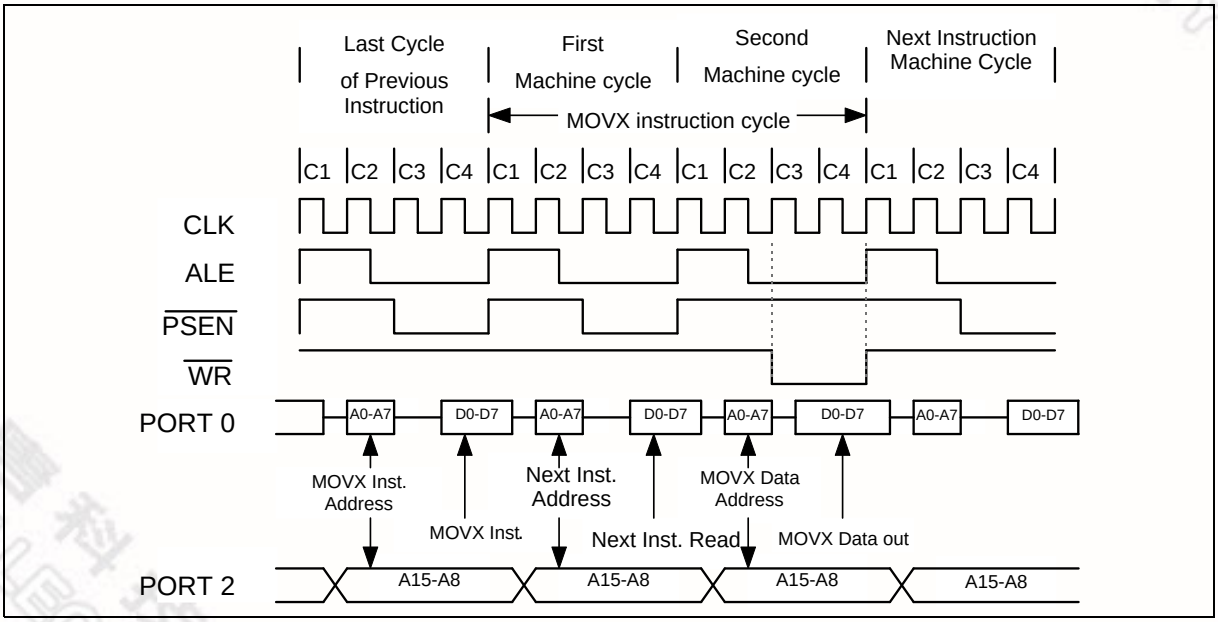


Figure 7-6 Data Memory Write with Stretch Value = 0

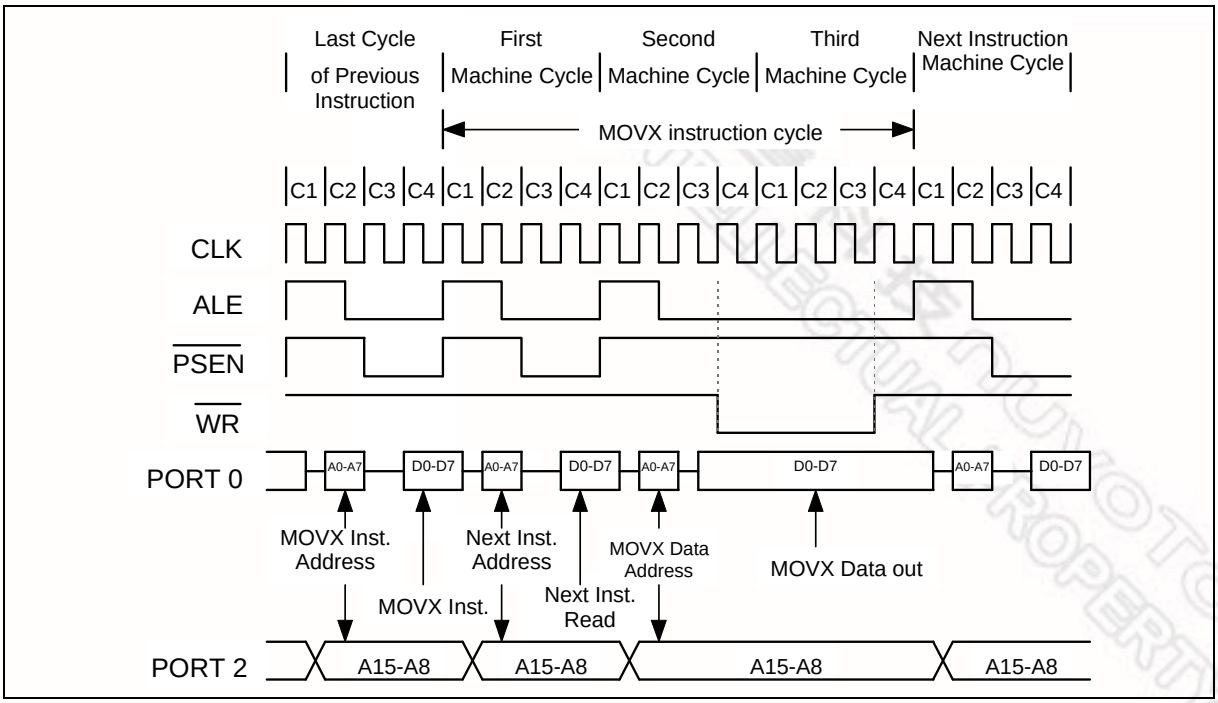


Figure 7-7 Data Memory Write with Stretch Value = 1

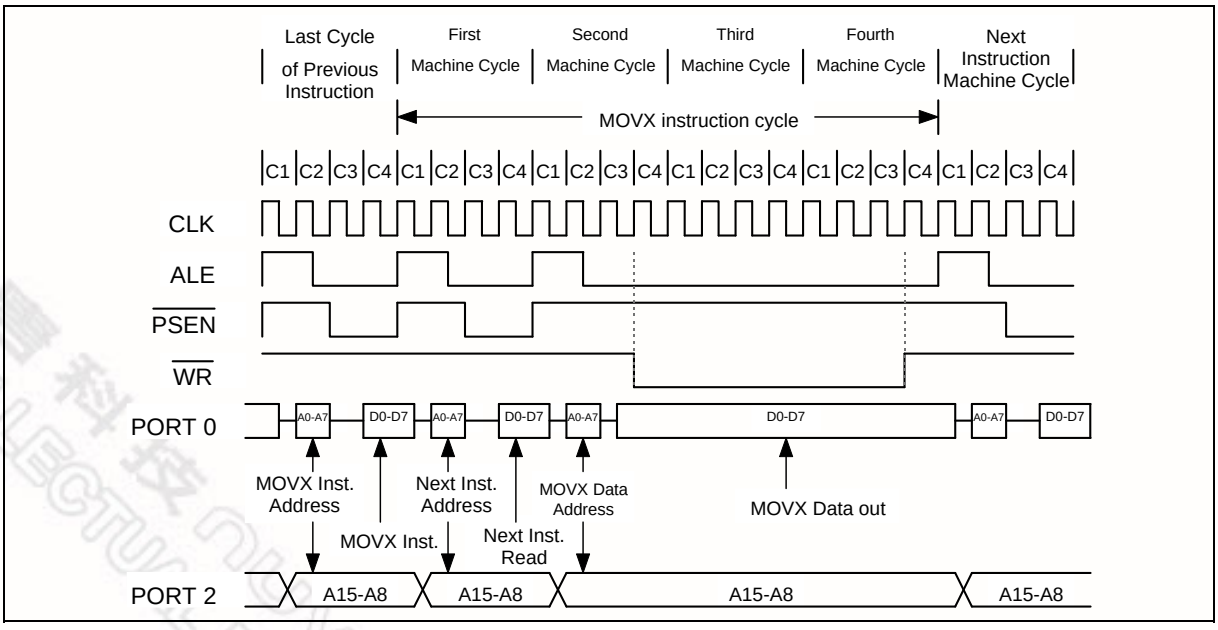


Figure 7-8 Data Memory Write with Stretch Value = 2

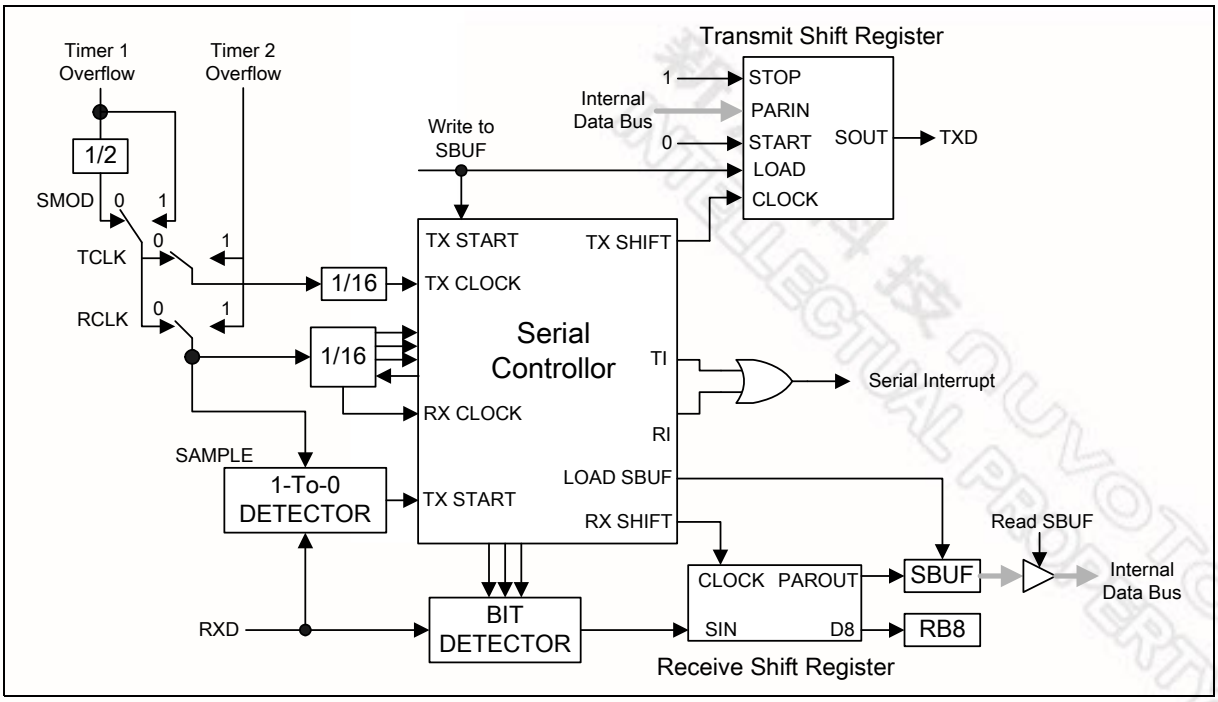


Figure 14-2 Serial Port Mode 1

14.3 Mode 2

In Mode 2, full-duplex asynchronous communication is used. Frames consist of eleven bits: one start bit (0), eight data bits (LSB first), a programmable ninth bit (TB8) and a stop bit (0). When receiving, the ninth bit is put into RB8. The baud rate is 1/16 or 1/32 of the oscillator frequency, as determined by SMOD in PCON.

Transmission begins with a write to SBUF but is synchronized with the divide-by-16 counter, not the write to SBUF. The start bit is put on TxD pin at C1 following the first roll-over of the divide-by-16 counter, and the next bit is placed on TxD at C1 following the next rollover. After all nine bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the next C1 state, or the 11th rollover of the divide-by-16 counter after the write to SBUF.

Reception is enabled when REN is high, and the serial port starts receiving data when it detects a falling edge on RxD. The falling-edge detector monitors the RxD line at 16 times the selected baud rate. When a falling edge is detected, the divide-by-16 counter is reset to align the bit boundaries with the rollovers of the counter. The 16 states of the counter divide the bit time into 16 slices. Bit detection is done on a best-of-three basis using samples at the 8th, 9th and 10th counter states. If the first bit after the falling edge is not 0, the start bit is invalid, reception is aborted, and the serial port resumes looking for a falling edge on RxD. If a valid start bit is detected, the rest of the bits are shifted into SBUF. After shifting in nine data bits, the stop bit is received. Then, if

1. RI is 0 and
2. SM2 is 0 or the received stop bit is 1

the stop bit goes into RB8, the eight data bits go into SBUF, and RI is set. Otherwise, the received frame may be lost. In the middle of the stop bit, the receiver resumes looking for a falling edge on RxD. The functional description is shown in the figure below.

15.3.1 Master/Transmitter Mode

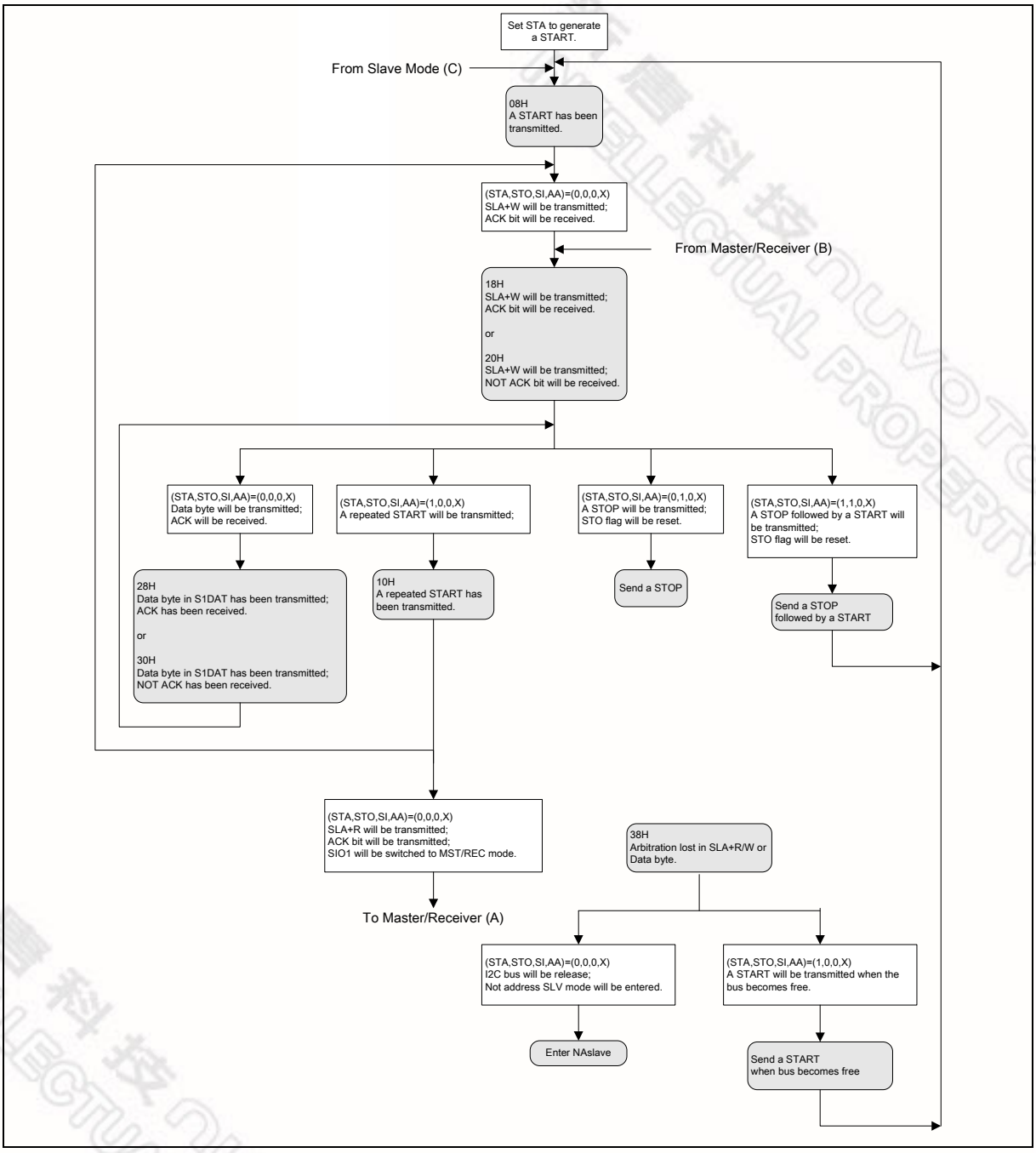


Figure 15-5 Master Transmitter Mode

15.3.2 Master/Receiver Mode

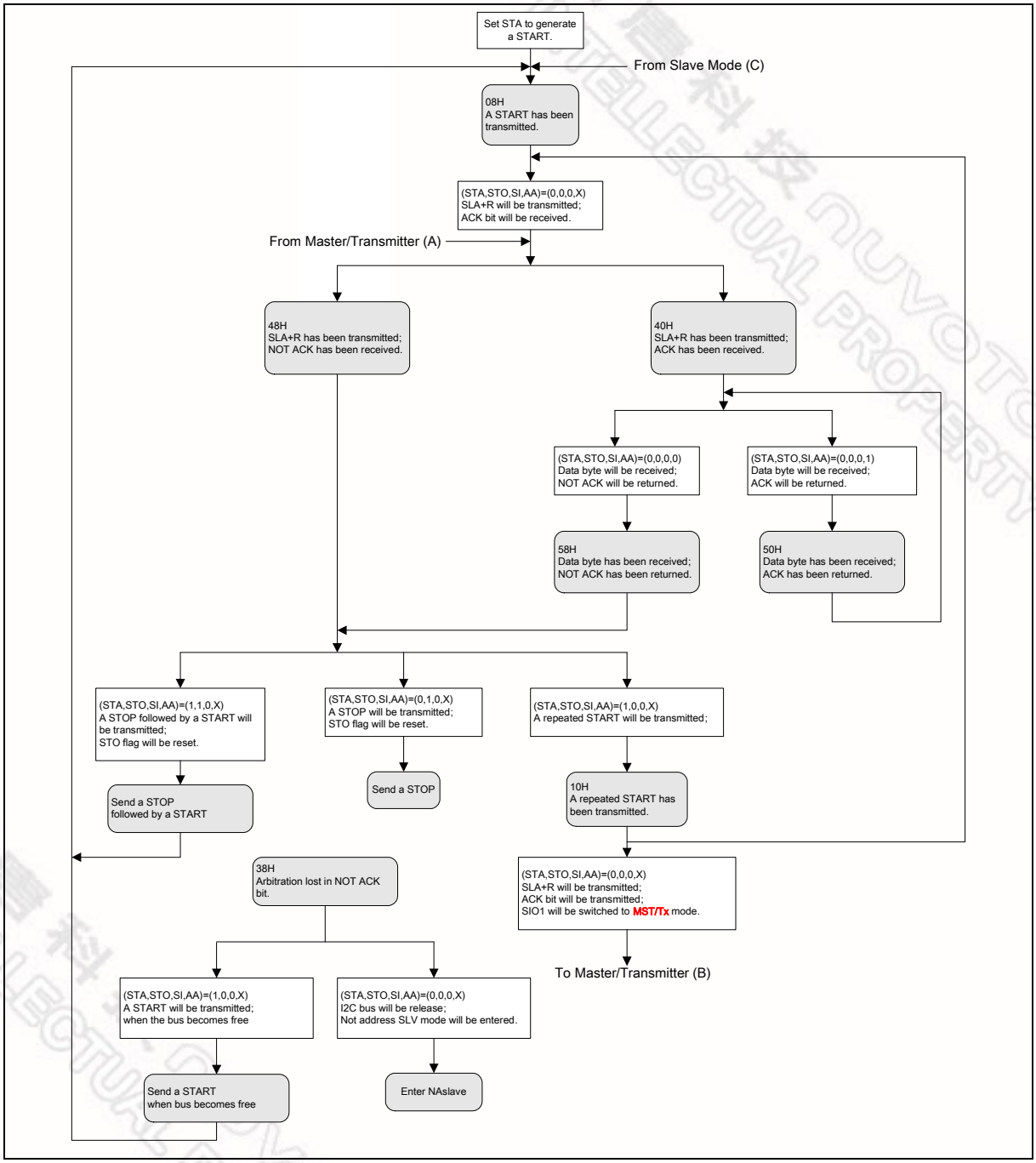


Figure 15-6 Master Receiver Mode

16.3 ADC Control Registers

ADC Control Register

Bit:	7	6	5	4	3	2	1	0
	ADCEN	-	ADCEX	ADCI	ADCS	AADR2	AADR1	AADR0

Mnemonic: ADCCON Address: C0h

ADCEN Enable A/D Converter Function. Set ADCEN to logic high to enable ADC block.

ADCEX Enable external start control of ADC conversion by a rising edge from P1.2. ADCEX=0: Disable external start. ADCEX=1: Enable external start control.

ADCI A/D Converting Complete/Interrupt Flag. This flag is set when ADC conversion is completed and will cause a hardware interrupt if ADC interrupt is enabled. It is cleared by software only.

ADCS A/D Converting Start. Setting this bit by software starts the conversion of the selected ADC input. ADCS remains high while ADC is converting signal and will be automatically cleared by hardware when ADC conversion is completed.

AADR[2:0] Select and enable analog input channel from ADC0 to ADC7.

AADR[2:0]	ADC SELECTED INPUT	AADR[2:0]	ADC SELECTED INPUT
000	ADCCH0 (P1.4)	100	ADCCH4 (P5.0)
001	ADCCH1 (P1.5)	101	ADCCH5 (P5.1)
010	ADCCH2 (P1.6)	110	ADCCH6 (P5.2)
011	ADCCH3 (P1.7)	111	ADCCH7 (P5.3)

The ADCI and ADCS control the ADC conversion as below:

ADCI	ADCS	ADC STATUS
0	0	ADC not busy; A conversion can be started.
0	1	ADC busy; Start of a new conversion is blocked.
1	0	Conversion completed; Start of a new conversion requires ADCI = 0.
1	1	This is an internal temporary state that user can ignore it.

ADC Converter Result Low Register

Bit:	7	6	5	4	3	2	1	0
	ADCLK1	ADCLK0	-	-	-	-	ADC.1	ADC.0

Mnemonic: ADCL Address: C1h

ADCLK[1:0] ADC Clock Frequency Select. The 10-bit ADC needs a clock to drive the converting that the clock frequency may not over 4MHz. ADCLK[1:0] controls the frequency of the clock to ADC block as below table.

ADCLK1	ADCLK0	ADC CLOCK FREQUENCY
0	0	Crystal clock / 4 (Default)
0	1	Crystal clock / 8
1	0	Crystal clock / 16
1	1	Reserved

Example 5: Invalid Access

```
MOV   TA, #0AAh      3 M/C
NOP                  1 M/C
MOV   TA, #055h      3 M/C
SETB  EWT            2 M/C
```

In the first three examples, the protected bits are written before the window closes. In Example 4, however, the write occurs after the window has closed, so there is no change in the protected bit. In Example 5, the second write to TA occurs four machine cycles after the first write, so the timed access window in not opened at all, and the write to the protected bit fails.

P40AH, P40AL:

The Base address register for comparator of P4.0. P40AH contains the high-order byte of address, P40AL contains the low-order byte of address.

P41AH,P41AL:

The Base address register for comparator of P4.1. P41AH contains the high-order byte of address, P41AL contains the low-order byte of address.

P42AH, P42AL:

The Base address register for comparator of P4.2. P42AH contains the high-order byte of address, P42AL contains the low-order byte of address.

P43AH, P43AL:

The Base address register for comparator of P4.3. P43AH contains the high-order byte of address, P43AL contains the low-order byte of address.

PORT 4

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	P4.3	P4.2	P4.1	P4.0

Mnemonic: P4 Address: A5h

P4.3-0 Port 4 is a bi-directional I/O port with internal pull-ups.

Port 4 Chip-select Polarity

Bit:	7	6	5	4	3	2	1	0
	P43INV	P42INV	P42INV	P40INV	-	PWDNH	RMWFP	-

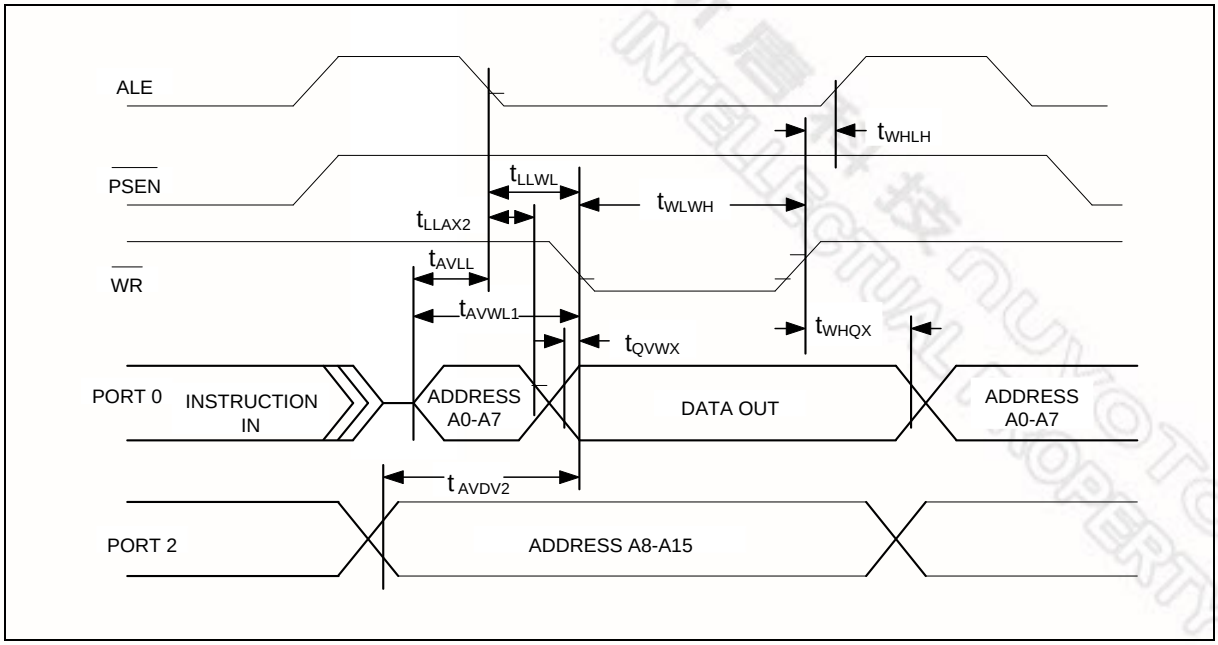
Mnemonic: P4CSIN Address: A2h

P4xINV The active polarity of P4.x when it is set as a chip-select strobe output. High = Active High. Low = Active Low.

PWDNH Set PWDNH to logic 1 then ALE and PSEN will keep high state, clear this bit to logic 0 then ALE and PSEN will output low during power down mode.

RMWFP Control Read Path of Instruction “Read-Modify-Write”. When this bit is set, the read path of executing “read-modify-write” instruction is from port pin otherwise from SFR.

23.7 Data Memory Write Cycle



```
                                ; DEPENDING ON USER'S SYSTEM CLOCK RATE.
        MOV  R7,#8AH
        MOV  TL0,R6
        MOV  TH0,R7

ERASE_P_4K:
        MOV  SFRCN,#22H     ; SFRCN = 22H, ERASE APFlash0
                            ; SFRCN = A2H, ERASE APFlash1
        MOV  TCON,#10H      ; TCON = 10H, TR0 = 1,GO
        MOV  PCON,#01H      ; ENTER IDLE MODE (FOR ERASE OPERATION)

;*********************************************************************
;* BLANK CHECK
;*********************************************************************
        MOV  SFRCN,#0H      ; SFRCN = 00H, READ APFlash0
                            ; SFRCN = 80H, READ APFlash1
        MOV  SFRAH,#0H      ; START ADDRESS = 0H
        MOV  SFRAL,#0H
        MOV  R6,#FDH        ; SET TIMER FOR READ OPERATION, ABOUT 1.5 μS.
        MOV  R7,#FFH
        MOV  TL0,R6
        MOV  TH0,R7

blank_check_loop:
        SETB  TR0           ; enable TIMER 0
        MOV  PCON,#01H      ; enter idle mode
        MOV  A,SFRFD        ; read one byte
        CJNE  A,#FFH,blank_check_error
        INC  SFRAL          ; next address
        MOV  A,SFRAL
        JNZ   blank_check_loop
        INC  SFRAH
        MOV  A,SFRAH
        CJNE  A,#0H,blank_check_loop   ; end address = FFFFH
        JMP  PROGRAM_APFlashROM

blank_check_error:
        JMP  $

;*****************************************************************************
;* RE-PROGRAMMING APFlash BANK
;*****************************************************************************
PROGRAM_APFlashROM:
```