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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	16MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	48
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.18x24.18)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p80c562eba-02-512

1 FEATURES

- 80C51 Central Processing Unit
- 8 kbytes ROM, expandable externally to 64 kbytes
- 256 bytes RAM, expandable externally to 64 kbytes
- Two standard 16-bit timer/counters
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- An 8-bit ADC with 8 multiplexed analog inputs
- Two 8-bit resolution, Pulse Width Modulated outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- Full-duplex UART compatible with the standard 80C51
- On-chip Watchdog Timer
- Oscillator frequency: 3.5 to 16 MHz.

2 GENERAL DESCRIPTION

The P80C562/P83C562 (hereafter generally referred to as P8xC562) single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family.
The P8xC562 has the same instruction set as the 80C51.
Two versions of the derivative exist:

- With 8 kbytes mask-programmable ROM
- ROMless version of the P8xC562.

This I/O intensive device provides architectural enhancements to function as a controller in the field of automotive electronics, specifically engine management and gear box control.

The P8xC562 contains a non-volatile 8 kbyte read only program memory, a volatile 256 byte read/write data memory, six 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a fourteen-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC with pulse width modulated outputs, a serial interface (UART), a Watchdog Timer and on-chip oscillator and timing circuits. For systems that require extra capability, the P8xC562 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 16 MHz crystal, 58% of the instructions are executed in 0.75 μs and 40% in 1.5 μs. Multiply and divide instructions require 3 μs.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			FREQUENCY RANGE (MHz)	TEMPERATURE RANGE (°C)
	NAME	DESCRIPTION	VERSION		
P80CE562EHA(1)	PLCC68	plastic leaded chip carrier; 68 leads	SOT188-2	3.5 to 16	–40 to +125
P80C562EBA(1)					0 to +70
P80C562EFA(1)					–40 to +85
P83C562EHA/nnn(2)					–40 to +125
P83C562EBA/nnn(2)					0 to +70
P83C562EFA/nnn(2)					–40 to +85

Notes

1. ROMless type.
2. ROM coded type; nnn denotes the ROM code number.

5 FUNCTIONAL DIAGRAM

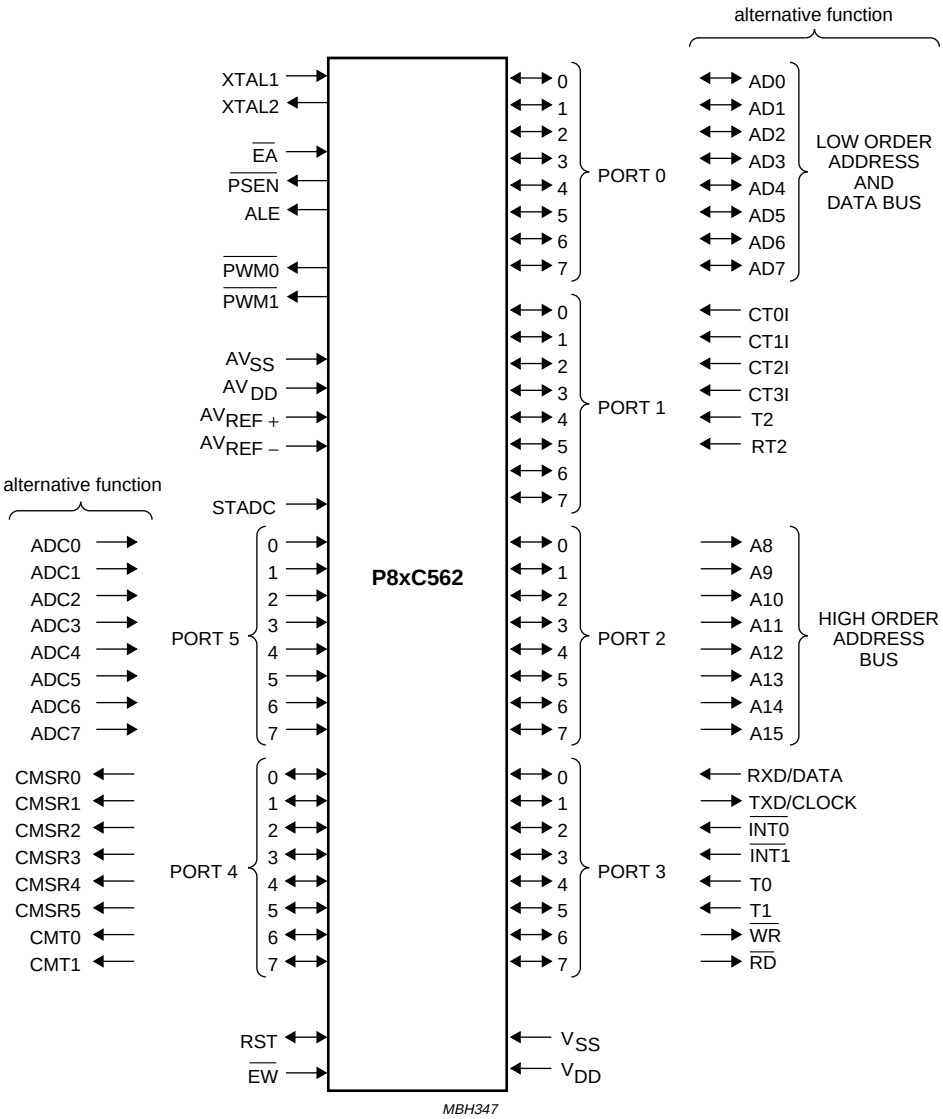


Fig.2 Functional diagram.

6 PINNING INFORMATION

6.1 Pinning

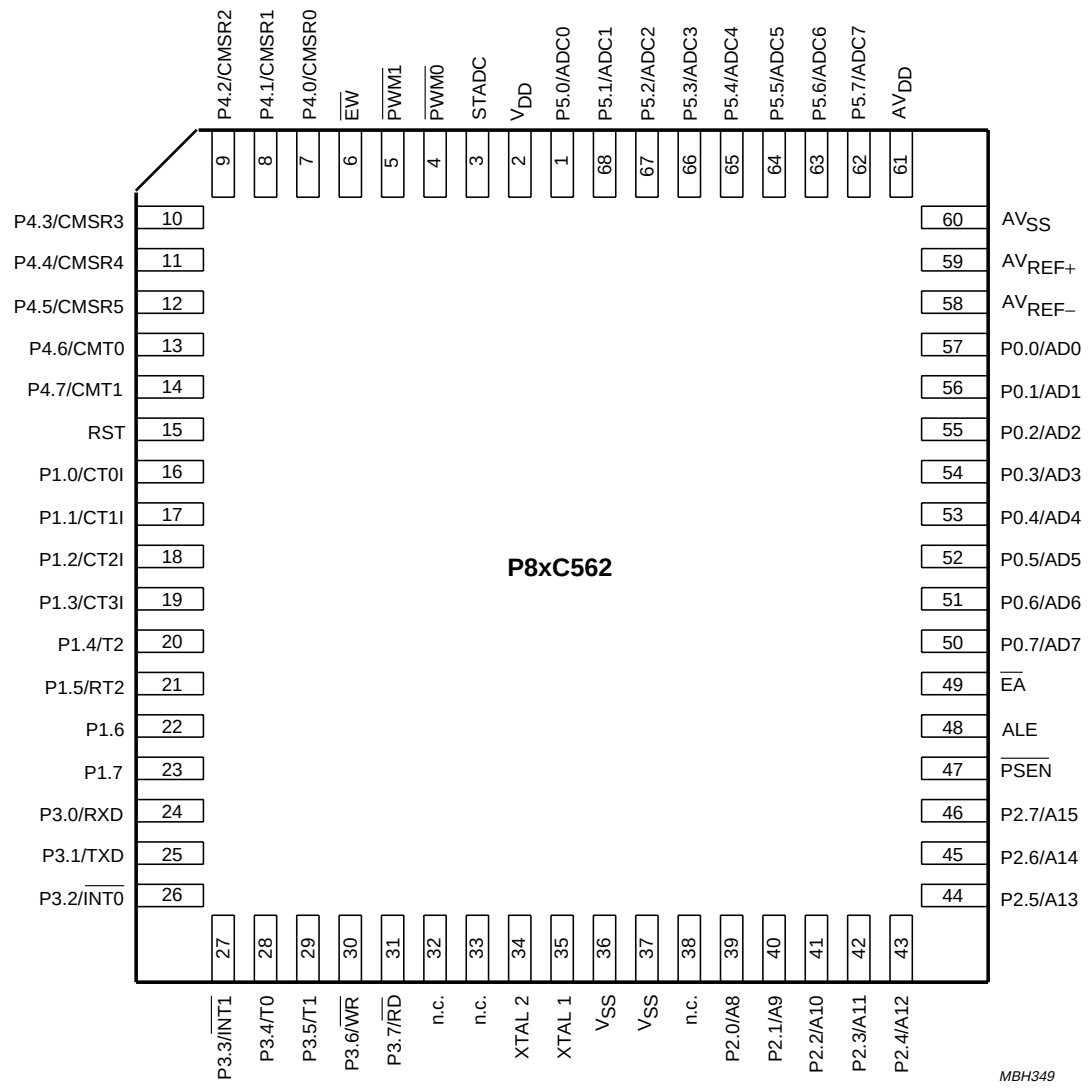


Fig.3 Pinning configuration for PLCC68 (SOT188-2) package.

8.2 Addressing

The P8xC562 has five methods for addressing source operands:

- Register
- Direct
- Register-Indirect
- Immediate
- Base-Register plus Index-Register-Indirect.

The first three methods can be used for addressing destination operands. Most instructions have a 'destination/source' field that specifies the data type, addressing methods and operands involved.
For operations other than MOVs, the destination operand is also a source operand.

Access to memory addressing is as follows:

- Registers in one of the four 8-register banks through Register, Direct or Register-Indirect
- 256 bytes of internal data RAM through Direct or Register-Indirect. Bytes 0 to 127 may be addressed directly/indirectly. Bytes 128 to 155 share their address locations with the SFR registers and so may only be addressed indirectly as data RAM
- Special Function Registers through Direct at address locations 128 to 255
- External data memory through Register-Indirect
- Program memory look-up tables through Base-Register plus Index-Register-Indirect.

The P8xC562 is classified as an 8-bit device since the internal ROM, RAM, Special Function Registers, Arithmetic Logic Unit and external data bus are all 8-bits wide. It performs operations on bit, nibble, byte and double-byte data types.

Facilities are available for byte transfer, logic and integer arithmetic operations. Data transfer, logic and conditional branch operations can be performed directly on Boolean variables to provide excellent bit handling.

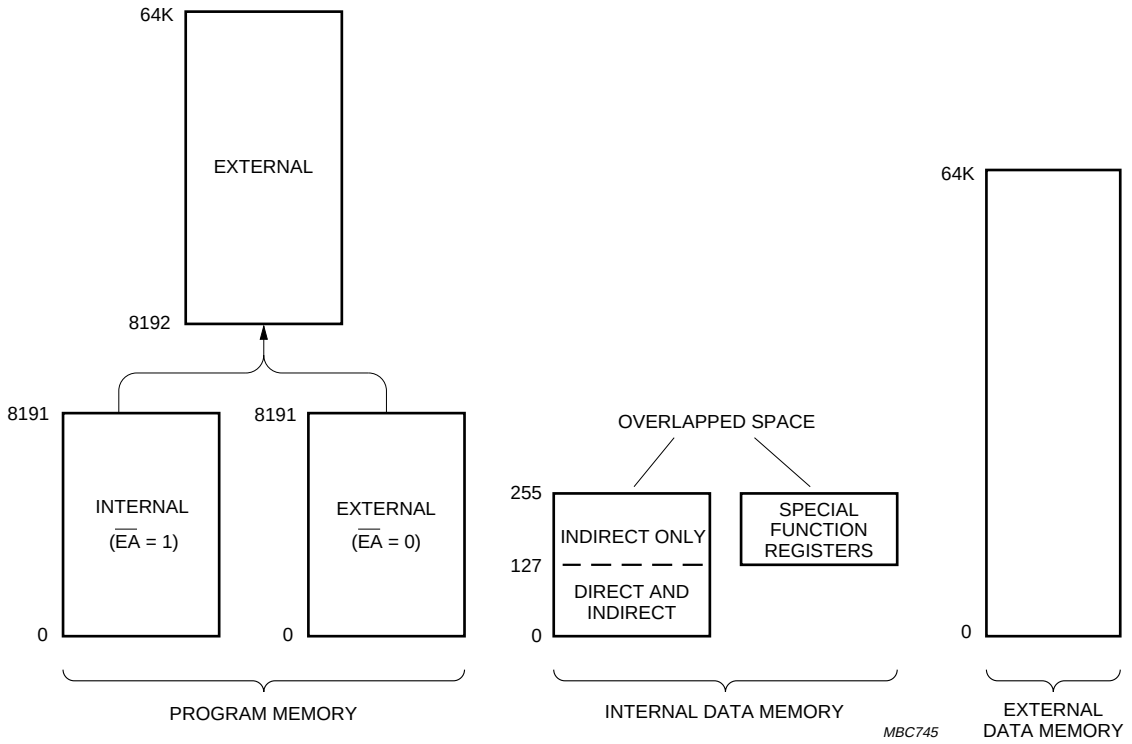


Fig.4 Memory map.

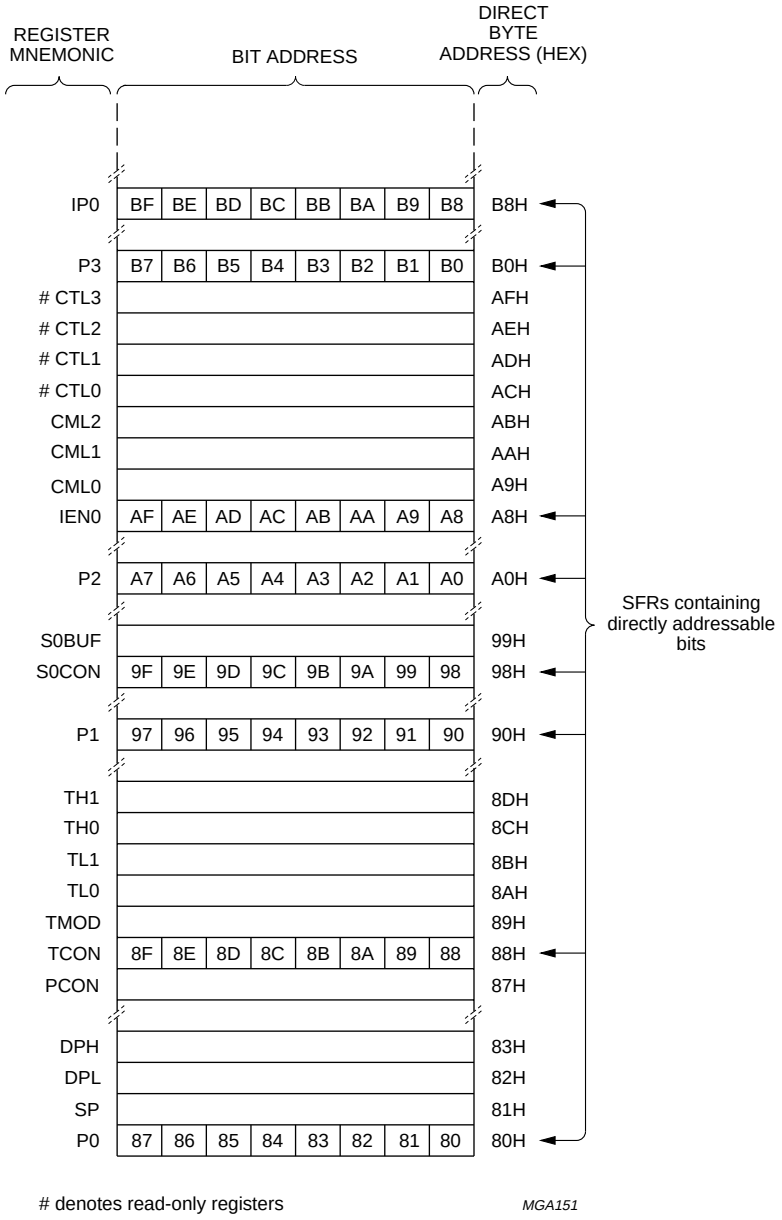


Fig.6 Special Function Register memory map (continued).

10 PULSE WIDTH MODULATED OUTPUTS

Two pulse width modulated output channels are provided with the P8xC562. These channels output pulses of programmable length and interval. The repetition frequency is defined by an 8-bit prescaler PWMP which generates the clock for the counter. Both the prescaler and counter are common to both PWM channels. The 8-bit counter counts modulo 255 i.e. from 0 to 254 inclusive. The value of the 8-bit counter is compared to the contents of two registers: PWM0 and PWM1.

Provided the contents of either of these registers is greater than the counter value, the output of $\overline{PWM0}$ or $\overline{PWM1}$ is set LOW. If the contents of these registers are equal to, or less than the counter value, the output will be HIGH. The pulse width ratio is therefore defined by the contents of the registers PWM0 and PWM1.

The pulse width ratio is in the range of 0 to 255/255 and may be programmed in increments of 1/255.

The repetition frequency f_{PWM}, at the $\overline{PWMn}$ outputs is given by: $f_{PWM} = \frac{f_{OSC}}{2 \times (1 + PWMP) \times 255}$

When using an oscillator frequency of 16 MHz for example, the above formula would give a repetition frequency range of 123 Hz to 31.4 kHz.

By loading the PWM registers with either 00H or FFH, the PWM outputs can be retained at a constant HIGH or LOW level respectively. When loading FFH to the PWM registers, the 8-bit counter will never actually reach this value. Both $\overline{PWMn}$ output pins are driven by push-pull drivers, and are not shared with any other function.

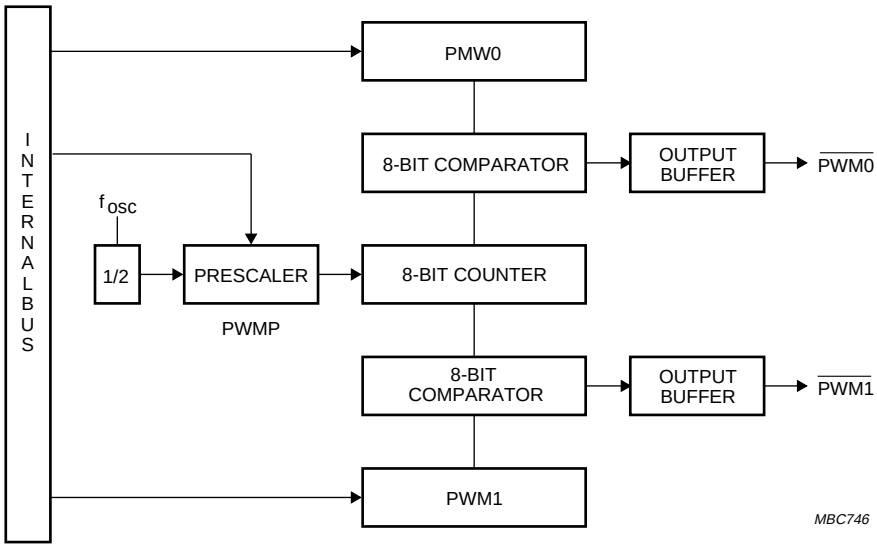


Fig.8 Functional diagram of Pulse Width Modulated outputs.

12.2.4 SET ENABLE REGISTER (STE)

Table 20 Set Enable Register (SFR address EEH)

7	6	5	4	3	2	1	0
TG47	TG46	SP45	SP44	SP43	SP42	SP41	SP40

Table 21 Description of STE bits (see notes 1 and 2)

BIT	SYMBOL	DESCRIPTION
7	TG47	If HIGH then P4.7 is reset on the next toggle, if LOW P4.7 is set on the next toggle.
6	TG46	If HIGH then P4.6 is reset on the next toggle, if LOW P4.6 is set on the next toggle.
5	SP45	If HIGH the P4.5 is set on a match of CM0 and T2.
4	SP44	If HIGH the P4.4 is set on a match of CM0 and T2.
3	SP43	If HIGH the P4.3 is set on a match of CM0 and T2.
2	SP42	If HIGH the P4.2 is set on a match of CM0 and T2.
1	SP41	If HIGH the P4.1 is set on a match of CM0 and T2.
0	SP40	If HIGH the P4.0 is set on a match of CM0 and T2.

Notes

1. If STE.n is LOW then P4.n is not affected by a match of CM0 and T2 (n = 0 to 5).
2. STE.6 and STE.7 are read only.

12.2.5 RESET/TOGGLE ENABLE REGISTER (RTE)

Table 22 Reset/toggle enable register (SFR address EFH)

7	6	5	4	3	2	1	0
TP47	TP46	RP45	RP44	RP43	RP42	RP41	RP40

Table 23 Description of RTE bits (note 1)

BIT	SYMBOL	DESCRIPTION
7	TP47	If HIGH then P4.7 toggles on a match of CM2 and T2.
6	TP46	If HIGH then P4.6 toggles on a match of CM2 and T2.
5	RP45	If HIGH then P4.5 is reset on a match of CM1 and T2.
4	RP44	If HIGH then P4.4 is reset on a match of CM1 and T2.
3	RP43	If HIGH then P4.3 is reset on a match of CM1 and T2.
2	RP42	If HIGH then P4.2 is reset on a match of CM1 and T2.
1	RP41	If HIGH then P4.1 is reset on a match of CM1 and T2.
0	RP40	If HIGH then P4.0 is reset on a match of CM1 and T2.

Note

1. If RTE.n is LOW then P4.n is not affected by a match of CM1 and T2 or CM2 and T2. For more information, refer to the 8051-based *"8-bit Microcontrollers Data Handbook IC20"*.

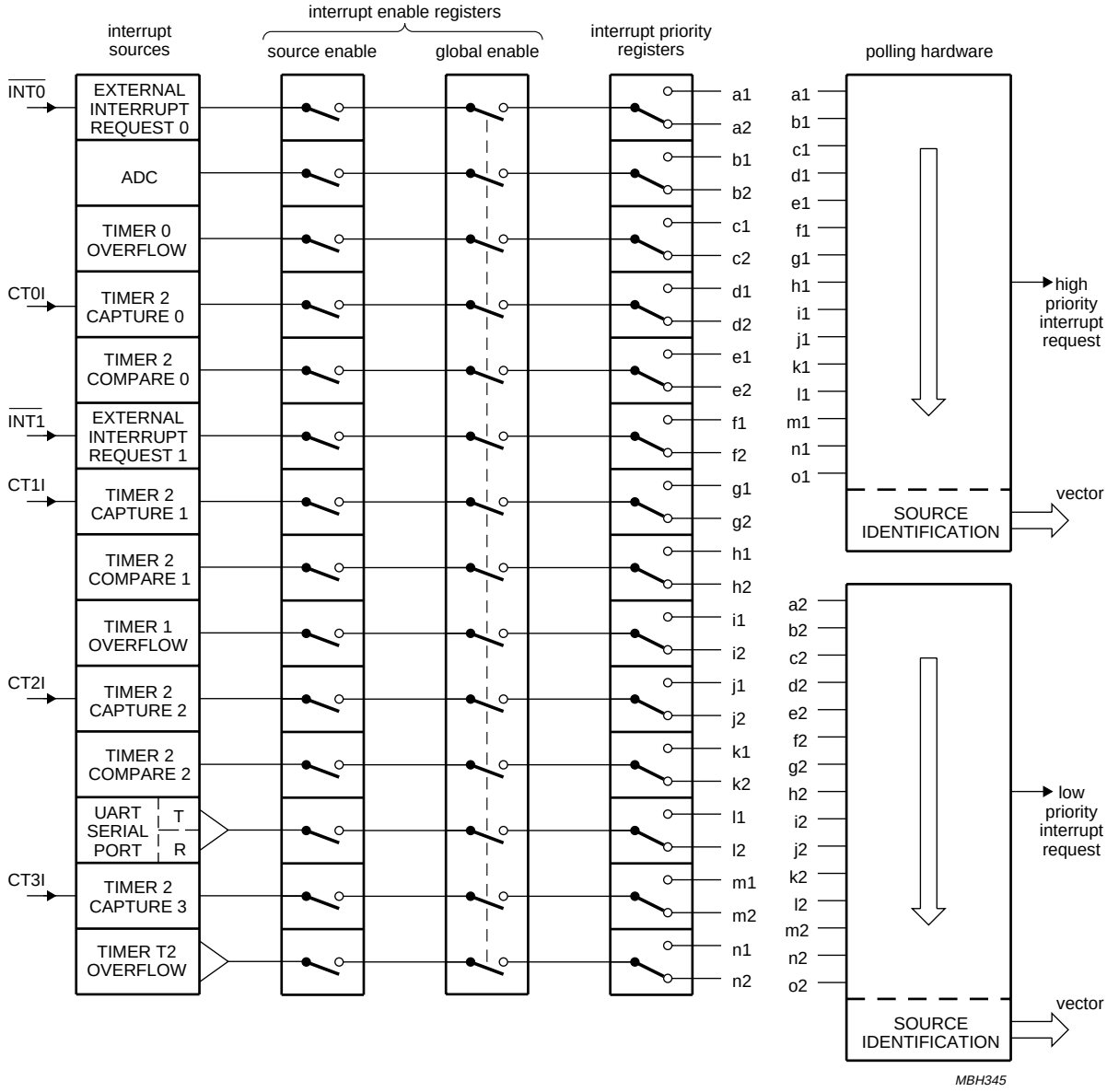


Fig.12 Interrupt system.

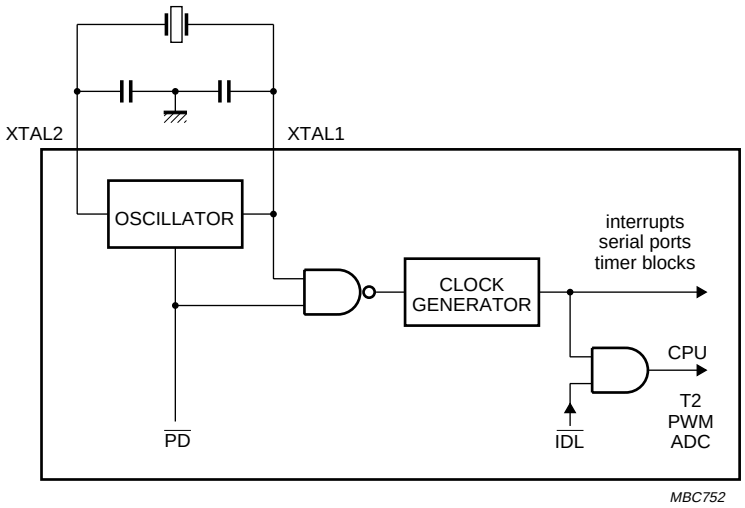


Fig.13 Internal Idle and Power-down clock configuration.

15.2 Power Control Register (PCON)

The reduced power modes are activated by software using this register. PCON is not bit addressable.

Table 34 Power Control Register (SFR address 87H)

7	6	5	4	3	2	1	0
SMOD	–	RFI	WLE	GF1	GF0	PD	IDL

Table 35 Description of PCON bits (note 1)

BIT	SYMBOL	DESCRIPTION
7	SMOD	**Double Baud rate.** When set to logic 1 the baud rate is doubled when the serial port SIO0 is being used in modes 1, 2 or 3.
6	–	Reserved.
5	RFI	**Reduced radio frequency interference.** When set to logic 1, the toggling of the ALE pin is prohibited; this bit is cleared on RESET (see Table 1).
4	WLE	**Watchdog Load Enable.** This flag must be set by software prior to loading the Watchdog Timer. It is cleared when the timer is loaded.
3	GF1	**General-purpose flag bits.**
2	GF0	
1	PD	**Power-down bit.** Setting this bit activates the Power-down mode. It can only be set if input $\overline{EW}$ is HIGH.
0	IDL	**Idle mode.** Setting this bit activates the Idle mode.

Note

1. If logic 1s are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is (0X000000).

Table 36 State of internal registers after an internal reset
X = undefined state.

REGISTER	7	6	5	4	3	2	1	0
ACC	0	0	0	0	0	0	0	0
ADC0N	X	X	0	0	0	0	0	0
ADCH	X	X	X	X	X	X	X	X
B	0	0	0	0	0	0	0	0
CML0 to CML2	0	0	0	0	0	0	0	0
CMH0 to CMH2	0	0	0	0	0	0	0	0
CTCON	0	0	0	0	0	0	0	0
CTL0 to CTL3	X	X	X	X	X	X	X	X
CTH0 to CTH3	X	X	X	X	X	X	X	X
DPL	0	0	0	0	0	0	0	0
DPH	0	0	0	0	0	0	0	0
IEN0	0	0	0	0	0	0	0	0
IEN1	0	0	0	0	0	0	0	0
IP0	X	0	0	0	0	0	0	0
IP1	0	0	0	0	0	0	0	0
PCH	0	0	0	0	0	0	0	0
PCL	0	0	0	0	0	0	0	0
PCON	0	X	0	0	0	0	0	0
PSW	0	0	0	0	0	0	0	0
PWM0	0	0	0	0	0	0	0	0
PWM1	0	0	0	0	0	0	0	0
PWMP	0	0	0	0	0	0	0	0
P0 to P4	1	1	1	1	1	1	1	1
P5	X	X	X	X	X	X	X	X
RTE	0	0	0	0	0	0	0	0
SBUF	X	X	X	X	X	X	X	X
SCON	0	0	0	0	0	0	0	0
SP	0	0	0	0	0	1	1	1
STE	1	1	0	0	0	0	0	0
TCON	0	0	0	0	0	0	0	0
TH0, TH1	0	0	0	0	0	0	0	0
TMH2	0	0	0	0	0	0	0	0
TL0, TL1	0	0	0	0	0	0	0	0
TML2	0	0	0	0	0	0	0	0
TMOD	0	0	0	0	0	0	0	0
TM2CON	0	0	0	0	0	0	0	0
TM2IR	0	0	0	0	0	0	0	0
T3	0	0	0	0	0	0	0	0

17.1 Power-on-reset

When V_{DD} is turned on, and provided its rise-time does not exceed 10 ms, an automatic reset can be obtained by connecting the RST pin to V_{DD} via a 2.2 µF capacitor. When the power is switched on, the voltage on the RST pin, is equal to V_{DD} minus the capacitor voltage, and decreases from V_{DD} as the capacitor charges through the internal resistor (R_{RST}) to ground. The larger the capacitor, the more slowly V_{RST} decreases. V_{RST} must remain above the lower threshold of the Schmitt trigger long enough to effect a complete reset. The time required is the oscillator start-up time, plus 2 machine cycles. The port pins will be in a random state until the oscillator has started and the internal reset algorithm has written logic 1s to the port pins. The Power-on-reset circuitry is shown in Fig.17.

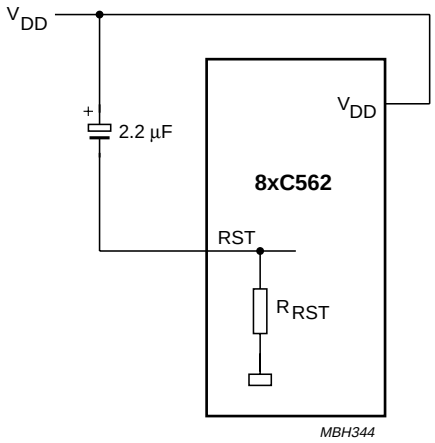


Fig.17 Power-on-reset.

18 INSTRUCTION SET

The P8xC562 uses the powerful instruction set of the 80C51. Additional Special Function Registers are incorporated to control the on-chip peripherals. The instruction set consists of 49 single-byte, 45 two-byte and 17 three-byte instructions. When using a 16 MHz oscillator, 64 instructions execute in 0.75 μs and 45 instructions execute in 1.5 μs. Multiply and divide instructions execute in 3 μs.

Tables 37 to 41 describe the Instruction set; Table 42 explains the Data addressing modes and the Hexadecimal opcodes.

Table 37 Instruction set descriptions: Arithmetic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Arithmetic operations					
ADD	A,Rr	Add register to A	1	1	2*
ADD	A,direct	Add direct byte to A	2	1	25
ADD	A,@Ri	Add indirect RAM to A	1	1	26, 27
ADD	A,#data	Add immediate data to A	2	1	24
ADDC	A,Rr	Add register to A with carry flag	1	1	3*
ADDC	A,direct	Add direct byte to A with carry flag	2	1	35
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1	36, 37
ADDC	A,#data	Add immediate data to A with carry flag	2	1	34
SUBB	A,Rr	Subtract register from A with borrow	1	1	9*
SUBB	A,direct	Subtract direct byte from A with borrow	2	1	95
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1	96, 97
SUBB	A,#data	Subtract immediate data from A with borrow	2	1	94
INC	A	Increment A	1	1	04
INC	Rr	Increment register	1	1	0*
INC	direct	Increment direct byte	2	1	05
INC	@Ri	Increment indirect RAM	1	1	06, 07
DEC	A	Decrement A	1	1	14
DEC	Rr	Decrement register	1	1	1*
DEC	direct	Decrement direct byte	2	1	15
DEC	@Ri	Decrement indirect RAM	1	1	16, 17
INC	DPTR	Increment data pointer	1	2	A3
MUL	AB	Multiply A & B	1	4	A4
DIV	AB	Divide A by B	1	4	84
DA	A	Decimal adjust A	1	1	D4

Table 43 Instruction map

First hexadecimal character of opcode ↓	← Second hexadecimal character of opcode → 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	AJMP addr11	LJMP addr16	RR A	INC A	INC direct	INC @Ri 0	INC @Ri 1	INC Rr 0	INC Rr 1	INC Rr 2	INC Rr 3	INC Rr 4	INC Rr 5	INC Rr 6	INC Rr 7
1	JBC bit,rel	ACALL addr11	LCALL addr16	RRC A	DEC A	DEC direct	DEC @Ri 0	DEC @Ri 1	DEC Rr 0	DEC Rr 1	DEC Rr 2	DEC Rr 3	DEC Rr 4	DEC Rr 5	DEC Rr 6	DEC Rr 7
2	JB bit,rel	AJMP addr11	RET	RL A	ADD A,#data	ADD A,direct	ADD A,@Ri 0	ADD A,@Ri 1	ADD A,Rr 0	ADD A,Rr 1	ADD A,Rr 2	ADD A,Rr 3	ADD A,Rr 4	ADD A,Rr 5	ADD A,Rr 6	ADD A,Rr 7
3	JNB bit,rel	ACALL addr11	RETI	RLC A	ADDC A,#data	ADDC A,direct	ADDC A,@Ri 0	ADDC A,@Ri 1	ADDC A,Rr 0	ADDC A,Rr 1	ADDC A,Rr 2	ADDC A,Rr 3	ADDC A,Rr 4	ADDC A,Rr 5	ADDC A,Rr 6	ADDC A,Rr 7
4	JC rel	AJMP addr11	ORL direct,A	ORL direct,#data	ORL A,#data	ORL A,direct	ORL A,@Ri 0	ORL A,@Ri 1	ORL A,Rr 0	ORL A,Rr 1	ORL A,Rr 2	ORL A,Rr 3	ORL A,Rr 4	ORL A,Rr 5	ORL A,Rr 6	ORL A,Rr 7
5	JNC rel	ACALL addr11	ANL direct,A	ANL direct,#data	ANL A,#data	ANL A,direct	ANL A,@Ri 0	ANL A,@Ri 1	ANL A,Rr 0	ANL A,Rr 1	ANL A,Rr 2	ANL A,Rr 3	ANL A,Rr 4	ANL A,Rr 5	ANL A,Rr 6	ANL A,Rr 7
6	JZ rel	AJMP addr11	XRL direct,A	XRL direct,#data	XRL A,#data	XRL A,direct	XRL A,@Ri 0	XRL A,@Ri 1	XRL A,Rr 0	XRL A,Rr 1	XRL A,Rr 2	XRL A,Rr 3	XRL A,Rr 4	XRL A,Rr 5	XRL A,Rr 6	XRL A,Rr 7
7	JNZ rel	ACALL addr11	ORL C,bit	JMP @A+DPTR	MOV A,#data	MOV direct,#data	MOV @Ri,#data 0	MOV @Ri,#data 1	MOV Rr,#data 0	MOV Rr,#data 1	MOV Rr,#data 2	MOV Rr,#data 3	MOV Rr,#data 4	MOV Rr,#data 5	MOV Rr,#data 6	MOV Rr,#data 7
8	SJMP rel	AJMP addr11	ANL C,bit	MOVC A,@A+PC	DIV AB	MOV direct,direct	MOV direct,@Ri 0	MOV direct,@Ri 1	MOV direct,Rr 0	MOV direct,Rr 1	MOV direct,Rr 2	MOV direct,Rr 3	MOV direct,Rr 4	MOV direct,Rr 5	MOV direct,Rr 6	MOV direct,Rr 7
9	MOV DTPR,#data16	ACALL addr11	MOV bit,C	MOVC A,@A+DPTR	SUBB A,#data	SUBB A,direct	SUBB A,@Ri 0	SUBB A,@Ri 1	SUB A,Rr 0	SUB A,Rr 1	SUB A,Rr 2	SUB A,Rr 3	SUB A,Rr 4	SUB A,Rr 5	SUB A,Rr 6	SUB A,Rr 7
A	ORL C,/bit	AJMP addr11	MOV bit,C	INC DPTR	MUL AB		MOV @Ri,direct 0	MOV @Ri,direct 1	MOV Rr,direct 0	MOV Rr,direct 1	MOV Rr,direct 2	MOV Rr,direct 3	MOV Rr,direct 4	MOV Rr,direct 5	MOV Rr,direct 6	MOV Rr,direct 7
B	ANL C,/bit	ACALL addr11	CPL bit	CPL C	CJNE A,#data,rel	CJNE A,direct,rel	CJNE @Ri,#data,rel 0	CJNE @Ri,#data,rel 1	CJNE Rr,#data,rel 0	CJNE Rr,#data,rel 1	CJNE Rr,#data,rel 2	CJNE Rr,#data,rel 3	CJNE Rr,#data,rel 4	CJNE Rr,#data,rel 5	CJNE Rr,#data,rel 6	CJNE Rr,#data,rel 7
C	PUSH direct	AJMP addr11	CLR bit	CLR C	SWAP A	XCH A,direct	XCH A,@Ri 0	XCH A,@Ri 1	XCH A,Rr 0	XCH A,Rr 1	XCH A,Rr 2	XCH A,Rr 3	XCH A,Rr 4	XCH A,Rr 5	XCH A,Rr 6	XCH A,Rr 7
D	POP direct	ACALL addr11	SETB bit	SETB C	DA A	DJNZ direct,rel	XCHD A,@Ri 0	XCHD A,@Ri 1	DJNZ Rr,rel 0	DJNZ Rr,rel 1	DJNZ Rr,rel 2	DJNZ Rr,rel 3	DJNZ Rr,rel 4	DJNZ Rr,rel 5	DJNZ Rr,rel 6	DJNZ Rr,rel 7
E	MOVX A,@DTPR	AJMP addr11	MOVX A,@Ri 0	MOVX A,@Ri 1	CLR A	MOV A,direct (1)	MOV A,@Ri 0	MOV A,@Ri 1	MOV A,Rr 0	MOV A,Rr 1	MOV A,Rr 2	MOV A,Rr 3	MOV A,Rr 4	MOV A,Rr 5	MOV A,Rr 6	MOV A,Rr 7
F	MOVX @DTPR,A	ACALL addr11	MOVX @Ri,A 0	MOVX @Ri,A 1	CPL A	MOV direct,A	MOV @Ri,A 0	MOV @Ri,A 1	MOV Rr,A 0	MOV Rr,A 1	MOV Rr,A 2	MOV Rr,A 3	MOV Rr,A 4	MOV Rr,A 5	MOV Rr,A 6	MOV Rr,A 7

Note

1. MOV A, ACC is not a valid instruction.

19 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_I	input voltage on any pin with respect to ground (V_{SS})	–0.5	+6.5	V
I_I, I_O	input, output DC current on any single I/O pin	–	5.0	mA
P_{tot}	total power dissipation	–	1.0	W
T_{stg}	storage temperature range	–65	+150	°C
T_{amb}	operating ambient temperature range			
	P8xC562EBx	0	+70	°C
	P8xC562EFx	–40	+85	°C
	P8xC562EHx	–40	+125	°C

20 DC CHARACTERISTICS

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; f_{OSC} = 16 MHz.
T_{amb} = –40 to +85 °C for the **P8xC562EFx**.

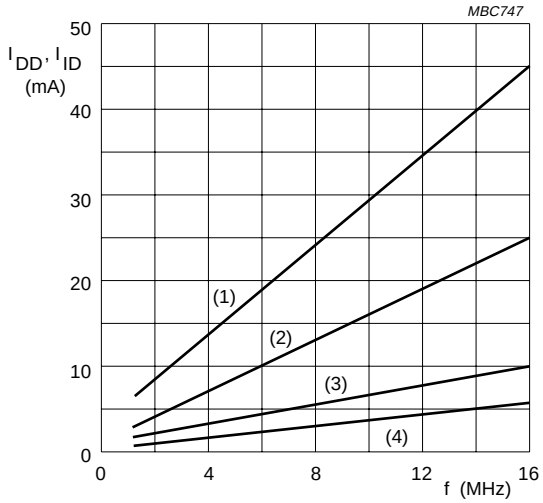
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supply (digital part)					
V_{DD}	supply voltage P8xC562Exx		4.5	5.5	V
I_{DD}	operating supply current	note 1			
	P8xC562Exx		–	40	mA
$I_{DD(ID)}$	supply current Idle mode	note 2			
	P8xC562Exx		–	9	mA
$I_{DD(PD)}$	supply current Power-down mode	note 3			
	P8X562EBx	$2\ V < V_{DD(PD)} < V_{DD(max)}$	–	50	µA
	P8X562EFx	$2\ V < V_{DD(PD)} < V_{DD(max)}$	–	50	µA
	P8X562EHx	$2\ V < V_{DD(PD)} < V_{DD(max)}$	–	150	µA
Inputs					
V_{IL}	LOW level input voltage (except $\overline{EA}$)		–0.5	$0.2V_{DD} - 0.1$	V
V_{IL1}	LOW level input voltage ($\overline{EA}$)		–0.5	$0.2V_{DD} - 0.3$	V
V_{IH}	HIGH level input voltage (except RST, XTAL1)		$0.2V_{DD} + 0.9$	$V_{DD} + 0.5$	V
V_{IH1}	HIGH level input voltage (RST and XTAL1)		$0.7V_{DD}$	$V_{DD} + 0.5$	V
I_{IL}	input current logic 0 Ports 1, 2, 3 and 4; (except P1.6/SCL, P1.7/SDA)	V_I = 0.45 V	–	–50	µA
I_{TL}	input current HIGH-to-LOW transition (Ports 1, 2, 3 and 4)	V_I = 2.0 V	–	–650	µA
I_{LI1}	input leakage current (Port 0, $\overline{EA}$, STADC, $\overline{EW}$)	$0.45\ V < V_I < V_{DD}$	–	±10	µA
I_{LI3}	input leakage current (Port 5)	$0.45\ V < V_I < V_{DD}$	–	±1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Outputs					
V_{OL}	LOW level output voltage (Ports 1, 2, 3 and 4)	I_{OL} = 1.6 mA; note 4	–	0.45	V
V_{OL1}	LOW level output voltage (Port 0, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$)	I_{OL} = 3.2 mA; note 4	–	0.45	V
V_{OH}	HIGH level output voltage Ports 1, 2, 3 and 4	I_{OH} = −60 µA	2.4	–	V
		I_{OH} = −25 µA	$0.75V_{DD}$	–	V
		I_{OH} = −10 µA	$0.9V_{DD}$	–	V
V_{OH1}	HIGH level output voltage Port 0 in external bus mode, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$; note 5	I_{OH} = −800 µA	2.4	–	V
		I_{OH} = −300 µA	$0.75V_{DD}$	–	V
		I_{OH} = −80 µA	$0.9V_{DD}$	–	V
V_{OH2}	HIGH level output voltage (RST)	I_{OH} = −400 µA	2.4	–	V
		I_{OH} = −120 µA	$0.8V_{DD}$	–	V
R_{RST}	RST pull-down resistor		50	150	kΩ
$C_{I/O}$	capacitance of I/O buffer	test frequency = 1 MHz; T_{amb} = 25 °C	–	10	pF
Supply (analog part)					
V_{DDA}	supply voltage P8X562Exx	$V_{DDA} = V_{DD} \pm 0.2$ V	4.5	5.5	V
I_{DDA}	supply current operating	Port 5 = 0 to V_{DDA}		1.2	mA
$I_{DDA(ID)}$	supply current Idle mode				
	P8X562EBx		–	50	µA
	P8X562EFx		–	50	µA
	P8X562EHx		–	100	µA
$I_{DDA(PD)}$	supply current Power-down mode	$2\text{ V} < V_{DDA(PD)} < V_{DDA(max)}$			
	P8X562EBx		–	50	µA
	P8X562EFx		–	50	µA
	P8X562EHx		–	100	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Analog inputs					
V_{IN}	analog input voltage		AV_{SS} – 0.2	AV_{DD} + 0.2	V
V_{REF+}	reference voltage (+)		–	AV_{DD} + 0.2	V
V_{REF-}	reference voltage (–)		AV_{SS} – 0.2	–	V
R_{REF}	resistance between V_{REF+} and V_{REF-}		5	25	kΩ
C_{IA}	analog input capacitance		–	15	pF
t_{ADS}	sampling time		–	$6t_{CY}$	µs
t_{ADC}	conversion time (including sample time)		–	$24t_{CY}$	µs
DL_e	differential non-linearity	notes 7 and 11	–	±1	LSB
IL_e	integral non-linearity	notes 6 and 8	–	±1	LSB
OS_e	offset error	notes 6 and 10	–	±1	LSB
G_e	gain error	notes 6 and 9	–	±0.4	%
M_{ctc}	channel-to-channel matching		–	±1	LSB
C_t	crosstalk between P5 inputs	0 to 100 kHz	–	–60	dB

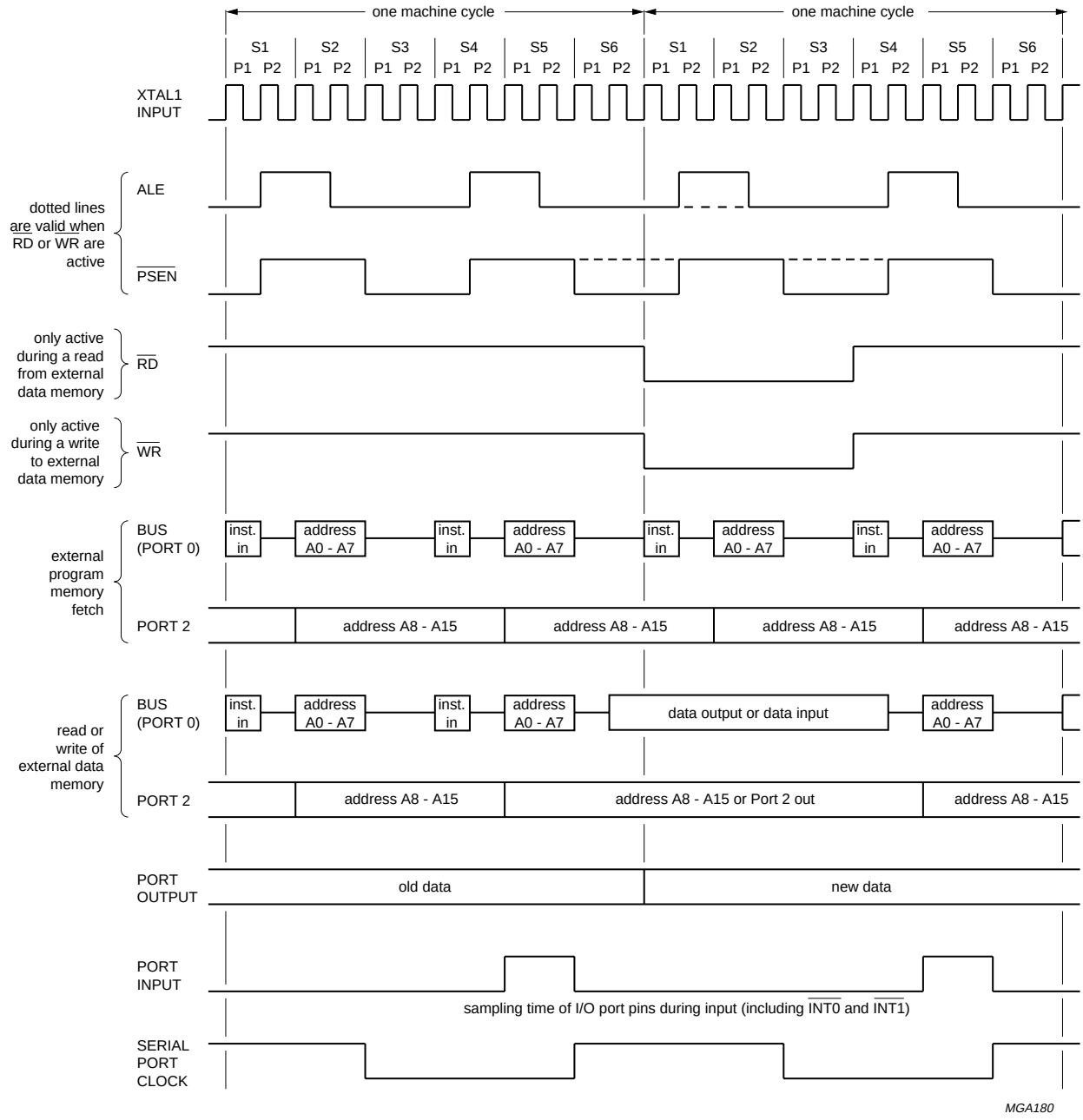
Notes to the DC characteristics

1. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 10$ ns; $V_{IL} = V_{SS} + 0.5$ V; $V_{IH} = V_{DD} - 0.5$ V; XTAL2 not connected; $\overline{EA}$ = RST = Port 0 = $\overline{EW}$ = V_{DD}; STADC = V_{SS}.
2. The Idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 10$ ns; $V_{IL} = V_{SS} + 0.5$ V; $V_{IH} = V_{DD} - 0.5$ V; XTAL2 not connected; $\overline{EA}$ = Port 0 = $\overline{EW}$ = V_{DD}; RST = STADC = V_{SS}.
3. The Power-down current is measured with all output pins disconnected; XTAL2 not connected; $\overline{EA}$ = Port 0 = $\overline{EW}$ = V_{DD}; RST = STADC = XTAL1 = V_{SS}.
4. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the low level output voltage of ALE and Ports 1, 3 and 4. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make HIGH-to-LOW transitions during bus operations. In the most adverse condition (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8 V. In such events it may be required to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger strobe input.
5. Capacitive loading on Ports 0 and 2 may cause the high level output voltage on ALE and $\overline{PSEN}$ to momentarily fall below to $0.9V_{DD}$ specification when the address bits are stabilizing.
6. $V_{REF+} = 5.12$ V; $V_{REF-} = 0$ V; $V_{DDA} = 5.0$ V.
7. The differential non-linearity (DL_e) is the difference between the actual step width and the ideal step width.
8. The integral non-linearity (IL_e) is the peak difference between the centre of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset error.
9. The gain error (G_e) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. Gain error is constant at every point on the transfer curve.
10. The offset error (OS_e) is the absolute difference between the straight line which fits the actual transfer curve after removing gain error, and a straight line which fits the ideal transfer curve. The offset error is constant at every point of the actual transfer curve.
11. $V_{REF-} = 0$ V; $V_{DDA} = 5$ V; $V_{REF+} = 5.12$ V. The ADC is monotonic with no missing codes. Measurement by continuously increasing V_{IN} from –20 mV to 5.12 V in increments of 2 mV.



(1) $I_{DD(max)}$ operating mode; V_{DD} = 5.5 V.
(2) $I_{DD(max)}$ operating mode; V_{DD} = 4.5 V.
(3) $I_{ID(max)}$ Idle mode; V_{DD} = 5.5V.
(4) $I_{ID(max)}$ Idle mode; V_{DD} = 4.5 V.
These values are valid within the specified frequency range.

Fig.18 Supply current (I_{DD}, I_{ID}) as a function of frequency at XTAL1 (f_{osc}).



The Port 5 input buffers have a maximum propagation delay of 300 ns. As a result Port 5 sample time starts 300 ns in advance of state S5 and ends when S5 has finished.

Fig.21 Instruction cycle timing.

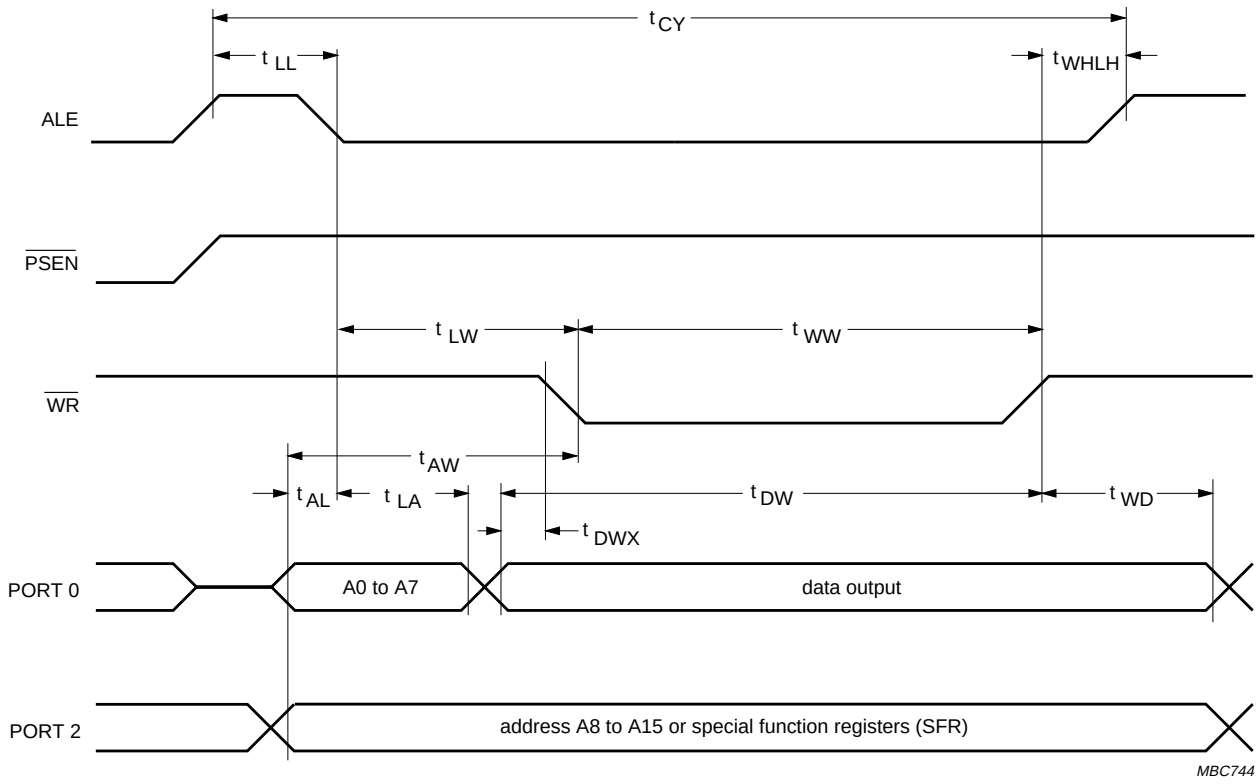


Fig.24 Write to data memory.

23 SOLDERING

23.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

23.2 Reflow soldering

Reflow soldering techniques are suitable for all PLCC packages.

The choice of heating method may be influenced by larger PLCC packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

23.3 Wave soldering

Wave soldering techniques can be used for all PLCC packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

23.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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