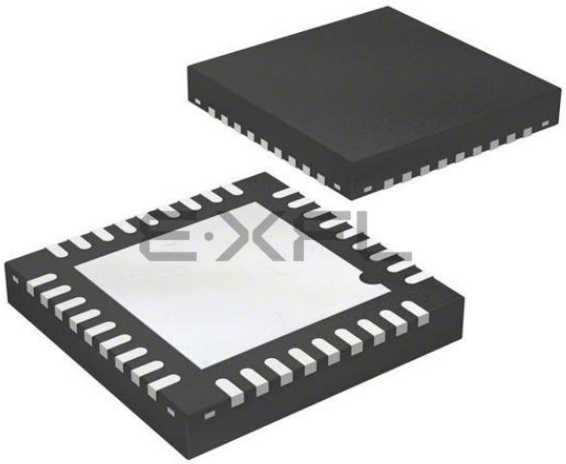

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	I²C, SPI
Clock Rate	18.6MHz
Non-Volatile Memory	-
On-Chip RAM	54kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFQFN Exposed Pad
Supplier Device Package	36-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/akm-semiconductor/ak7755en

6. Absolute Maximum Ratings

(AVSS=DVSS=0V; Note 2)

Parameter	Symbol	min	max	Unit
Power Supplies				
Analog	AVDD	-0.3	4.3	V
Digital1(I/F)	TVDD	-0.3	4.3	V
Digital2(Core)	DVDD	-0.3	1.6	V
DVSS-AVSS (Note 2)	ΔGND	-0.3	0.3	V
Input Current, Any Pin Except Supplies	IIN	—	±10	mA
Analog Input Voltage (Note 3)	VINA	-0.3	(AVDD+0.3)≤4.3	V
Digital Input Voltage (Note 4)	VIND	-0.3	(TVDD+0.3)≤4.3	V
Ambient Temperature	Ta	-40	85	℃
Storage Temperature	Tstg	-65	150	℃

Note 2. All voltages with respect to ground. AVSS and DVSS must be the same voltage.
Note 3. The maximum analog input voltage is smaller value between (AVDD+0.3)V and 4.3V.
Note 4. The maximum digital input voltage is smaller value between (DVDD+0.3)V and 4.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSS=DVSS=0V; Note 2)

Parameter	Symbol	min	typ	max	Unit
Power Supplies					
Analog	AVDD	3.0	3.3	3.6	V
Digital1(I/F)	TVDD	1.7	3.3	3.6	V
Digital2(Core)	DVDD	1.14	1.2	1.3	V

Note 5. AVDD and TVDD must be powered up first before DVDD when DVDD is supplied externally (LDOE pin = "L"). In this case, the power-up sequence between AVDD and TVDD is not critical. When using the internal regulator (LDOE pin = "H"), the power-up sequence between AVDD and TVDD is not critical. But all power supplies must be ON before starting operation of the AK7755 by PDN pin = "H".
Note 6. Do not turn off the power supply of the AK7755 with the power supply of the surrounding device turned on. Pull-up of SDA and SCL pins must not exceed TVDD.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

8. Electrical Characteristics

■ Analog Characteristics

1. MIC Amplifier Gain

(Ta= 25°C; AVDD=TVDD=3.3V; DVDD=1.2V; AVSS=DVSS=0V)

	Parameter		min	typ	max	Unit
MIC AMP	Input Impedance		14	20		kΩ
	Gain	MGNL[3:0]bits=0h, MGNR[3:0]bits=0h		0		dB
		MGNL[3:0]bits=1h, MGNR[3:0]bits=1h		2		dB
		MGNL[3:0]bits=2h, MGNR[3:0]bits=2h		4		dB
		MGNL[3:0]bits=3h, MGNR[3:0]bits=3h		6		dB
		MGNL[3:0]bits=4h, MGNR[3:0]bits=4h		8		dB
		MGNL[3:0]bits=5h, MGNR[3:0]bits=5h		10		dB
		MGNL[3:0]bits=6h, MGNR[3:0]bits=6h		12		dB
		MGNL[3:0]bits=7h, MGNR[3:0]bits=7h		14		dB
		MGNL[3:0]bits=8h, MGNR[3:0]bits=8h		16		dB
		MGNL[3:0]bits=9h, MGNR[3:0]bits=9h		18		dB
		MGNL[3:0]bits=Ah, MGNR[3:0]bits=Ah		21		dB
		MGNL[3:0]bits=Bh, MGNR[3:0]bits=Bh		24		dB
		MGNL[3:0]bits=Ch, MGNR[3:0]bits=Ch		27		dB
		MGNL[3:0]bits=Dh, MGNR[3:0]bits=Dh		30		dB
		MGNL[3:0]bits=Eh, MGNR[3:0]bits=Eh		33		dB
		MGNL[3:0]bits=Fh, MGNR[3:0]bits=Fh		36		dB

2. Line-in Amplifier Gain

(Ta= 25°C; AVDD=TVDD=3.3V; DVDD=1.2V; AVSS=DVSS=0V)

	Parameter		min	typ	max	Unit
Line-in AMP	Input Impedance		14	20		kΩ
	Gain (Note 7)	LIGN[3:0]bits=0h		0		dB
		LIGN[3:0]bits=1h		-3		dB
		LIGN[3:0]bits=2h		-6		dB
		LIGN[3:0]bits=3h		-9		dB
		LIGN[3:0]bits=4h		-12		dB
		LIGN[3:0]bits=5h		-15		dB
		LIGN[3:0]bits=6h		-18		dB
		LIGN[3:0]bits=7h		-21		dB
		LIGN[3:0]bits=8h		N/A		dB
		LIGN[3:0]bits=9h		+3		dB
		LIGN[3:0]bits=Ah		+6		dB
		LIGN[3:0]bits=Bh		+9		dB
		LIGN[3:0]bits=Ch		+12		dB
		LIGN[3:0]bits=Dh		+15		dB
		LIGN[3:0]bits=Eh		+18		dB
		LIGN[3:0]bits=Fh		+21		dB

Note 7. If the output signal of line-in amplifier is input to the analog mixer, +18dB gain is added to the signal at the mixer.

■ DC Characteristics

(Ta= -40 to 85°C, AVDD=3.3V, DVDD=1.2V, TVDD=1.7 to 3.6V, AVSS=DVSS=0V)

Parameter		Symbol	min	typ	max	Unit
High Level Input Voltage		VIH	80%TVDD			V
Low Level Input Voltage		VIL			20%TVDD	V
SCL, SDA High Level Input Voltage		VIH	70%TVDD			V
SCL, SDA Low Level Input Voltage		VIL			30%TVDD	V
DMDAT1, DMDAT2 High Level Input Voltage (DMIC1, DMIC2 bit = "1")		VIH2	65%AVDD			V
DMDAT1, DMDAT2 Low Level Input Voltage (DMIC1, DMIC2 bit = "1")		VIL2			35%AVDD	V
High Level Output Voltage Iout= -100μA (Note 21)		VOH	TVDD-0.3			V
Low Level Output Voltage Iout=100μA (Note 22)		VOL			0.3	V
SDA Low Level Output Voltage Iout=3mA	TVDD≥2.0V	VOL			0.4	V
	TVDD<2.0V	VOL			20%TVDD	
DMCLK1, DMCLK2 High Level Output Voltage Iout = -80μA (DMIC1, DMIC2 bit = "1")		VOH2	AVDD-0.4			V
DMCLK1, DMCLK2 Low Level Output Voltage Iout = 80μA (DMIC1, DMIC2 bit = "1")		VOL2			0.4	V
Input Leak Current (Note 23)		Iin			±10	μA
Input Leak Current at Pulled-down Pins (Note 24)		Iid		77		μA
Input Leak Current at XTI pin		lix		17		μA

Note 21. Except XTO pin
Note 22. Except SDA and XTO pins.
Note 23. Internal Pulled-down pins, except the XTI pin
Note 24. The LRCK, BICK, SDOUT2/JX3/MAT0 and SDOUT3/JX2/MAT1 pins are internal pulled-down pins (typ. 43 kΩ@3.3V).

■ Power Consumptions

(Ta=25°C, AVDD=3.0 to 3.6V (typ=3.3V, max=3.6V), TVDD=1.7 to 3.6V (typ=3.3V, max=3.6V), DVDD=1.14 to 1.3V (typ=1.2V, max=1.3V), AVSS=DVSS=0V)

	Parameter	min	typ	max	Unit
Power consumptions in operation 1 (Note 25) (LDOE pin = "L")	AVDD		16	24	mA
	TVDD		3	4.5	mA
	DVDD		25	40	mA
Power consumptions in operation 2 (Note 25) (LDOE pin = "H")	AVDD		48	72	mA
	TVDD		3	4.5	mA
Power consumptions in power-down (PDN pin= "L", LDOE pin = "L")	AVDD		10		uA
	TVDD		10		uA
	DVDD		200		uA
Power consumptions in power-down (PDN pin= "L", LDOE pin = "H")	AVDD		1		uA
	TVDD		1		uA

Note 25. DVDD power consumption will be changed depending on DSP programs.
(e.g. It will be 6mA when using AKM's Hands Free program.)

4. SPI Interface

4-1. Clock Reset (CKRESTN bit = "0")

(Ta= -40 to 85°C; AVDD=3.0 to 3.6V, TVDD=1.7 to 3.6V, DVDD=1.14 to 1.3V, AVSS=DVSS=0V, CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Microcontroller Interface Signal					
SCLK Frequency	fSCLK			3.5	MHz
SCLK Low Level Width	tSCLKL	120			ns
SCLK High Level Width	tSCLKH	120			ns
Microcontroller → AK7755					
CSN High Level Width	tWRQH	300			ns
Time from CSN "↑" to PDN "↑"	tRST	360			ns
Time from PDN"↑" to CSN "↓"	tIRRQ	1			ms
Time from RQN"↓" to SCLK"↓"	tWSC	360			ns
Time from SCLK"↑" to CSN"↑"	tSCW	480			ns
SI Latch Setup Time	tSIS	120			ns
SI Latch Hold Time	tSIH	120			ns
AK7755 → Microcontroller					
SO Output Delay Time from SCLK "↓"	tSOS			120	ns
SO Output Hold Time from SCLK "↑" (Note 38)	tSOH	120			ns

Note 38. Except when input the eighth bit of the command code.

4-2. PLL Clock (CKRESTN bit = "1")

(Ta= -40 to 85°C; AVDD=3.0 to 3.6V, TVDD=1.7 to 3.6V, DVDD=1.14 to 1.3V, AVSS=DVSS=0V, CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Microcontroller Interface Signal					
SCLK Frequency	fSCLK			7	MHz
SCLK Low Level Width	tSCLKL	60			ns
SCLK High Level Width	tSCLKH	60			ns
Microcontroller → AK7755					
CSN High Level Width	tWRQH	150			ns
Time from CSN "↑" to PDN "↑"	tRST	180			ns
Time from PDN"↑" to CSN "↓"	tIRRQ	1			ms
Time from RQN"↓" to SCLK"↓"	tWSC	150			ns
Time from SCLK"↑" to CSN"↑"	tSCW	240			ns
SI Latch Setup Time	tSIS	60			ns
SI Latch Hold Time	tSIH	60			ns
AK7755 → Microcontroller					
SO Output Delay Time from SCLK "↓"	tSOS			60	ns
SO Output Hold Time from SCLK "↑" (Note 38)	tSOH	60			ns

Note 39. It takes 10ms at maximum until PLL is locked, after setting CKRESTN bit to "1" from "0".

CONT03: Delay RAM, DSP Input / Output Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
C3h	43h	CONT03	0	0	0	0	BANK[3]	BANK[2]	BANK[1]	BANK[0]	00h

D7, D6: DIF2[1:0] DSP DIN2 Input Format Select

DIF2 Mode	DIF2[1:0]	Input Data Format	
0	00	MSB (24-bit)	(default)
1	01	LSB 24-bit	
2	10	LSB 20-bit	
3	11	LSB 16-bit	

Set "00" for I^2S compatible, PCM Short and PCM Long formats.
Set "11" when BITFS[1:0] bits (CONT01: D5, D4) = 2h (32fs).

D5, D4: DOF2[1:0] DSP DOUT2 Output Format Select

DOF2 Mode	DOF2[1:0]	Output Data Format	
0	00	MSB (24-bit)	(default)
1	01	LSB 24-bit	
2	10	LSB 20-bit	
3	11	LSB 16-bit	

Set "00" for I^2S compatible, PCM Short and PCM Long formats.
Set "11" when BITFS[1:0] bits = 2h (32fs).

D3, D2, D1, D0: BANK[3:0] DLRAM mode Setting

DLRAM Partition mode	BANK [3:0]	Delay RAM		
		Bank1	Bank0	
		Linear 20.4f	Ring 20.4f	
0	0000	0	8192 words	(default)
1	0001	1024 words	7168 words	
2	0010	2048 words	6144 words	
3	0011	3072 words	5120 words	
4	0100	4096 words	4096 words	
5	0101	5120 words	3072 words	
6	0110	6144 words	2048 words	
7	0111	7168 words	1024 words	
8	1000	8192 words	0	
9-15	1001 1111		N/A	

CONT05: Accelerator Setting, JX3 Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
C5h	45h	CONT05	ACCRAM CLRN	JX3E	FIR MODE1	FIR MODE2	SUB MODE1	SUB MODE2	MEM DIV[1]	MEM DIV[0]	00h

D7: ACCRAMCLRN Accelerator CRAM Clear Setting
0: Accelerator CRAM is cleared by 0 data after releasing reset. (default)
1: Accelerator CRAM is not cleared after releasing reset.

D6: JX3E External Conditional Jump3 Enable
0: JX3 Disable (default), No. 15 pin output (SDOUT2) when OUT2E bit (CONT0A:D1) = "1"
1: JX3 Enable, No. 15 pin Input

D5: FIRMODE1 Accelerator Ch1 Operation Select
0: Adaptive Filter (default)
1: FIR Filter

D4: FIRMODE2 Accelerator Ch2 Operation Select
0: Adaptive Filter (default)
1: FIR Filter

D3: SUBMODE1 Accelerator Ch1 Mode Select
0: Fullband (default)
1: Subband

D2: SUBMODE2 Accelerator Ch2 Mode Select
0: Fullband (default)
1: Subband

D1, D0: MEMDIV[1:0] Accelerator Memory Select

MODE	MEMDIV[1:0]	ch1	ch2	
0	00	2048	-	(default)
1	01	1792	256	
2	10	1536	512	
3	11	1024	1024	

Write "0" into the "0" registers.

CONT07: DSP Output Format Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
C7h	47h	CONT07	DOF4[1]	DOF4[0]	DOF3[1]	DOF3[0]	0	DOF1[2]	DOF1[1]	DOF1[0]	00h

D7, D6: DOF4[1:0] DSP DOUT4 Output Format Select

DOF4 mode	DOF4[1:0]	Output Data Format	
0	00	MSB justified (24-bit)	(default)
1	01	LSB justified 24-bit	
2	10	LSB justified 20-bit	
3	11	LSB justified 16-bit	

Set "00" for I^2S Compatible, PCM Short and PCM Long formats.
Set "11" when BITFS[1:0] bits (CONT01: D5, D4) =2h (32fs).
Set "00" when connecting to the DAC.

D5, D4: DOF3[1:0] DSP DOUT3 Output Format Select

DOF3 mode	DOF3[1:0]	Output Data Format	
0	00	MSB justified (24-bit)	(default)
1	01	LSB justified 24-bit	
2	10	LSB justified 20-bit	
3	11	LSB justified 16-bit	

Set "00" for I^2S Compatible, PCM Short and PCM Long formats.
Set "11" when BITFS[1:0] bits=2h (32fs).

D2, D1, D0: DOF1[2:0] DSP DOUT1 Output Format Select

DOF1 mode	DOF1[2:0]	Output Data Format	
0	000	MSB (24-bit)	(default)
1	001	LSB 24-bit	
2	010	LSB 20-bit	
3	011	LSB 16-bit	
4	100	MSB 8-bit μ-Law	
5	101	MSB 8-bit A-Law	
6	110	N/A	
7	111	N/A	

Set "000" for I^2S Compatible, PCM Short and PCM Long formats.
Set "011" when BITFS[1:0] bits=2h (32fs).

Write "0" into the "0" registers.

CONT12: Microphone Gain Setting

W	R	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
D2h	52h	CONT12	MGNR [3]	MGNR [2]	MGNR [1]	MGNR [0]	MGNL [3]	MGNL [2]	MGNL [1]	MGNL [0]	00h

D7, D6, D5, D4: MGNR[3:0] Microphone Input Rch Gain Setting

MGNR mode	MGNR[3:0]	Microphone Input Rch Gain	
0	0000	0dB	(default)
1	0001	2dB	
2	0010	4dB	
3	0011	6dB	
4	0100	8dB	
5	0101	10dB	
6	0110	12dB	
7	0111	14dB	
8	1000	16dB	
9	1001	18dB	
A	1010	21dB	
B	1011	24dB	
C	1100	27dB	
D	1101	30dB	
E	1110	33dB	
F	1111	36dB	

D3, D2, D1, D0: MGNL[3:0] Microphone Input Lch Gain

MGNL mode	MGNL[3:0]	Microphone Input Lch Gain	
0	0000	0dB	(default)
1	0001	2dB	
2	0010	4dB	
3	0011	6dB	
4	0100	8dB	
5	0101	10dB	
6	0110	12dB	
7	0111	14dB	
8	1000	16dB	
9	1001	18dB	
A	1010	21dB	
B	1011	24dB	
C	1100	27dB	
D	1101	30dB	
E	1110	33dB	
F	1111	36dB	

■ Power-down and Reset

1. Power-down, Reset and Power Management of the AK7755

The AK7755 has four types of power-down and reset functions that are power-down (PDN pin), Clock reset (CLKRESETN bit (CONT01:D0)), CODEC reset (CRESETN bit(CONT0F:D3)) and DSP reset (DSPRESETN bit(CONT0F:D2)). Each block can be powered-down by power management registers.

2. Power-down

The AK7755 is powered down by setting the PDN pin = "L". The PDN pin must be set to "L" when power up the AK7755. The statuses of output pins in power-down mode are shown below.

LDOE pin = "L" (External 1.2V supply mode)

No	Pin Name	I/O	Power-down Mode Status	No	Pin Name	I/O	Power-down Mode Status
1	VCOM	O	L	17	SO/SDA	I/O	Hi-Z
6	STO/RDY	O	H	18	SCLK/SCL	I/O	Hi-Z
7	LRCK	I/O	L	26	OUT3	O	Hi-Z
8	BICK	I/O	L	27	OUT2	O	Hi-Z
9	CLKO	O	L	28	OUT1	O	Hi-Z
10	XTO	O	H	31	IN4/INN2/DMCLK2	I/O	Hi-Z
11	XTI	I	H	32	IN3/INP2/DMDAT2	I	Hi-Z
14	JX2/SDOUT3/JX2/MAT1	I/O	L	33	IN2/INN1/DMCLK1	I/O	Hi-Z
15	SDOUT2/JX3/MAT1	I/O	L	34	IN1/INP1/DMDAT1	I	Hi-Z
16	SDOUT1	O	L				

Note 44. [I/O] indicates Input / Output attribute of each pin.

LDOE pin = "H" (LDO mode)

No	Pin Name	I/O	Power-down Mode Status	No	Pin Name	I/O	Power-down Mode Status
1	VCOM	O	L	17	SO/SDA	I/O	Hi-Z
6	STO/RDY	O	L	18	SCLK/SCL	I/O	Hi-Z
7	LRCK	I/O	L	24	AVDRV	O	L
8	BICK	I/O	L	26	OUT3	O	Hi-Z
9	CLKO	O	L	27	OUT2	O	Hi-Z
10	XTO	O	H	28	OUT1	O	Hi-Z
11	XTI	I	H	31	IN4/INN2/DMCLK2	I/O	Hi-Z
14	JX2/SDOUT3/JX2/MAT1	I/O	L	32	IN3/INP2/DMDAT2	I	Hi-Z
15	SDOUT2/JX3/MAT1	I/O	L	33	IN2/INN1/DMCLK1	I/O	Hi-Z
16	SDOUT1	O	L	34	IN1/INP1/DMDAT1	I	Hi-Z

3. Power-down Release

3-1. LDOE = "L" (External 1.2V supply mode)

DVDD, TVDD and AVDD should be supplied when the PDN pin = "L". By bringing the PDN pin "H" 600ns (min) after all power supplies are fed (DVDD, TVDD and AVDD), REF voltage circuit (Analog reference voltage) starts operation. Control register write / read should be made 1ms after bringing the PDN pin = "H" (Figure 24). AVDD and TVDD must be powered up first before DVDD. In this case, the power-up sequence between AVDD and TVDD is not critical.

3-2. LDOE = "H" (LDO mode)

TVDD and AVDD should be supplied when the PDN pin = "L". By bringing the PDN pin "H" 600ns (min) after TVDD and AVDD are fed, the power supply circuits for REF generator and internal digital circuit start operation. Control register write / read should be made 1ms after bringing the PDN pin = "H" (Figure 28).

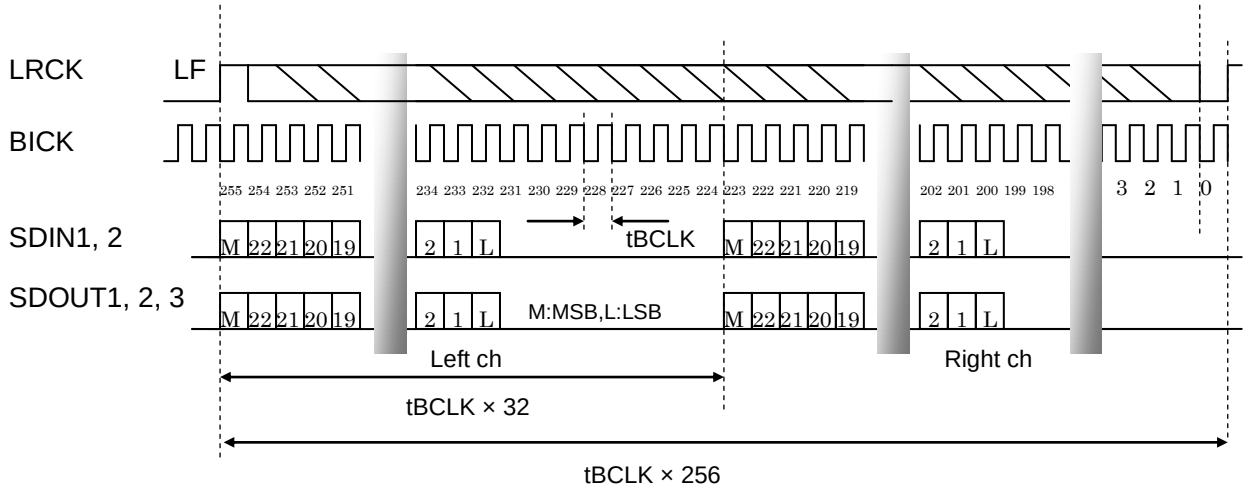

Figure 42. PCM Long Frame 256fs

7. TDM Mode

TDM interface formats shown below are available by setting TDM256 bit = "1". BITFS[1:0] bits should be set to 3h since BICK is fixed to 256fs.

Mode	LRIF[1:0]	TDMMODE[1:0]	Format	Note
0	0h	0h	MSB 24-bit	
1	0h	1h	MSB 24-bit	SLOT7 and 8 Inputs Not Available
2	0h	2h	MSB 24-bit	SLOT5, 6, 7 and 8 Inputs Not Available
3	1h	0h	I^2S Compatible	
4	1h	1h	I^2S Compatible	SLOT7 and 8 Inputs Not Available
5	1h	2h	I^2S Compatible	SLOT5, 6, 7 and 8 Inputs Not Available
6	2h	0h	PCM Short Frame	
7	2h	1h	PCM Short Frame	SLOT7 and 8 Inputs Not Available
8	2h	2h	PCM Short Frame	SLOT5, 6, 7 and 8 Inputs Not Available
9	3h	0h	PCM Long Frame	
10	3h	1h	PCM Long Frame	SLOT7 and 8 Inputs Not Available
11	3h	2h	PCM Long Frame	SLOT5, 6, 7 and 8 Inputs Not Available

Read

Command	Address	Data Length	Description
0x24	16bit	24bit×n	CRAM/OFREG Preparation Data Read during RUN
0x32	16bit	24bit×n	Read operation form OFREG during system reset
0x34	16bit	24bit×n	Read operation from CRAM during system reset
0x38	16bit	40bit×n	Read operation from PRAM during system reset
0x3B	16bit	24bit×n	Read operation from ACRAM during system reset
0x40~0x5F	None	8bit	Write operation to Control Registers 00~1Fh
0x60	None	8bit	Device Identification
0x66	None	8bit	Write operation to Control Register 26h
0x6A	None	8bit	Write operation to Control Register 2Ah
0x70	None	8bit	DSP Error Status Read
0x72	None	16bit	CRC result Read
0x76	None	32bit	Read operation from MIR1 28-bit is upper-bit justified. Lower 4-bits are for validity flags.
0x78	None	32bit	Read operation from MIR2 28-bit is upper-bit justified. Lower 4-bits are for validity flags.
0x7A	None	32bit	Read operation from MIR3 28-bit is upper-bit justified. Lower 4-bits are for validity flags.
0x7C	None	32bit	Read operation from MIR4 28-bit is upper-bit justified. Lower 4-bits are for validity flags.

Reading other than this command code is prohibited.

5. Echo-Back Mode

The AK7755 has an echo-back mode that the device outputs write data sequentially from the SO pin.

5-1. Write Sequence

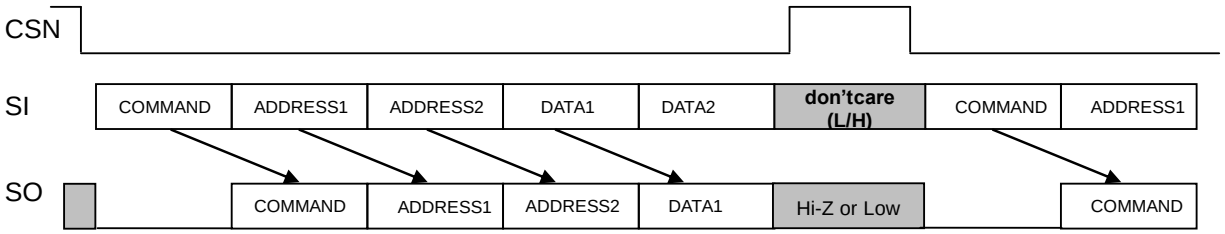

Figure 49. Echo-Back Writing 1 (SPI)

The input data of the SI pin is echoed back on the SO pin by shifting 8-bit to the right.

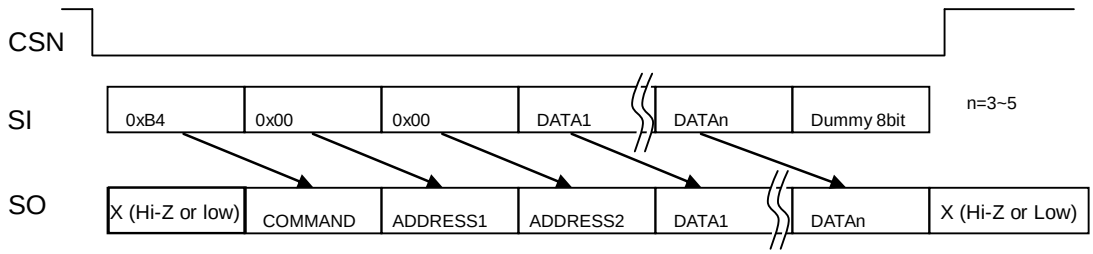

Figure 50. Echo-Back Writing 2 (SPI)

It is possible to verify the written data by inputting an extra 8-bit clock. If the dummy data is more than the data length, this dummy data is written on the next address. (40 bits for PRAM, 24 bits for CRAM and 24 bits for OFREG writings)

3. Offset REG (OFREG) Write (during system reset)

Field	Write data
(1) COMMAND Code	0xB2
(2) ADDRESS1	0 0 0 0 0 0 0 0
(3) ADDRESS2	0 0 A5 A4 A3 A2 A1 A0
(4) DATA1	0 0 0 0 0 0 0 0
(5) DATA2	0 0 0 D12 D11 D10 D9 D8
(6) DATA3	D7~D0
	Three bytes of data may be written continuously for each address.

4. Accelerator Coefficient RAM (ACRAM) Write (during system reset)

Field	Write data
(1) COMMAND Code	0xBB
(2) ADDRESS1	0 0 0 0 0 A10 A9 A8
(3) ADDRESS2	A7 A6 A5 A4 A3 A2 A1 A0
(4) DATA1	D19~D12
(5) DATA2	D11~D4
(6) DATA3	D3~D0 0 0 0 0
	Three bytes of data may be written continuously for each address.

6-2. Write Operation during System Reset / RUN

1. Control Register Write (during system reset / RUN)

Field	Write data
(1) COMMAND Code	0xC0~0xDF, 0xE6, 0xEA
(2) DATA	D7~D0

2. External Conditional Jump Code Write (during system reset / RUN)

Field	Write data
(1) COMMAND Code	0xF4
(2) DATA	D7~D0

3. CRC Code Write (during system reset / RUN)

Field	Write data
(1) COMMAND Code	0xF2
(2) DATA	D15~D8
(3) DATA	D7~D0

6-3. Write Operation during RUN

1. Coefficient RAM (CRAM) Write Preparation (during RUN)

Preparation	Write data
(1) COMMAND Code	0x80~0x8F (one data at 80h, sixteen data at 8Fh)
(2) ADDRESS1	0 0 0 0 0 A10 A9 A8
(3) ADDRESS2	A7 ~ A0
(4) DATA1	D23~D16
(5) DATA2	D15~D8
(6) DATA3	D7~D0

6-6. Read Operation during RUN

1. CRAM Write Preparation Read (during RUN)

Field	Write data	Readout data
(1) COMMAND Code	0x24	
(2) ADDRESS1		A15~A8
(3) ADDRESS2		A8~A0
(4) DATA1		D23~D16
(5) DATA2		D15~D8
(6) DATA3		D7~D0

2. OFREG Write Preparation Read (during RUN)

Field	Write data	Readout data
(1) COMMAND Code	0x24	
(2) ADDRESS1		A15~A8
(3) ADDRESS2		A8~A0
(4) DATA1		0 0 0 0 0 0 0 0
(5) DATA2		D15~D8
(6) DATA3		D7~D0

3. MIR1/2/3/4 Read (during RUN)

Field	Write data	Readout data
(1) COMMAND Code	0x76(MIR1) 0x78(MIR2) 0x7A(MIR3) 0x7C(MIR4)	
(2) DATA1		D27~D20
(3) DATA2		D19~D12
(4) DATA3		D11~D4
(5) DATA4		D3 D2 D1 D0 (flag3) (flag2) (flag1) (flag0)

Note 48. Data is valid only when all flags are zero.

7. Timing

7-1. RAM Writing Timing during System Reset

Write to Program RAM (PRAM), Coefficient RAM (CRAM), Offset REG (OFREG) and Accelerator Coefficient RAM (CRAM) during system reset in the order of command code, address and data. The PRAM start address is fixed to 0h. When writing the data to consecutive address locations, continue to input data only. PRAM address is incremented by 1 automatically.

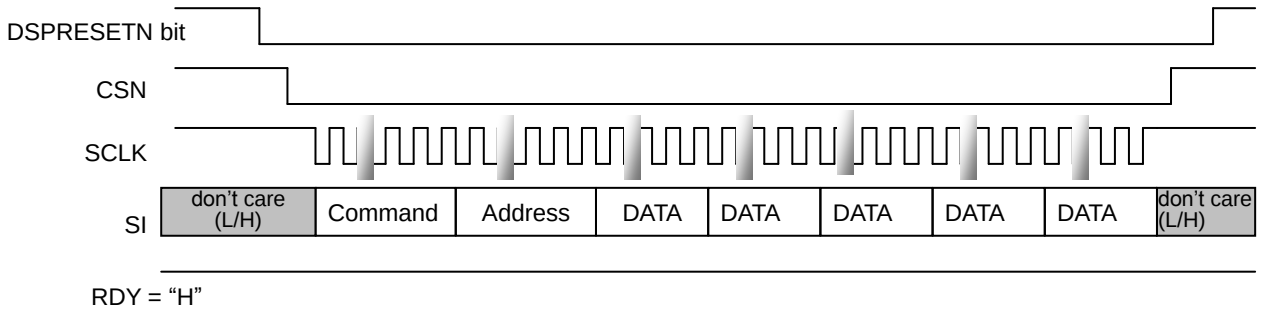

Figure 53. Writing to RAM at Consecutive Address Locations (SPI)

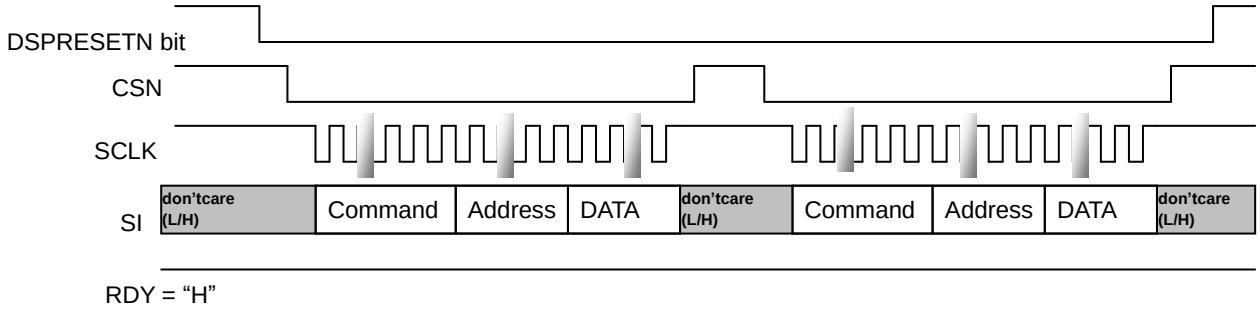

Figure 54. Writing to RAM at Random Address Locations (SPI)

7-2. RAM Writing Timing during RUN

These operations are to rewrite the Coefficient RAM (CRAM) and Offset REG (OFREG) during RUN. Data writing is executed in two steps; write preparation and write execution. The written data can be confirmed by reading the write preparation data.

1. Write Preparation

After inputting the assigned command code (8 bits) to select the number of data from 1 to 16, input the starting address of write (16 bits all "0") and the number of data assigned by command code in this order. In slave mode, a write preparation command is prohibited for "2 LRCK" cycles (2/fs) after releasing DSP reset (DSPRESETN bit).

2. Write Preparation Data Confirmation

After write preparation, prepared data for writing can be confirmed. Address and Data are read in this order by write preparation data confirmation command "24h". The data will be "0x000001" when reading more than write preparation data. Execute write preparation again when the address and data are disturbed by external noise.

3. Write Execution

Upon completion of this operation, execute a RAM write during RUN by inputting the corresponding command code and address (16 bits, all "0") in this order.

Note 49. Execute write preparation, write preparation read and write execution in this order. When writing to RAM without a write preparation sequence, a malfunction occurs. Access operation by a microcontroller is prohibited until RDY changes to "H".

Write modification of the RAM content is executed whenever the RAM address for modification is assigned. For example, when 5 data are written, from RAM address "10", it is executed as shown below.

RAM execution address	7	8	9	10	11	13	16	11	12	13	14	15
				↓	↓				↓	↓	↓	
Write execution position				○	○	↑			○	○	○	

Note 50. Address "13" is not executed until rewriting address "12".

4. Acknowledgement Polling

The AK7755 cannot receive instructions while the RDY pin (Data Write Ready pin) is at low level. The maximum transition time of the RDY pin from low level to high level is 2/fs (fs: sampling frequency), but it is possible to confirm in a faster cycle that the RDY pin has become high by checking the AK7755 internal condition, which is made by verifying the acknowledgement.

4-1. Generation of "Not Acknowledged"

The AK7755 does not accept command codes until the RDY pin is set to a high level, when a command is received to set the RDY pin to a low level. In order to confirm the RDY pin condition, a "Write Slave-Address assignment" should be sent after a Start condition. If the RDY pin is then at a low level, "Acknowledgement" is not generated at the succeeding clock (generation of "Not Acknowledged"). After sending "Not Acknowledged", the BUS is released and all receiving data are ignored until the next start condition (behaves as if it received Slave address of other device).

4-2. When Read Slave-address assignment is received without receiving read command code

Data read in the AK7755 can be made only in the previously documented Read sequence. Data cannot be read out without receiving a read command code. The AK7755 generates a "Not Acknowledged" when a "Read Slave-address Assignment" is received without proper receipt of read command.

5. Limitation in use of I^2C Interface

The I2C interface does not support the following features.
No operation in Hs Mode (max:3.4MHz). The AK7755 Supports FAST mode (max:400KHz).

Note 54. Do not turn off the power of the AK7755 whenever the power supplies of other devices of the same system are turned on. The source of the pull-up of SDA and SCL of I^2C BUS must not exceed the TVDD. (The diode exists for TVDD in the SDA and SCL pins.)

4. LINE Input Gain Amplifier

The AK7755 has a gain amplifier for line inputs. It is enabled by setting PMLI bit (CONT0F: D5) = "1", and it outputs a signal to the L channel of the ADC2. LIGN[3:0] bits (CONT13: D7-D4) controls the gain. The typical input impedance is 20kΩ (typ). A pop noise occurs if the input gain is changed during operation.

The AK7755 becomes digital microphone interface mode when DMIC2 bit (CONT1E: D4) = "1". Digital microphone input data to the DMDAT2 pin is input to the Lch/Rch of the ADC2.

ADC2 Input Setting

DMIC2 bit	ADC2 Lch Input	ADC2 Rch Input	
0	LIN	No	(default)
1	Digital Microphone	Digital Microphone	

Mode	LIGN[3]	LIGN[2]	LIGN[1]	LIGN[0]	Input Gain	
0	0	0	0	0	0dB	(default)
1	0	0	0	1	-3dB	
2	0	0	1	0	-6dB	
3	0	0	1	1	-9dB	
4	0	1	0	0	-12dB	
5	0	1	0	1	-15dB	
6	0	1	1	0	-18dB	
7	0	1	1	1	-21dB	
8	1	0	0	0	N/A	
9	1	0	0	1	+3dB	
A	1	0	1	0	+6dB	
B	1	0	1	1	+9dB	
C	1	1	0	0	+12dB	
D	1	1	0	1	+15dB	
E	1	1	1	0	+18dB	
F	1	1	1	1	+21dB	

Table 3. Line Input Gain

The period of (1) varies by the setting value of DATT bit. The transition time of attenuation amount from 0dB to -∞ and vice versa is shown below.

ATSPAD	(1)Period (max)			
	LRCK Cycle	fs=48kHz	fs=44.1kHz	fs=8kHz
0	828/fs	17.25ms	18.82ms	103.5ms
1	828/fs x 4	69ms	75.27ms	414ms

When changing channels, the input channel should be changed during (2). The period of (2) should be around 200ms because there is some DC difference between the channels (3).

2-3. ADC Digital Volume

The ADC of the AK7755 has channel-independent digital volume control (256 levels, 0.5dB step). VOLADL [7:0] bits (CONT15:D7-D0), VOLADR [7:0] bits (CONT16:D7-D0), VOLAD2L [7:0] bits (CONT17:D7-D0) and VOLAD2R [7:0] bits (CONT1D:D7-D0) control these volume values independently.

ADC Stereo Lch VOLADL [7:0]	ADC Stereo Rch VOLADR [7:0]	ADC2 Lch VOLAD2L [7:0]	ADC2 Rch VOLAD2R [7:0]	Attenuation Level	
00h	00h	00h	00h	+24.0dB	
01h	01h	01h	01h	+23.5dB	
02h	02h	02h	02h	+23.0dB	
:	:	:	:	:	
2Fh	2Fh	2Fh	2Fh	+0.5dB	
30h	30h	30h	30h	0.0dB	(default)
31h	31h	31h	31h	-0.5dB	
:	:	:	:	:	
FDh	FDh	FDh	FDh	-102.5dB	
FEh	FEh	FEh	FEh	-103.0dB	
FFh	FFh	FFh	FFh	Mute (-∞)	

Table 4. ADC Digital Volume Level Setting

Transition time between set values can be selected by ATSPAD bit (CONT0C: D5).

MODE	ATSPAD	ATT speed
0	0	1/fs
1	1	4/fs

Table 5. ADC Volume Transition Time Setting

The transition between set values is soft transition of 1021 levels in Mode 0. It takes 1021/fs (21.3ms@fs=48kHz) from 00h to FFh(MUTE). If the PDN pin is set to “L”, the VOLADL/R[7:0] bits are initialized to 30h.

■ Analog Output Block

The AK7755 can output an analog mixing signal of DAC and line-in amplifier outputs from the OUT3 pin. AD conversion is available by setting PMAD2L bit (CONT0E: D5) to "1" even when the analog mixing output is ON.

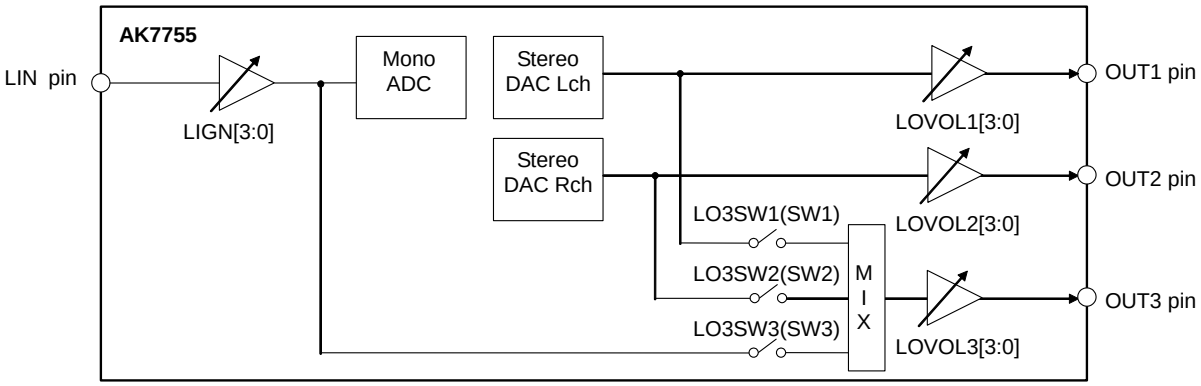

Figure 74. Analog Output Circuit

1. Line Output Amplifier

The AK7755 has a line output amplifier. The maximum amplitude is 0.76 × AVDD (2.51[Vpp] @AVDD=3.3V) and load resistance is 10kΩ (min). LOVOL1/2/3[3:0] bits (CONT14: D3-D0/ CONT14: D7-D4/ CONT13: D3-D0) control the stereo line output volume. A pop noise occurs if the output gain is changed during operation.

LOVOL1,L2,L3[3:0]	Attenuation	LOVOL1, L2, L3[3:0]	Attenuation
0h	Mute(default)	8h	-14dB
1h	-28dB	9h	-12dB
2h	-26dB	Ah	-10dB
3h	-24dB	Bh	-8dB
4h	-22dB	Ch	-6dB
5h	-20dB	Dh	-4dB
6h	-18dB	Eh	-2dB
7h	-16dB	Fh	0dB

Table 11. Line Output Volume

2. Output1 and Output2

The OUT1 and OUT2 pins are connected to the L and R channels of the internal stereo DAC, respectively. The relationship of each control bit and the OUT1 and OUT2 pins are shown below.
The OUT1 and OUT2 pins output settings are controlled by PMLO1/2 bit (CONT0E: D2/D3), PMDAL/R bit (CONT0E: D0 /D1) and LOVOL1/2[3:0] bits (CONT014: D3-D0/D7-D4).

PMLO1 bit	PMDAL bit	LOVOL1[3:0] bits	OUT1 pin Output
0	X	X	Hi-Z
1	0	X	1/2 x AVDD
1	1	0h(mute)	1/2 x AVDD
1	1	1h-Fh	DAC Lch Output

PMLO2 bit	PMDAR bit	LOVOL2[3:0] bits	OUT2 pin Output
0	X	X	Hi-Z
1	0	X	1/2 x AVDD
1	1	0h(mute)	1/2 x AVDD
1	1	1h-Fh	DAC Rch Output

68ABh	00h	Dummy Data2_0
68ACh	00h	Dummy Data2_1
68ADh	00h	Dummy Data3_0
68AEh	00h	Dummy Data3_1
68AFh	00h	Dummy Data4_0
68B0h	00h	Dummy Data4_1
68B1h	00h	Dummy Data5_0
68B2h	00h	Dummy Data5_1
68B3h	00h	Dummy Data6_0
68B4h	00h	Dummy Data6_1
68B5h	F2h	CRC WRITE Command Code
68B6h	CRC DATA15-8	CRC MSB 8-bit Data
68B7h	CRC DATA7-0	CRC LSB 8-bit Data
68B8h	00h	Reserve
• • •	• • •	
7FFFh	00h	Reserve

Note 57. DSPRESETN bit (CONT0F: D2) must be "0" when downloading a DSP program. Especially this setting is necessary when changing the DSP program during operation by selecting EEPROM mat.

Note 58. A WRITE command for arbitrary control register can be written to Dummy data *_0, and write register setting for the control register to Dummy data*_1 in the table above.

Data transffer from EEPROM can be confirmed by writing R(x) (16-bit) data to CRCDATA (addr: 787Ch, 787Dh) which is the remainder of serial data D(x) from addres 0000h to 68B7h devided by a generating polynominal; $G(x)=x^{16}+x^{12}+x^5+1$ (Initial Value= 0).

3. EEPROM Automatic Re-downloading

When a programmed WDT or CRC error is detected, automatic re-downloading of the EEPROM data is available up to 4 times by setting the EXPEEP pin = "H". When an error occurs after re-downloading more than 4 times, "L" level is output on the STO pin and the device stops. The device status can be checked by reading STO bit (CONT0D: D7). The CRC function is enabled by setting CRCE bit (CONT10: D6) to "1". The default setting of CRCE bit is "0" (disabled).
This setting is initialized (error count: 0) by the PDN pin = "L". It is not initialized by a clock reset.

4. EEPROM Mat Select

The pin number 20 becomes the MATSEL pin that enables EEPROM program mat selecting when the EXTEEP pin = "H".
Connect a 256K-bit EEPROM and bring the MATSEL pin = "L" when not selecting the EEPROM mat.
Connect a 1M-bit EEPROM and bring the MATSEL pin = "H" when selecting the EEPROM mat. In this case, the pin number 14 (MAT1) and 15 (MAT0) are address pins of the mat select.
Single program is stored in every 256K bits as a program map. The EEPROM can store four programs in total. The MAT1 and MAT0 pins select a program to download to the AK7755. OUT3E bit (CONT0A, D2) and OUT2E bit (CONT0A, D1) must not set to "1" when selecting an EEPROM mat (MATSEL pin = "H").

Program No.	MAT1 (14pin)	MAT0 (15pin)	EEPROM Storing Beginning Address	I^2C 1st Byte
1	0	0	17'h00000	"1 0 1 0 0 0 0 R/Wn
2	0	1	17'h08000	"1 0 1 0 0 0 0 R/Wn
3	1	0	17'h10000	"1 0 1 0 0 0 1 R/Wn"
4	1	1	17'h18000	"1 0 1 0 0 0 1 R/Wn"

5. I2CSEL pin = “H”, EXTEEP pin = “H”, MATSEL pin = “L”, LDOE pin = “L”

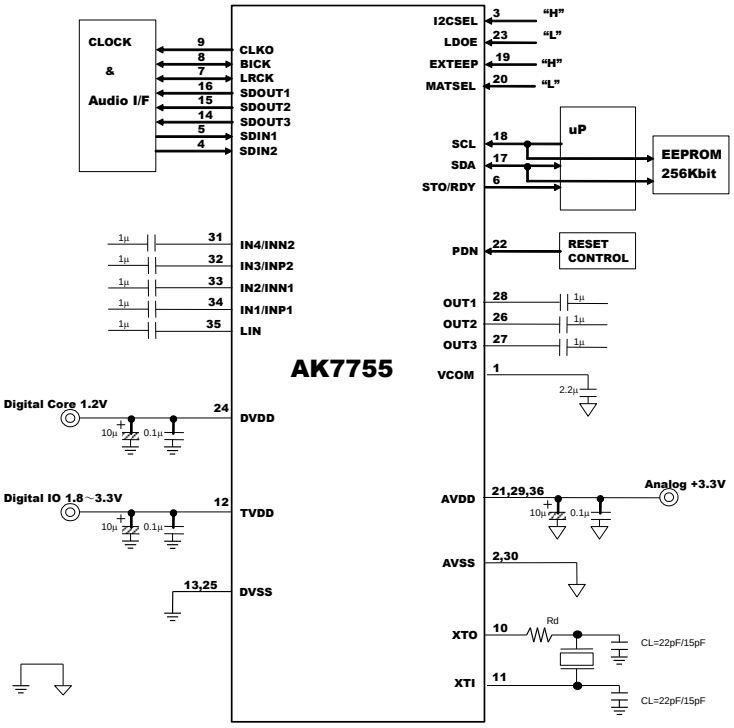

Figure 83. I^{2}C Interface Connection with External Power Supply and EEPROM

6. I2CSEL pin = “H”, EXTEEP pin = “H”, MATSEL pin = “L”, LDOE pin = “H”

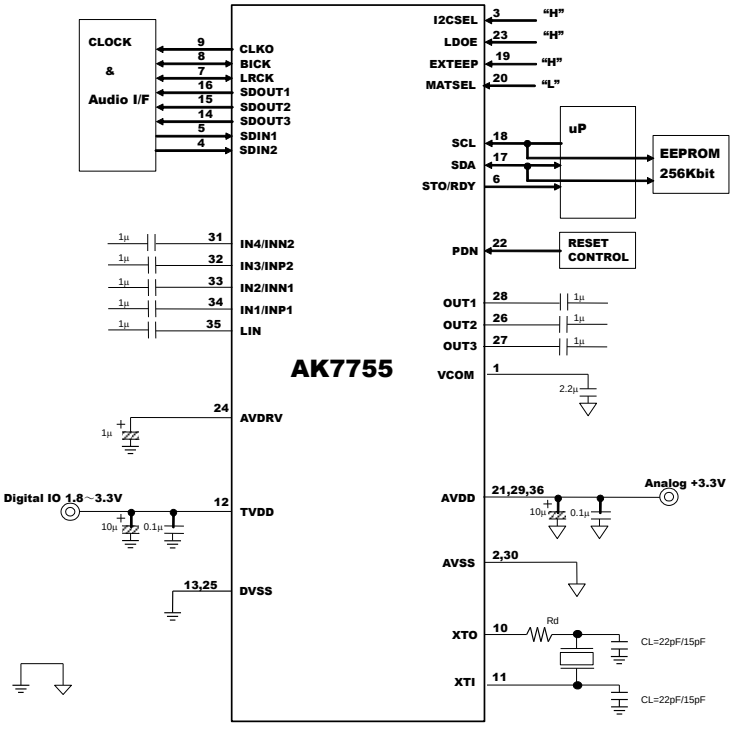

Figure 84. I^{2}C Interface Connection with Internal LDO and EEPROM