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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-4
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	EBI/EMI, FIFO, SCI, SmartCard
Peripherals	DMA, POR, WDT
Number of I/O	28
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-BBGA
Supplier Device Package	256-BGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/d6417750rba240hvu0

Section 8 Pipelining

Section 9 Power-Down Modes

Section 10 Clock Oscillation Circuits

Section 11 Realtime Clock (RTC)

Section 12 Timer Unit (TMU)

Item	Features
Interrupt controller (INTC)	• Five independent external interrupts: NMI, IRL3 to IRL0 • 15-level encoded external interrupts: IRL3 to IRL0 • On-chip peripheral module interrupts: Priority level can be set for each module
User break controller (UBC)	• Supports debugging by means of user break interrupts • Two break channels • Address, data value, access type, and data size can all be set as break conditions • Supports sequential break function
Bus state controller (BSC)	• Supports external memory access — 64/32/16/8-bit external data bus • External memory space divided into seven areas, each of up to 64 Mbytes, with the following parameters settable for each area: — Bus size (8, 16, 32, or 64 bits) — Number of wait cycles (hardware wait function also supported) — Connection of DRAM, synchronous DRAM, and burst ROM possible by setting space type — Supports fast page mode and DRAM EDO — Supports PCMCIA interface — Chip select signals ($\overline{CS0}$ to $\overline{CS6}$) output for relevant areas • DRAM/synchronous DRAM refresh functions — Programmable refresh interval — Supports CAS-before-RAS refresh mode and self-refresh mode • DRAM/synchronous DRAM burst access function • Big endian or little endian mode can be set

In the SH7750, the CPU cannot access a PCMCIA interface area. When performing access from the CPU to a PCMCIA interface area in the SH7750S or the SH7750R, access is always performed using the values of the SA and TC bits set in the PTEA register.

The PCMCIA interface area is always accessed by the DMAC with the values of CHCRn.SSAn, CHCRn.DSAn, CHCRn.STC, and CHCRn.DTC in the DMAC. For details, see section 14, Direct Memory Access Controller (DMAC).

P0, P1, P3, U0 Areas: The P0, P1, P3, and U0 areas can be accessed using the cache. Whether or not the cache is used is determined by the cache control register (CCR). When the cache is used, with the exception of the P1 area, switching between the copy-back method and the write-through method for write accesses is specified by the CCR.WT bit. For the P1 area, switching is specified by the CCR.CB bit. Zeroizing the upper 3 bits of an address in these areas gives the corresponding external memory space address. However, since area 7 in the external memory space is a reserved area, a reserved area also appears in these areas.

P2 Area: The P2 area cannot be accessed using the cache. In the P2 area, zeroizing the upper 3 bits of an address gives the corresponding external memory space address. However, since area 7 in the external memory space is a reserved area, a reserved area also appears in this area.

P4 Area: The P4 area is mapped onto SH-4 on-chip I/O channels. This area cannot be accessed using the cache. The P4 area is shown in detail in figure 3.4.

4.1.2 Register Configuration

Table 4.4 shows the cache control registers.

Table 4.4 Cache Control Registers

Name	Abbreviation	R/W	Initial Value*1	P4 Address*2	Area 7 Address*2	Access Size
Cache control register	CCR	R/W	H'0000 0000	H'FF00 001C	H'1F00 001C	32
Queue address control register 0	QACR0	R/W	Undefined	H'FF00 0038	H'1F00 0038	32
Queue address control register 1	QACR1	R/W	Undefined	H'FF00 003C	H'1F00 003C	32

Notes: 1. The initial value is the value after a power-on or manual reset.
2. This is the address when using the virtual/physical address space P4 area. The area 7 address is the address used when making an access from physical address space area 7 using the TLB.

Table 5.3 Types of Reset

	Reset State Transition Conditions		Internal States	
Type	**SCK2**	**$\overline{\text{RESET}}$**	**CPU**	**On-Chip Peripheral Modules**
Power-on reset	High	Low	Initialized	See Register Configuration in each section
Manual reset	Low	Low	Initialized	

(3) H-UDI Reset

- Source: SDIR.TI3–TI0 = B'0110 (negation) or B'0111 (assertion)
- Transition address: H'A000 0000
- Transition operations:

  Exception code H'000 is set in EXPEVT, initialization of VBR and SR is performed, and a branch is made to PC = H'A000 0000.

  In the initialization processing, the VBR register is set to H'0000 0000, and in SR, the MD, RB, and BL bits are set to 1, the FD bit is cleared to 0, and the interrupt mask bits (IMASK) are set to B'1111.

  CPU and on-chip peripheral module initialization is performed. For details, see the register descriptions in the relevant sections.

```
H-UDI_reset()
{
    EXPEVT = H'00000000;
    VBR = H'00000000;
    SR.MD = 1;
    SR.RB = 1;
    SR.BL = 1;
    SR.IMASK = B'1111;
    SR.FD = 0;
    Initialize_CPU();
    Initialize_Module(PowerOn);
    PC = H'A0000000;
}
```

Section 6 Floating-Point Unit (FPU)

6.1 Overview

The floating-point unit (FPU) has the following features:

- Conforms to IEEE754 standard
- 32 single-precision floating-point registers (can also be referenced as 16 double-precision registers)
- Two rounding modes: Round to Nearest and Round to Zero
- Two denormalization modes: Flush to Zero and Treat Denormalized Number
- Six exception sources: FPU Error, Invalid Operation, Divide By Zero, Overflow, Underflow, and Inexact
- Comprehensive instructions: Single-precision, double-precision, graphics support, system control

When the FD bit in SR is set to 1, the FPU cannot be used, and an attempt to execute an FPU instruction will cause an FPU disable exception.

6.2 Data Formats

6.2.1 Floating-Point Format

A floating-point number consists of the following three fields:

- Sign (s)
- Exponent (e)
- Fraction (f)

The FPU can handle single-precision and double-precision floating-point numbers, using the formats shown in figures 6.1 and 6.2.

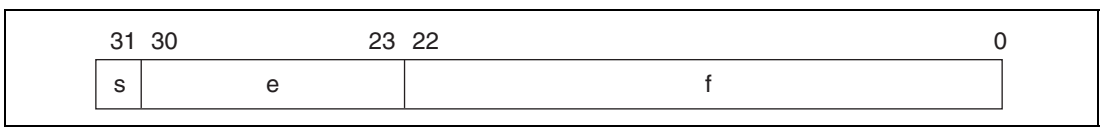


Figure 6.1 Format of Single-Precision Floating-Point Number

The FPSCR cause field contains bits corresponding to all of above sources E, V, Z, O, U, and I, and the FPSCR flag and enable fields contain bits corresponding to sources V, Z, O, U, and I, but not E. Thus, FPU errors cannot be disabled.

When an exception source occurs, the corresponding bit in the cause field is set to 1, and 1 is added to the corresponding bit in the flag field. When an exception source does not occur, the corresponding bit in the cause field is cleared to 0, but the corresponding bit in the flag field remains unchanged.

- Enable/disable exception handling

  The FPU supports enable exception handling and disable exception handling.

  Enable exception handling is initiated in the following cases:

  — FPU error (E): FPSCR.DN = 0 and a denormalized number is input

  — Invalid operation (V): FPSCR.EN.V = 1 and (instruction = FTRV or invalid operation)

  — Division by zero (Z): FPSCR.EN.Z = 1 and division with a zero divisor

  — Overflow (O): FPSCR.EN.O = 1 and instruction with possibility of operation result overflow

  — Underflow (U): FPSCR.EN.U = 1 and instruction with possibility of operation result underflow

  — Inexact exception (I): FPSCR.EN.I = 1 and instruction with possibility of inexact operation result

  For information on these possibilities, see the individual instruction descriptions in chapter 9 of the SH-4 Software Manual. The particulars differ demanding on the instruction. All exception events that originate in the FPU are assigned as the same exception event. The meaning of an exception is determined by software by reading system register FPSCR and interpreting the information it contains. If no bits are set in the cause field of FPSCR when one or more of bits O, U, I, and V (in case of FTRV only) are set in the enable field, this indicates that an actual exception source is not generated. Also, the destination register is not changed by any enable exception handling operation.

  Except for the above, the FPU disables exception handling. In all processing, the bit corresponding to source V, Z, O, U, or I is set to 1, and disable exception handling is provided for each exception.

  — Invalid operation (V): qNAN is generated as the result.

  — Division by zero (Z): Infinity with the same sign as the unrounded value is generated.

Functional Category	No.	Instruction		Instruction Group	Issue Rate	Latency	Execution Pattern	Lock		
								Stage	Start	Cycles
System control instructions	119	NOP		MT	1	0	#1	—	—	—
	120	CLRMAC		CO	1	3	#28	F1	3	2
	121	CLRS		CO	1	1	#1	—	—	—
	122	CLRT		MT	1	1	#1	—	—	—
	123	SETS		CO	1	1	#1	—	—	—
	124	SETT		MT	1	1	#1	—	—	—
	125	TRAPA	#imm	CO	7	7	#13	—	—	—
	126	RTE		CO	5	5	#8	—	—	—
	127	SLEEP		CO	4	4	#9	—	—	—
	128	LDTLB		CO	1	1	#2	—	—	—
	129	LDC	Rm,DBR	CO	1	3	#14	SX	3	2
	130	LDC	Rm,GBR	CO	3	3	#15	SX	3	2
	131	LDC	Rm,Rp_BANK	CO	1	3	#14	SX	3	2
	132	LDC	Rm,SR	CO	4	4	#16	SX	3	2
	133	LDC	Rm,SSR	CO	1	3	#14	SX	3	2
	134	LDC	Rm,SPC	CO	1	3	#14	SX	3	2
	135	LDC	Rm,VBR	CO	1	3	#14	SX	3	2
	136	LDC.L	@Rm+,DBR	CO	1	1/3	#17	SX	3	2
	137	LDC.L	@Rm+,GBR	CO	3	3/3	#18	SX	3	2
	138	LDC.L	@Rm+,Rp_BANK	CO	1	1/3	#17	SX	3	2
	139	LDC.L	@Rm+,SR	CO	4	4/4	#19	SX	3	2
	140	LDC.L	@Rm+,SSR	CO	1	1/3	#17	SX	3	2
	141	LDC.L	@Rm+,SPC	CO	1	1/3	#17	SX	3	2
	142	LDC.L	@Rm+,VBR	CO	1	1/3	#17	SX	3	2
	143	LDS	Rm,MACH	CO	1	3	#28	F1	3	2
	144	LDS	Rm,MACL	CO	1	3	#28	F1	3	2
	145	LDS	Rm,PR	CO	2	3	#24	SX	3	2
	146	LDS.L	@Rm+,MACH	CO	1	1/3	#29	F1	3	2
	147	LDS.L	@Rm+,MACL	CO	1	1/3	#29	F1	3	2
	148	LDS.L	@Rm+,PR	CO	2	2/3	#25	SX	3	2
	149	STC	DBR,Rn	CO	2	2	#20	—	—	—
	150	STC	SGR,Rn	CO	3	3	#21	—	—	—

4. Conditional branch latency “2 (or 1)”: The latency is 2 for a nonzero displacement, and 1 for a zero displacement.
5. Double-precision floating-point instruction latency “(L1, L2)/L3”: L1 is the latency for FR [n+1], L2 that for FR [n], and L3 that for FPSCR.
6. FTRV latency “(L1, L2, L3, L4)/L5”: L1 is the latency for FR [n], L2 that for FR [n+1], L3 that for FR [n+2], L4 that for FR [n+3], and L5 that for FPSCR.
7. Latency “L1/L2/L3/L4” of MAC.L and MAC.W instructions: L1 is the latency for Rm, L2 that for Rn, L3 that for MACH, and L4 that for MACL.
8. Latency “L1/L2” of MUL.L, MULS.W, MULU.W, DMULS.L, and DMULU.L instructions: L1 is the latency for MACH, and L2 that for MACL.
9. Execution pattern: The instruction execution pattern number (see figure 8.2)
10. Lock/stage: Stage locked by the instruction
11. Lock/start: Locking start cycle; 1 is the first D-stage of the instruction.
12. Lock/cycles: Number of cycles locked

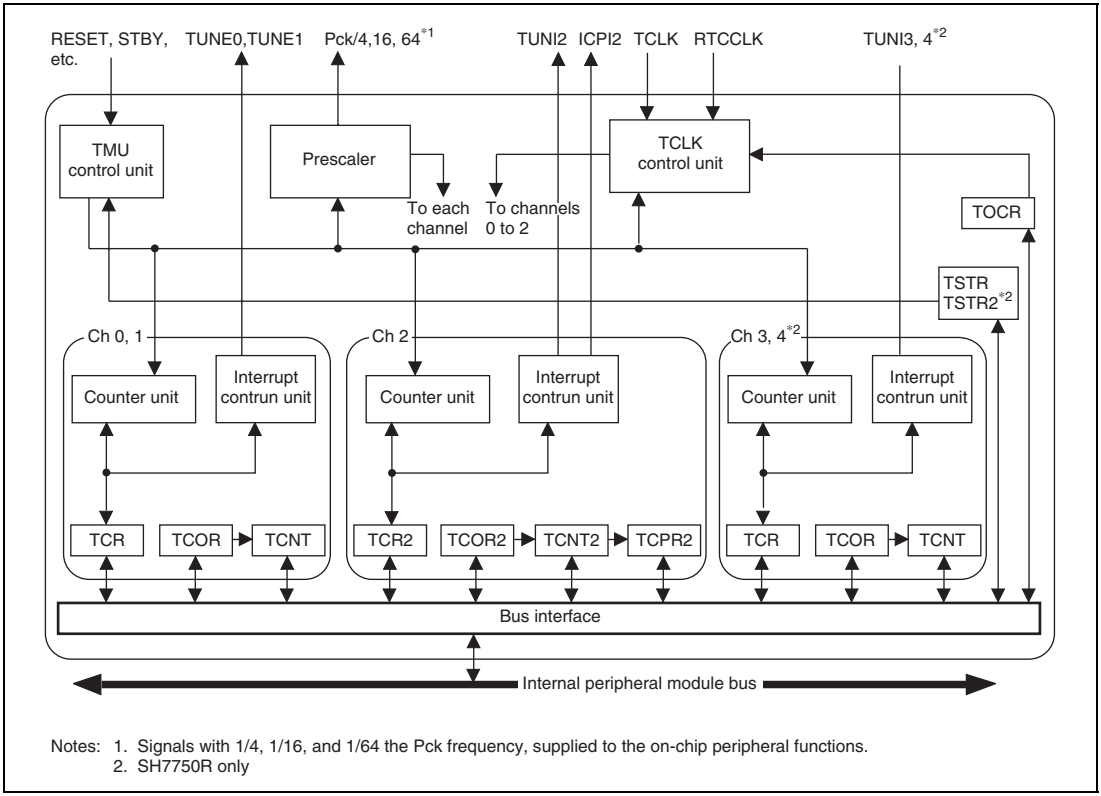
Exceptions:

1. When a floating-point computation instruction is followed by an FMOV store, an STS FPUL, Rn instruction, or an STS.L FPUL, @-Rn instruction, the latency of the floating-point computation is decreased by 1 cycle.
2. When the preceding instruction loads the shift amount of the following SHAD/SHLD, the latency of the load is increased by 1 cycle.
3. When an LS group instruction with a latency of less than 3 cycles is followed by a double-precision floating-point instruction, FIPR, or FTRV, the latency of the first instruction is increased to 3 cycles.

   Example: In the case of FMOV FR4,FR0 and FIPR FV0,FV4, FIPR is stalled for 2 cycles.
4. When MAC/MUL/DMUL is followed by an STS.L MAC, @-Rn instruction, the latency of MAC/MUL/DMUL is 5 cycles.
5. In the case of consecutive executions of MAC/MUL/DMUL, the latency is decreased to 2 cycles.
6. When an LDS to MAC is followed by an STS.L MAC, @-Rn instruction, the latency of the LDS to MAC is 4 cycles.
7. When an LDS to MAC is followed by MAC/MUL/DMUL, the latency of the LDS to MAC is 1 cycle.
8. When an FSCHG or FRCHG instruction is followed by an LS group instruction that reads or writes to a floating-point register, the aforementioned LS group instruction[s] cannot be executed in parallel.
9. When a single-precision FTRC instruction is followed by an “STS FPUL, Rn” instruction, the latency of the single-precision FTRC instruction is 1 cycle.

12.1.2 Block Diagram

Figure 12.1 shows a block diagram of the TMU.



Notes: 1. Signals with 1/4, 1/16, and 1/64 the Pck frequency, supplied to the on-chip peripheral functions.
2. SH7750R only

Figure 12.1 Block Diagram of TMU

12.1.3 Pin Configuration

Table 12.1 shows the TMU pins.

Table 12.1 TMU Pins

Pin Name	Abbreviation	I/O	Function
Clock input/clock output	TCLK	I/O	External clock input pin/input capture control input pin/RTC output pin (shared with RTC)

Bits 13 to 11—Area 0 Burst ROM Control (A0BST2–A0BST0): These bits specify whether burst ROM interface is used in area 0. When burst ROM interface is used, they also specify the number of accesses in a burst. If area 0 is an MPX interface area, these bits are ignored.

Bit 13: A0BST2	Bit 12: A0BST1	Bit 11: A0BST0	Description
0	0	0	Area 0 is accessed as SRAM interface (Initial value)
		1	Area 0 is accessed as burst ROM interface (4 consecutive accesses) Can be used with 8-, 16-, 32-, or 64*-bit bus width
	1	0	Area 0 is accessed as burst ROM interface (8 consecutive accesses) Can only be used with 8-, 16-, or 32-bit bus width
		1	Area 0 is accessed as burst ROM interface (16 consecutive accesses) Can only be used with 8- or 16-bit bus width. Do not specify for 32-bit bus width
1	0	0	Area 0 is accessed as burst ROM interface (32 consecutive accesses) Can only be used with 8-bit bus width
		1	Reserved
	1	0	Reserved
		1	Reserved

Note: * Settable only for SH7750R.

14.8.4 Clearing Request Queues by DTR Format

In DDT mode, the request queues of any channel can be cleared by using DTR.ID, DTR.MD, DTR.SZ, and DTR.COUNT [7:4] in a DTR format. This function is only available when DMAOR.DBL = 1. Table 14.17 shows the DTR format settings for clearing request queues.

Table 14.17 DTR Format for Clearing Request Queues

DMAOR.DBL	DTR.ID	DTR.MD	DTR.SZ	DTR.COUNT[7:4]	Description
0	00	10	110	*	Clear the request queues of all channels (1–7).
					Clear the CH0 request-accepted flag
		11			Setting prohibited
1	00	10	110	*	Clear the request queues of all channels (1–7).
					Clear the CH0 request-accepted flag.
		11		0001	Clear the CH0 request-accepted flag
				0010	Clear the CH1 request queues.
				0011	Clear the CH2 request queues.
				0100	Clear the CH3 request queues.
				0101	Clear the CH4 request queues.
				0110	Clear the CH5 request queues.
				0111	Clear the CH6 request queues.
				1000	Clear the CH7 request queues.

Note: (SH7750R) DTR.SZ = DTR[63:61], DTR.ID = DTR[59:58], DTR.MD = DTR[57:56], DTR.COUNT[7:4] = DTR[55:52]

14.8.5 Interrupt-Request Codes

When the number of transfers specified in DMATCR has been finished and the interrupt request is enabled (CHCR.IE = 1), a transfer-end interrupt request can be sent to the CPU from each channel. Table 14.18 lists the interrupt-request codes that are associated with these transfer-end interrupts.

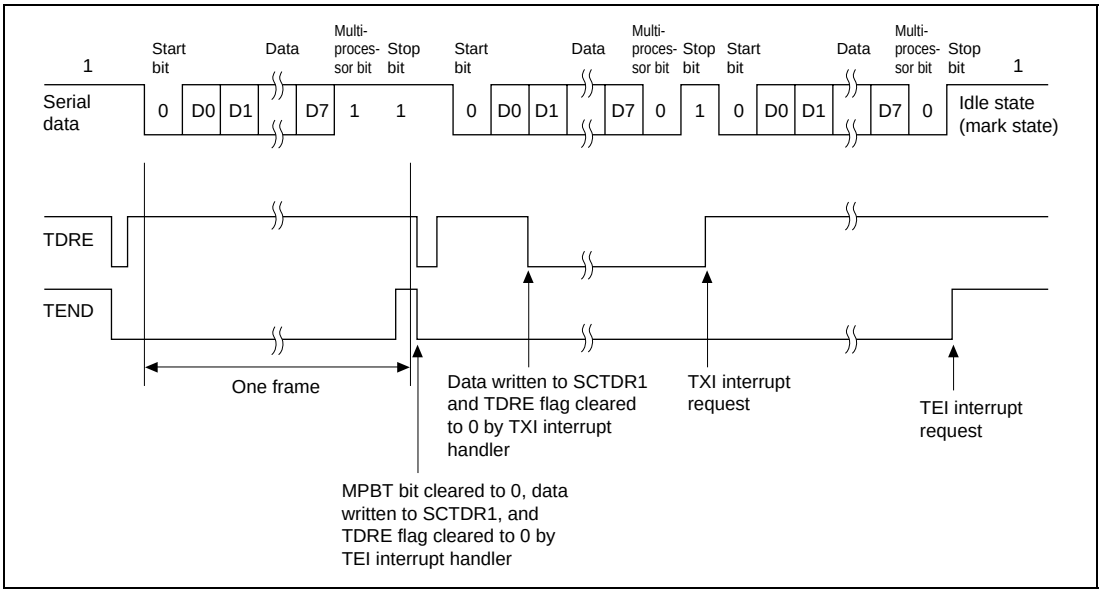


Figure 15.14 Example of SCI Transmit Operation (Example with 8-Bit Data, Multiprocessor Bit, One Stop Bit)

Multiprocessor Serial Data Reception: Figure 15.15 shows a sample flowchart for multiprocessor serial reception.

Use the following procedure for multiprocessor serial data reception after enabling the SCI for reception.

1. Method for determining whether an interrupt generated during receive operation is a multiprocessor interrupt

   When an interrupt such as RXI occurs during receive operation using the on-chip SCI multiprocessor communication function, check the state of the MPIE bit in the SCSCR1 register as part of the interrupt handling routine.

   a. If the MPIE bit in the SCSCR1 register is set to 1

      Ignore the received data.

      Data with the multiprocessor bit (MPB) set to 0 and intended for another station was received, and the RDRF bit in the SCSCR1 register was set to 1. Therefore, clear the RDRF bit in the SCSCR1 register to 0.

16.2.4 Transmit FIFO Data Register (SCFTDR2)

Bit:	7	6	5	4	3	2	1	0
R/W:	W	W	W	W	W	W	W	W

SCFTDR2 is an 8-bit 16-stage FIFO register that stores data for serial transmission.

If SCTSR2 is empty when transmit data has been written to SCFTDR2, the SCIF transfers the transmit data written in SCFTDR2 to SCTSR2 and starts serial transmission.

SCFTDR2 is a write-only register, and cannot be read by the CPU.

The next data cannot be written when SCFTDR2 is filled with 16 bytes of transmit data. Data written in this case is ignored.

The contents of SCFTDR2 are undefined after a power-on reset or manual reset.

16.2.5 Serial Mode Register (SCSMR2)

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	7	6	5	4	3	2	1	0
	—	CHR	PE	O/$\overline{E}$	STOP	—	CKS1	CKS0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R	R/W	R/W

SCSMR2 is a 16-bit register used to set the SCIF's serial transfer format and select the baud rate generator clock source.

SCSMR2 can be read or written to by the CPU at all times.

SCSMR2 is initialized to H'0000 by a power-on reset or manual reset. It is not initialized in standby mode or in the module standby state.

Bits 15 to 7—Reserved: These bits are always read as 0, and should only be written with 0.

16.2.11 Serial Port Register (SCSPTR2)

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	7	6	5	4	3	2	1	0
	RTSIO	RTSDT	CTSIO	CTSDT	—	—	SPB2IO	SPB2DT
Initial value:	0	—	0	—	0	—	0	—
R/W:	R/W	R/W	R/W	R/W	R	R	R/W	R/W

SCSPTR2 is a 16-bit readable/writable register that controls input/output and data for the port pins multiplexed with the serial communication interface (SCIF) pins. Input data can be read from the RxD2 pin, output data written to the TxD2 pin, and breaks in serial transmission/reception controlled, by means of bits 1 and 0. Data can be read from, and output data written to, the $\overline{\text{CTS2}}$ pin by means of bits 5 and 4. Data can be read from, and output data written to, the $\overline{\text{RTS2}}$ pin by means of bits 6 and 7.

SCSPTR2 can be read or written to by the CPU at all times. All SCSPTR2 bits except bits 6, 4, and 0 are initialized to 0 by a power-on reset or manual reset; the value of bits 6, 4, and 0 is undefined. SCSPTR2 is not initialized in standby mode or in the module standby state.

Bits 15 to 8—Reserved: These bits are always read as 0, and should only be written with 0.

Bit 7—Serial Port RTS Port I/O (RTSIO): Specifies the serial port $\overline{\text{RTS2}}$ pin input/output condition. When the $\overline{\text{RTS2}}$ pin is actually set as a port output pin and outputs the value set by the RTSDT bit, the MCE bit in SCFCR2 should be cleared to 0.

Bit 7: RTSIO	Description	
0	RTSDT bit value is not output to $\overline{\text{RTS2}}$ pin	(Initial value)
1	RTSDT bit value is output to $\overline{\text{RTS2}}$ pin	

16.2.12 Line Status Register (SCLSR2)

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	ORER
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	(R/W)*

Note: * Only 0 can be written, to clear the flag.

Bits 15 to 1—Reserved: These bits are always read as 0, and should only be written with 0.

Bit 0—Overrun Error (ORER): Indicates that an overrun error occurred during reception, causing abnormal termination.

Bit 0: ORER	Description
0	Reception in progress, or reception has ended normally*1 (Initial value) [Clearing conditions] • Power-on reset or manual reset • When 0 is written to ORER after reading ORER = 1
1	An overrun error occurred during reception*2 [Setting condition] When the next serial reception is completed while the receive FIFO is full

Notes: 1. The ORER flag is not affected and retains its previous state when the RE bit in SCSCR2 is cleared to 0.
2. The receive data prior to the overrun error is retained in SCFRDR2, and the data received subsequently is lost. Serial reception cannot be continued while the ORER flag is set to 1.

Table 18.2 shows the SCI I/O port pin configuration.

Table 18.2 SCI I/O Port Pins

Pin Name	Abbreviation	I/O	Function
Serial clock pin	MD0/SCK	I/O	Clock input/output
Receive data pin	RxD	Input	Receive data input
Transmit data pin	MD7/TxD	Output	Transmit data output

Note: Pins MD0/SCK and MD7/TxD function as mode input pins MD0 and MD7 after a power-on reset. They are made to function as serial pins by performing SCI operation settings with the TE, RE, CKEI, and CKE0 bits in SCSCR1 and the C/$\overline{A}$ bit in SCSMR1. Break state transmission and detection can be performed by means of a setting in the SCI's SCSPTR1 register.

Table 18.3 shows the SCIF I/O port pin configuration.

Table 18.3 SCIF I/O Port Pins

Pin Name	Abbreviation	I/O	Function
Serial clock pin	$\overline{\text{MRESET}}$/SCK2	Input	Clock input
Receive data pin	MD2/RxD2	Input	Receive data input
Transmit data pin	MD1/TxD2	Output	Transmit data output
Modem control pin	$\overline{\text{CTS2}}$	I/O	Transmission enabled
Modem control pin	MD8/$\overline{\text{RTS2}}$	I/O	Transmission request

Note: The MRESET/SCK2 pin functions as the $\overline{\text{MRESET}}$ manual reset pin when a manual reset is executed. The MD1/TxD2, MD2/RxD2, and MD8/$\overline{\text{RTS2}}$ pins function as the MD1, MD2, and MD8 mode input pins after a power-on reset. These pins are made to function as serial pins by performing SCIF operation settings with the TE and RE bits in SCSCR2 and the MCE bit in SCFCR2. Break state transmission and detection can be set in the SCIF's SCSPTR2 register.

Interrupt Source		INTEVT Code	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Unit	Default Priority
TMU3	TUNI3*2	H'B00	15–0 (0)	INTPRI00 (11–8)	—	High
TMU4	TUNI4*2	H'B80	15–0 (0)	INTPRI00 (15–12)	—	
TMU0	TUNI0	H'400	15–0 (0)	IPRA (15–12)	—	
TMU1	TUNI1	H'420	15–0 (0)	IPRA (11–8)	—	
TMU2	TUNI2	H'440	15–0 (0)	IPRA (7–4)	High	
	TICPI2	H'460			Low	
RTC	ATI	H'480	15–0 (0)	IPRA (3–0)	High	
	PRI	H'4A0				
	CUI	H'4C0			Low	
SCI	ERI	H'4E0	15–0 (0)	IPRB (7–4)	High	
	RXI	H'500				
	TXI	H'520				
	TEI	H'540			Low	
SCIF	ERI	H'700	15–0 (0)	IPRC (7–4)	High	
	RXI	H'720				
	BRI	H'740				
	TXI	H'760			Low	
WDT	ITI	H'560	15–0 (0)	IPRB (15–12)	—	
REF	RCMI	H'580	15–0 (0)	IPRB (11–8)	High	
	ROVI	H'5A0			Low	Low

Legend:

TUNI0–TUNI4: Underflow interrupts

TICPI2: Input capture interrupt

ATI: Alarm interrupt

PRI: Periodic interrupt

CUI: Carry-up interrupt

ERI: Receive-error interrupt

RXI: Receive-data-full interrupt

TXI: Transmit-data-empty interrupt

TEI: Transmit-end interrupt

BRI: Break interrupt request

ITI: Interval timer interrupt

Table 22.7 DC Characteristics (HD6417750SF200 (V))

T_a = –20 to +75°C

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Power supply voltage		V_{DDQ} $V_{DD-PLL1/2}$ V_{DD-CPG} V_{DD-RTC}	3.0	3.3	3.6	V	Normal mode, sleep mode, deep sleep mode, standby mode
		V_{DD}	1.8	1.95	2.07		Normal mode, sleep mode, deep sleep mode, standby mode
Current dissipation	Normal operation	I_{DD}	—	410	780	mA	Ick = 200 MHz
	Sleep mode		—	165	210		
	Standby mode		—	—	2000	µA	T_a = 25°C (RTC on*)
			—	—	5000		T_a > 50°C (RTC on*)
Current dissipation	Normal operation	I_{DDQ}	—	140	180	mA	Ick = 200 MHz, Bck = 67 MHz
	Sleep mode		—	40	50		
	Standby mode		—	—	2200	µA	T_a = 25°C (RTC on*)
			—	—	5500		T_a > 50°C (RTC on*)
RTC current dissipation	During RTC operation	I_{DD-RTC}	—	15	25	µA	RTC input clock: 32.768 kHz Power is supplied only to V_{DD-RTC}
Input voltage	$\overline{\text{RESET}}$, NMI, $\overline{\text{TRST}}$	V_{IH}	V_{DDQ} × 0.9	—	V_{DDQ} + 0.3	V	
	Other input pins		2.0	—	V_{DDQ} + 0.3		
	$\overline{\text{RESET}}$, NMI, $\overline{\text{TRST}}$	V_{IL}	–0.3	—	V_{DDQ} × 0.1		
	Other input pins		–0.3	—	V_{DDQ} × 0.2		
Output voltage	All output pins	V_{OH}	2.4	—	—	V	I_{OH} = –2 mA
		V_{OL}	—	—	0.55		I_{OL} = 2 mA

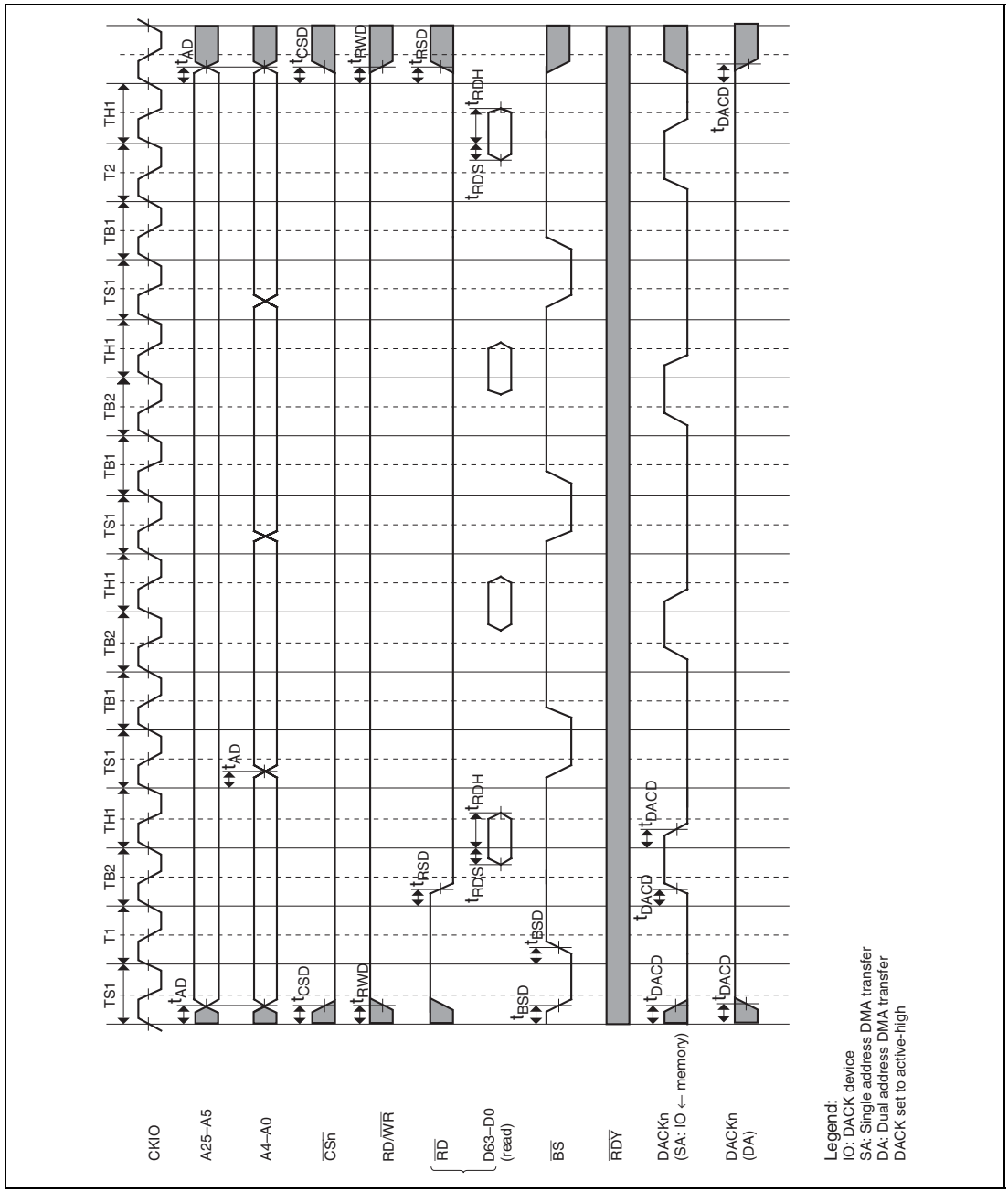


Figure 22.21 Burst ROM Bus Cycle
(No Wait, Address Setup/Hold Time Insertion, AnS = 1, AnH = 1)