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Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128ga202-e-ss

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TABLE 1-3: PIC24FJ128GA204 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locator			I/O	Input Buffer	Description
	28-Pin SPDIP/SOIC/ SSOP	28-Pin QFN-S	44-Pin TQFP/QFN			
CN0	12	9	34	—	—	Interrupt-on-Change Inputs.
CN1	11	8	33	—	—	
CN2	2	27	19	—	—	
CN3	3	28	20	—	—	
CN4	4	1	21	—	—	
CN5	5	2	22	—	—	
CN6	6	3	23	—	—	
CN7	7	4	24	—	—	
CN8	—	—	25	—	—	
CN9	—	—	26	—	—	
CN10	—	—	27	—	—	
CN11	26	23	15	—	—	
CN12	25	22	14	—	—	
CN13	24	21	11	—	—	
CN14	23	20	10	—	—	
CN15	22	19	9	—	—	
CN16	21	18	8	—	—	
CN17	—	—	3	—	—	
CN18	—	—	2	—	—	
CN19	—	—	5	—	—	
CN20	—	—	4	—	—	
CN21	18	15	1	—	—	
CN22	17	14	44	—	—	
CN23	16	13	43	—	—	
CN24	15	12	42	—	—	
CN25	—	—	37	—	—	
CN26	—	—	38	—	—	
CN27	14	11	41	—	—	
CN28	—	—	36	—	—	
CN29	10	7	31	—	—	
CN30	9	6	30	—	—	
CN33	—	—	13	—	—	
CN34	—	—	32	—	—	
CN35	—	—	35	—	—	
CN36	—	—	12	—	—	
CTCMP	4	1	21	I	ANA	CTMU Comparator 2 Input (Pulse mode).

Legend: ST = Schmitt Trigger input
TTL = TTL compatible input
I = Input
ANA = Analog input
O = Output
P = Power
I^2C = ST with I^2C™ or SMBus levels

TABLE 1-3: PIC24FJ128GA204 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locator			I/O	Input Buffer	Description
	28-Pin SPDIP/SOIC/ SSOP	28-Pin QFN-S	44-Pin TQFP/QFN			
PMA0/PMALL	—	—	3	O	—	Parallel Master Port Address.
PMA1/PMALH	—	—	2	O	—	
PMA14/PMCS/ PMCS1	—	—	15	O	—	
PMA2/PMALU	—	—	12	O	—	
PMA3	—	—	38	O	—	
PMA4	—	—	37	O	—	
PMA5	—	—	4	O	—	
PMA6	—	—	5	O	—	
PMA7	—	—	13	O	—	
PMA8	—	—	32	O	—	
PMA9	—	—	35	O	—	
PMACK1	—	—	27	I	ST/TTL	Parallel Master Port Acknowledge Input 1.
PMBE0	—	—	36	O	—	Parallel Master Port Byte Enable 0 Strobe.
PMBE1	—	—	25	O	—	Parallel Master Port Byte Enable 1 Strobe.
PMCS1	—	—	30	I/O	ST/TTL	Parallel Master Port Chip Select 1 Strobe.
PMD0	—	—	10	I/O	ST/TTL	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes).
PMD1	—	—	9	I/O	ST/TTL	
PMD2	—	—	8	I/O	ST/TTL	
PMD3	—	—	1	I/O	ST/TTL	
PMD4	—	—	44	I/O	ST/TTL	
PMD5	—	—	43	I/O	ST/TTL	
PMD6	—	—	42	I/O	ST/TTL	
PMD7	—	—	41	I/O	ST/TTL	
PMRD	—	—	11	O	—	Parallel Master Port Read Strobe.
PMWR	—	—	14	O	—	Parallel Master Port Write Strobe.
RA0	2	27	19	I/O	ST	PORTA Digital I/Os.
RA1	3	28	20	I/O	ST	
RA2	9	6	30	I/O	ST	
RA3	10	7	31	I/O	ST	
RA4	12	9	34	I	ST	
RA7	—	—	13	I/O	ST	
RA8	—	—	32	I/O	ST	
RA9	—	—	35	I/O	ST	
RA10	—	—	12	I/O	ST	

Legend: ST = Schmitt Trigger input
ANA = Analog input
I^2C = ST with I^2C™ or SMBus levels
TTL = TTL compatible input
O = Output
I = Input
P = Power

TABLE 4-9: I²C™ REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1RCV	02DA	—	—	—	—	—	—	—	—	I2C1 Receive Register								0000
I2C1TRN	02DC	—	—	—	—	—	—	—	—	I2C1 Transmit Register								00FF
I2C1BRG	02DE	—	—	—	—	Baud Rate Generator Register												0000
I2C1CONL	02E0	I2CEN	—	I2CSIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1CONH	02E2	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
I2C1STAT	02E4	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/$\overline{A}$	P	S	R/$\overline{W}$	RBF	TBF	0000
I2C1ADD	02E6	—	—	—	—	—	—	I2C1 Address Register										0000
I2C1MSK	02E8	—	—	—	—	—	—	I2C1 Address Mask Register										0000
I2C2RCV	02EA	—	—	—	—	—	—	—	—	I2C2 Receive Register								0000
I2C2TRN	02EC	—	—	—	—	—	—	—	—	I2C2 Transmit Register								00FF
I2C2BRG	02EE	—	—	—	—	Baud Rate Generator Register												0000
I2C2CONL	02F0	I2CEN	—	I2CSIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C2CONH	02F2	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
I2C2STAT	02F4	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/$\overline{A}$	P	S	R/$\overline{W}$	RBF	TBF	0000
I2C2ADD	02F6	—	—	—	—	—	—	I2C2 Address Register										0000
I2C2MSK	02F8	—	—	—	—	—	—	I2C2 Address Mask Register										0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-34: EDS MEMORY ADDRESS WITH DIFFERENT PAGES AND ADDRESSES

DSRPAG (Data Space Read Register)	DSWPAG (Data Space Write Register)	Source/Destination Address While Indirect Addressing	24-Bit EA Pointing to EDS	Comment
x(1)	x(1)	0000h to 1FFFh	000000h to 001FFFh	Near Data Space(2)
		2000h to 7FFFh	002000h to 007FFFh	
001h	001h	8000h to FFFFh	008000h to 00FFFEh	EPMP Memory Space
002h	002h		010000h to 017FFEh	
003h • • • • • 1FFh	003h • • • • • 1FFh		018000h to 0187FEh • • • • FF8000h to FFFFFEh	
000h	000h		Invalid Address	Address Error Trap(3)

Note 1: If the source/destination address is below 8000h, the DSRPAG and DSWPAG registers are not considered.

2: This Data Space can also be accessed by Direct Addressing.

3: When the source/destination address is above 8000h and DSRPAG/DSWPAG are '0', an address error trap will occur.

4.2.6 SOFTWARE STACK

Apart from its use as a Working register, the W15 register in PIC24F devices is also used as a Software Stack Pointer (SSP). The pointer always points to the first available free word and grows from lower to higher addresses. It predecrements for stack pops and post-increments for stack pushes, as shown in Figure 4-7. Note that for a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, ensuring that the MSB is always clear.

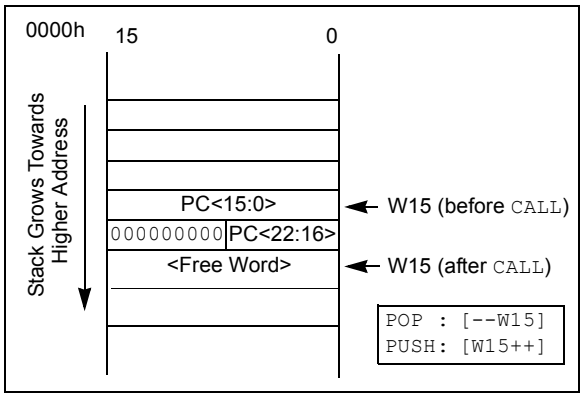
Note:	A PC push during exception processing will concatenate the SRL Register to the MSB of the PC prior to the push.

The Stack Pointer Limit Value (SPLIM) register, associated with the Stack Pointer, sets an upper address boundary for the stack. SPLIM is uninitialized at Reset. As is the case for the Stack Pointer, SPLIM<0> is forced to '0' as all stack operations must be word-aligned. Whenever an EA is generated using W15 as a Source or Destination Pointer, the resulting address is compared with the value in SPLIM. If the contents of the Stack Pointer (W15) and the SPLIM register are equal, and a push operation is performed, a stack error trap will not occur. The stack error trap will occur on a subsequent push operation. Thus, for example, if it is desirable to cause a stack error trap when the stack grows beyond address, 2000h in RAM, initialize the SPLIM with the value, 1FFEh.

Similarly, a Stack Pointer underflow (stack error) trap is generated when the Stack Pointer address is found to be less than 0800h. This prevents the stack from interfering with the SFR space.

A write to the SPLIM register should not be immediately followed by an indirect read operation using W15.

FIGURE 4-7: CALL STACK FRAME



5.0 DIRECT MEMORY ACCESS CONTROLLER (DMA)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Direct Memory Access Controller (DMA)"** (DS39742). The information in this data sheet supersedes the information in the FRM.

The Direct Memory Access (DMA) Controller is designed to service high data throughput peripherals operating on the SFR bus, allowing them to access data memory directly and alleviating the need for CPU intensive management. By allowing these data-intensive peripherals to share their own data path, the main data bus is also deloaded, resulting in additional power savings.

The DMA Controller functions both as a peripheral and a direct extension of the CPU. It is located on the microcontroller data bus between the CPU and DMA-enabled peripherals, with direct access to SRAM. This partitions the SFR bus into two buses, allowing the DMA Controller access to the DMA capable peripherals located on the new DMA SFR bus. The controller serves as a master device on the DMA SFR bus, controlling data flow from DMA capable peripherals.

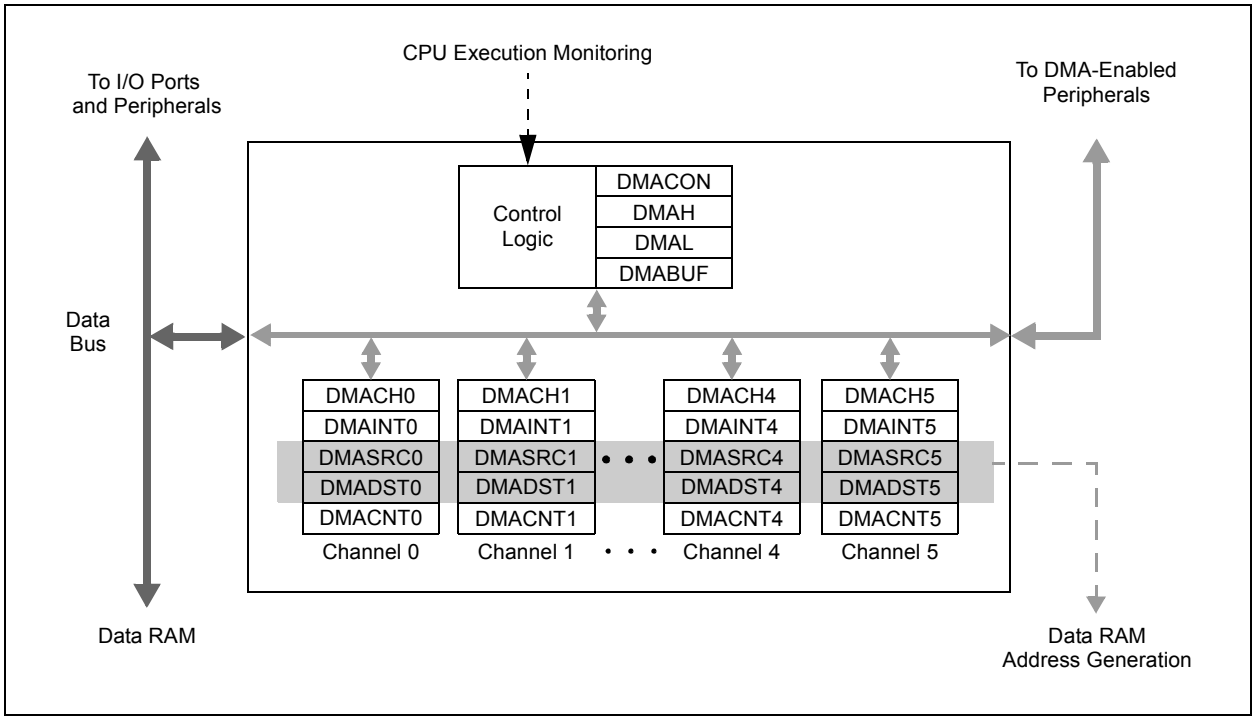
The controller also monitors CPU instruction processing directly, allowing it to be aware of when the CPU requires access to peripherals on the DMA bus and automatically relinquishing control to the CPU as needed. This increases the effective bandwidth for handling data without DMA operations causing a processor stall. This makes the controller essentially transparent to the user.

The DMA Controller has these features:

- Six multiple independent and independently programmable channels
- Concurrent operation with the CPU (no DMA caused Wait states)
- DMA bus arbitration
- Five Programmable Address modes
- Four Programmable Transfer modes
- Four Flexible Internal Data Transfer modes
- Byte or word support for data transfer
- 16-Bit Source and Destination Address register for each channel, dynamically updated and reloadable
- 16-Bit Transaction Count register, dynamically updated and reloadable
- Upper and Lower Address Limit registers
- Counter half-full level interrupt
- Software triggered transfer
- Null Write mode for symmetric buffer operations

A simplified block diagram of the DMA Controller is shown in Figure 5-1.

FIGURE 5-1: DMA FUNCTIONAL BLOCK DIAGRAM



REGISTER 8-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0 (CONTINUED)

bit 2 **OC1IF:** Output Compare Channel 1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **IC1IF:** Input Capture Channel 1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **INT0IF:** External Interrupt 0 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 8-18: IEC5: INTERRUPT ENABLE CONTROL REGISTER 5

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	SPI3TXIE	SPI3IE	U4TXIE	U4RXIE
bit 15							bit 8

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
U4ERIE	—	I2C2BCIE	I2C1BCIE	U3TXIE	U3RXIE	U3ERIE	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11 **SPI3TXIE:** SPI3 Transmit Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 10 **SPI3IE:** SPI3 General Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 9 **U4TXIE:** UART4 Transmitter Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 8 **U4RXIE:** UART4 Receiver Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 7 **U4ERIE:** UART4 Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 6 **Unimplemented:** Read as '0'

bit 5 **I2C2BCIE:** I2C2 Bus Collision Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 4 **I2C1BCIE:** I2C1 Bus Collision Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 3 **U3TXIE:** UART3 Transmitter Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 2 **U3RXIE:** UART3 Receiver Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **U3ERIE:** UART3 Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **Unimplemented:** Read as '0'

REGISTER 10-3: RCON2: RESET AND SYSTEM CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	r-0	R/CO-1	R/CO-1	R/CO-1	R/CO-0
—	—	—	—	VDDBOR(1)	VDDPOR(1,2)	VBPOR(1,3)	VBAT(1)
bit 7							bit 0

Legend:	CO = Clearable Only bit	r = Reserved bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4 **Reserved:** Maintain as '0'

bit 3 **VDDBOR:** VDD Brown-out Reset Flag bit(1)
1 = A VDD Brown-out Reset has occurred (set by hardware)
0 = A VDD Brown-out Reset has not occurred

bit 2 **VDDPOR:** VDD Power-on Reset Flag bit(1,2)
1 = A VDD Power-on Reset has occurred (set by hardware)
0 = A VDD Power-on Reset has not occurred

bit 1 **VBPOR:** VBAT Power-on Reset Flag bit(1,3)
1 = A VBAT POR has occurred (no battery connected to the VBAT pin or VBAT power is below Deep Sleep Semaphore retention level; set by hardware)
0 = A VBAT POR has not occurred

bit 0 **VBAT:** VBAT Flag bit(1)
1 = A POR exit has occurred while power is applied to the VBAT pin (set by hardware)
0 = A POR exit from VBAT has not occurred

Note 1: This bit is set in hardware only; it can only be cleared in software.

2: This bit indicates a VDD Power-on Reset. Setting the POR bit (RCON<0>) indicates a VCORE Power-on Reset.

3: This bit is set when the device is originally powered up, even if power is present on VBAT.

REGISTER 11-3: ANSC: PORTC ANALOG FUNCTION SELECTION REGISTER(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1
—	—	—	—	—	ANSC<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as '0'

bit 2-0 **ANSC<2:0>:** PORTC Analog Function Selection bits
1 = Pin is configured in Analog mode; I/O port read is disabled
0 = Pin is configured in Digital mode; I/O port read is enabled

Note 1: These pins are not available in 28-pin devices.

REGISTER 13-2: TyCON: TIMER3 AND TIMER5 CONTROL REGISTER(1)

R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
TON(2)	—	TSIDL(2)	—	—	—	TECS1(2,3)	TECS0(2,3)
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
—	TGATE(2)	TCKPS1(2)	TCKPS0(2)	—	—	TCS(2,3)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timery On bit(2)
1 = Starts 16-bit Timery
0 = Stops 16-bit Timery

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timery Stop in Idle Mode bit(2)
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9-8 **TECS<1:0>:** Timery Extended Clock Source Select bits (selected when TCS = 1)(2,3)
11 = Generic Timer (TMRCK) External Input
10 = LPRC Oscillator
01 = TxCK External Clock Input
00 = SOSC

bit 7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timery Gated Time Accumulation Enable bit(2)
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timery Input Clock Prescale Select bits(2)
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timery Clock Source Select bit(2,3)
1 = External clock from pin, TyCK (on the rising edge)
0 = Internal clock (FOSC/2)

bit 0 **Unimplemented:** Read as '0'

Note 1: Changing the value of TyCON while the timer is running (TON = 1) causes the timer prescale counter to reset and is not recommended.

2: When 32-bit operation is enabled (T2CON<3> or T4CON<3> = 1), these bits have no effect on Timery operation; all timer functions are set through T2CON and T4CON.

3: If TCS = 1 and TECS<1:0> = x1, the selected external timer input (TyCK) must be configured to an available RPn/RPIn pin. For more information, see **Section 11.4 "Peripheral Pin Select (PPS)"**.

REGISTER 17-3: I2CxSTAT: I2Cx STATUS REGISTER

R-0, HSC	R-0, HSC	R-0, HSC	U-0	U-0	R/C-0, HSC	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10
bit 15							bit 8

R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D/$\overline{A}$	P	S	R/$\overline{W}$	RBF	TBF
bit 7							bit 0

Legend:	C = Clearable bit	HS = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	HS = Hardware Settable bit

bit 15 **ACKSTAT:** Acknowledge Status bit (updated in all Master and Slave modes)
1 = Acknowledge was not received from slave
0 = Acknowledge was received from slave

bit 14 **TRSTAT:** Transmit Status bit (when operating as I^2C™ master; applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress

bit 13 **ACKTIM:** Acknowledge Time Status bit (valid in I^2C Slave mode only)
1 = Indicates I^2C bus is in an Acknowledge sequence, set on 8th falling edge of SCLx clock
0 = Not an Acknowledge sequence, cleared on 9th rising edge of SCLx clock

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Bus Collision Detect bit (Master/Slave mode; cleared when I^2C module is disabled, I2CEN = 0)
1 = A bus collision has been detected during a master or slave transmit operation
0 = No bus collision has been detected

bit 9 **GCSTAT:** General Call Status bit (cleared after Stop detection)
1 = General call address was received
0 = General call address was not received

bit 8 **ADD10:** 10-Bit Address Status bit (cleared after Stop detection)
1 = 10-bit address was matched
0 = 10-bit address was not matched

bit 7 **IWCOL:** I2Cx Write Collision Detect bit
1 = An attempt to write to the I2CxTRN register failed because the I^2C module is busy; must be cleared in software
0 = No collision

bit 6 **I2COV:** I2Cx Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte; I2COV is a "don't care" in Transmit mode, must be cleared in software
0 = No overflow

bit 5 **D/$\overline{A}$:** Data/$\overline{\text{Address}}$ bit (when operating as I^2C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received or transmitted was an address

bit 4 **P:** I2Cx Stop bit
Updated when Start, Reset or Stop is detected; cleared when the I^2C module is disabled, I2CEN = 0.
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last

TABLE 20-1: MEMORY ADDRESSABLE IN DIFFERENT MODES

Data Port Size	PMA<9:8>	PMA<7:0>	PMD<7:4>	PMD<3:0>	Accessible memory
Demultiplexed Address (ADRMUX<1:0> = 00)					
8-Bit (PTSZ<1:0> = 00)	Addr<9:8>	Addr<7:0>	Data		1K
4-Bit (PTSZ<1:0> = 01)	Addr<9:8>	Addr<7:0>	—	Data	1K
1 Address Phase (ADRMUX<1:0> = 01)					
8-Bit (PTSZ<1:0> = 00)	—	PMALL	Addr<7:0> Data		1K
4-Bit (PTSZ<1:0> = 01)	Addr<9:8>	PMALL	Addr<7:4>	Addr<3:0>	1K
			—	Data (1)	
2 Address Phases (ADRMUX<1:0> = 10)					
8-Bit (PTSZ<1:0> = 00)	—	PMALL	Addr<7:0>		64K
		PMALH	Addr<15:8>		
		—	Data		
4-Bit (PTSZ<1:0> = 01)	Addr<9:8>	PMALL	Addr<3:0>		1K
		PMALH	Addr<7:4>		
		—	Data		
3 Address Phases (ADRMUX<1:0> = 11)					
8-Bit (PTSZ<1:0> = 00)	—	PMALL	Addr<7:0>		2 Mbytes
		PMALH	Addr<15:8>		
		PMALU	Addr<22:16>		
		—	Data		
4-Bit (PTSZ<1:0> = 01)	Addr<13:12>	PMALL	Addr<3:0>		16K
		PMALH	Addr<7:4>		
		PMALU	Addr<11:8>		
		—	Data		

REGISTER 22-1: CRYCONL: CRYPTOGRAPHIC CONTROL LOW REGISTER (CONTINUED)

bit 7-4 **OPMOD<3:0>:** Operating Mode Selection bits(1,2)

1111 = Loads session key (decrypt session key in CRYTXTA/CRYTXTB using the Key Encryption Key and write to CRYKEY)
1110 = Encrypts session key (encrypt session key in CRYKEY using the Key Encryption Key and write to CRYTXTA/CRYTXTB)
1011 = Reserved
1010 = Generate a random number
1001
•
• = Reserved
•
0011
0010 = AES decryption key expansion
0001 = Decryption
0000 = Encryption

bit 3 **CPHRSEL:** Cipher Engine Select bit(1,2)

1 = AES engine
0 = DES engine

bit 2-0 **CPHRMOD<2:0>:** Cipher Mode bits(1,2)

11x = Reserved
101 = Reserved
100 = Counter (CTR) mode
011 = Output Feedback (OFB) mode
010 = Cipher Feedback (CFB) mode
001 = Cipher Block Chaining (CBC) mode
000 = Electronic Codebook (ECB) mode

Note 1: These bits are reset on system Resets or whenever the CRYMD bit is set.
2: Writes to these bit fields are locked out whenever an operation is in progress (CRYGO bit is set).
3: If the device enters Idle mode when CRYSIDL = 1, the module will stop its current operation. Entering into Idle mode while an OTP write operation is in process can result in irreversible corruption of the OTP.

REGISTER 22-2: CRYCONH: CRYPTOGRAPHIC CONTROL HIGH REGISTER

U-0	R/W-0(1)	R/W-0(1)	R/W-0(1)	R/W-0(1)	R/W-0(1)	R/W-0(1)	R/W-0(1)
—	CTRSIZE6(2,3)	CTRSIZE5(2,3)	CTRSIZE4(2,3)	CTRSIZE3(2,3)	CTRSIZE2(2,3)	CTRSIZE1(2,3)	CTRSIZE0(2,3)
bit 15							bit 8

R/W-0(1)	R/W-0(1)	R/W-0(1)	U-0	R/W-0(1)	R/W-0(1)	R/W-0(1)	R/W-0(1)
SKEYSEL	KEYMOD1(2)	KEYMOD0(2)	—	KEYSRC3(2)	KEYSRC2(2)	KEYSRC1(2)	KEYSRC0(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **CTRSIZE<6:0>:** Counter Size Select bits(1,2,3)
Counter is defined as CRYTXTB<n:0>, where n = CTRSIZEx. The counter increments after each operation and generates a rollover event when the counter rolls over from (2^{n-1} – 1) to 0.
1111111 = 128 bits (CRYTXTB<127:0>)
1111110 = 127 bits (CRYTXTB<126:0>)
•
•
•
0000010 = 3 bits (CRYTXTB<2:0>)
0000001 = 2 bits (CRYTXTB<1:0>)
0000000 = 1 bit (CRYTXTB<0>); rollover event occurs when CRYTXTB<0> toggles from '1' to '0'

bit 7 **SKEYSEL:** Session Key Select bit(1)
1 = Key generation/encryption/loading performed with CRYKEY<255:128>
0 = Key generation/encryption/loading performed with CRYKEY<127:0>

bit 6-5 **KEYMOD<1:0>:** AES/DES Encrypt/Decrypt Key Mode/Key Length Select bits(1,2)
For DES Encrypt/Decrypt Operations (CPHRSEL = 0):
11 = 64-bit, 3-key 3DES
10 = Reserved
01 = 64-bit, standard 2-key 3DES
00 = 64-bit DES
For AES Encrypt/Decrypt Operations (CPHRSEL = 1):
11 = Reserved
10 = 256-bit AES
01 = 192-bit AES
00 = 128-bit AES

bit 4 **Unimplemented:** Read as '0'

bit 3-0 **KEYSRC<3:0>:** Cipher Key Source bits(1,2)
Refer to Table 22-1 and Table 22-2 for KEYSRC<3:0> values.

Note 1: These bits are reset on system Resets or whenever the CRYMD bit is set.
2: Writes to these bit fields are locked out whenever an operation is in progress (CRYGO bit is set).
3: Used only in CTR operations when CRYTXTB is being used as a counter; otherwise, these bits have no effect.

REGISTER 24-1: AD1CON1: A/D CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADON	—	ADSIDL	DMABM(1)	DMAEN	MODE12	FORM1	FORM0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0, HSC	R/C-0, HSC
SSRC3	SSRC2	SSRC1	SSRC0	—	ASAM	SAMP	DONE
bit 7							bit 0

Legend:	C = Clearable bit	U = Unimplemented bit, read as '0'	
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ADON:** A/D Operating Mode bit
1 = A/D Converter module is operating
0 = A/D Converter is off

bit 14 **Unimplemented:** Read as '0'

bit 13 **ADSIDL:** A/D Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **DMABM:** Extended DMA Buffer Mode Select bit(1)
1 = Extended Buffer mode: Buffer address is defined by the DMADSTn register
0 = PIA mode: Buffer addresses are defined by the DMA Controller and AD1CON4<2:0>

bit 11 **DMAEN:** Extended DMA/Buffer Enable bit
1 = Extended DMA and buffer features are enabled
0 = Extended features are disabled

bit 10 **MODE12:** 12-Bit Operation Mode bit
1 = 12-bit A/D operation
0 = 10-bit A/D operation

bit 9-8 **FORM<1:0>:** Data Output Format bits (see formats following)
11 = Fractional result, signed, left justified
10 = Absolute fractional result, unsigned, left justified
01 = Decimal result, signed, right justified
00 = Absolute decimal result, unsigned, right justified

bit 7-4 **SSRC<3:0>:** Sample Clock Source Select bits
1xxx = Unimplemented, do not use
0111 = Internal counter ends sampling and starts conversion (auto-convert); do not use in Auto-Scan mode
0110 = Unimplemented
0101 = TMR1
0100 = CTMU
0011 = TMR5
0010 = TMR3
0001 = INT0
0000 = The SAMP bit must be cleared by software to start conversion

bit 3 **Unimplemented:** Read as '0'

bit 2 **ASAM:** A/D Sample Auto-Start bit
1 = Sampling begins immediately after last conversion; SAMP bit is auto-set
0 = Sampling begins when SAMP bit is manually set

Note 1: This bit is only available when Extended DMA/Buffer features are available (DMAEN = 1).

REGISTER 28-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
HLVDEN	—	LSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
VDIR	BGVST	IRVST	—	HLVDL3	HLVDL2	HLVDL1	HLVDL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **HLVDEN:** High/Low-Voltage Detect Power Enable bit
1 = HLVD is enabled
0 = HLVD is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **LSIDL:** High/Low-Voltage Detect Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **VDIR:** Voltage Change Direction Select bit
1 = Event occurs when voltage equals or exceeds trip point (HLVDL<3:0>)
0 = Event occurs when voltage equals or falls below trip point (HLVDL<3:0>)

bit 6 **BGVST:** Band Gap Voltage Stable Flag bit
1 = Indicates that the band gap voltage is stable
0 = Indicates that the band gap voltage is unstable

bit 5 **IRVST:** Internal Reference Voltage Stable Flag bit
1 = Internal reference voltage is stable; the High-Voltage Detect logic generates the interrupt flag at the specified voltage range
0 = Internal reference voltage is unstable; the High-Voltage Detect logic will not generate the interrupt flag at the specified voltage range and the HLVD interrupt should not be enabled

bit 4 **Unimplemented:** Read as '0'

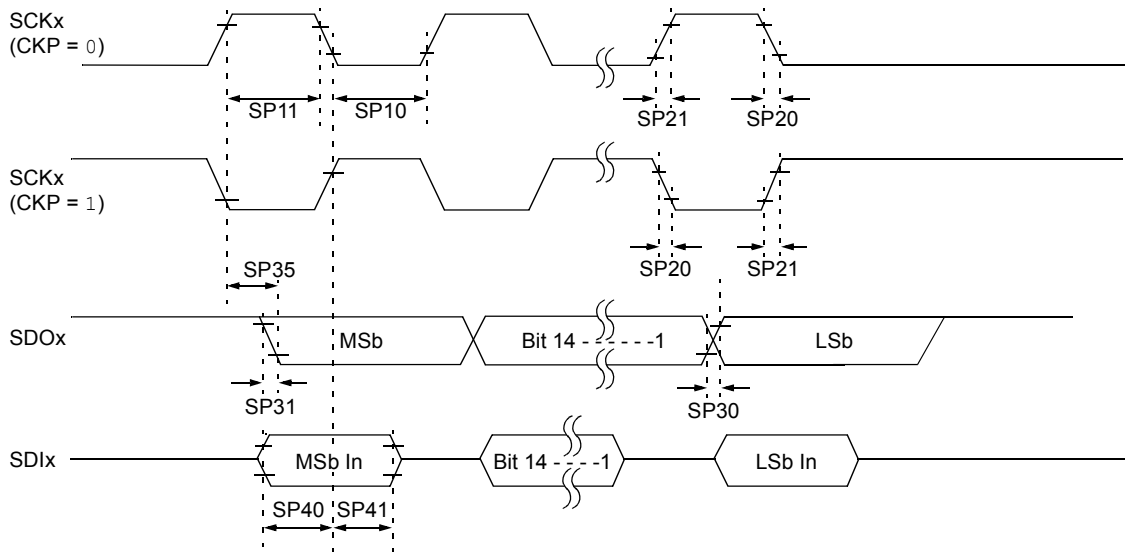
bit 3-0 **HLVDL<3:0>:** High/Low-Voltage Detection Limit bits
1111 = External analog input is used (input comes from the HLVDIN pin)
1110 = Trip Point 1(1)
1101 = Trip Point 2(1)
1100 = Trip Point 3(1)
•
•
•
0100 = Trip Point 11(1)
00xx = Unused

Note 1: For the actual trip point, see **Section 32.0 "Electrical Characteristics"**.

TABLE 31-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
PWRSAV	PWRSAV	#lit1	Go into Sleep or Idle mode	1	1	WDTO, Sleep
RCALL	RCALL	Expr	Relative Call	1	2	None
	RCALL	Wn	Computed Call	1	2	None
REPEAT	REPEAT	#lit14	Repeat Next Instruction lit14 + 1 times	1	1	None
	REPEAT	Wn	Repeat Next Instruction (Wn) + 1 times	1	1	None
RESET	RESET		Software Device Reset	1	1	None
RETFIE	RETFIE		Return from Interrupt	1	3 (2)	None
RETLW	RETLW	#lit10,Wn	Return with Literal in Wn	1	3 (2)	None
RETURN	RETURN		Return from Subroutine	1	3 (2)	None
RLC	RLC	f	f = Rotate Left through Carry f	1	1	C, N, Z
	RLC	f,WREG	WREG = Rotate Left through Carry f	1	1	C, N, Z
	RLC	Ws,Wd	Wd = Rotate Left through Carry Ws	1	1	C, N, Z
RLNC	RLNC	f	f = Rotate Left (No Carry) f	1	1	N, Z
	RLNC	f,WREG	WREG = Rotate Left (No Carry) f	1	1	N, Z
	RLNC	Ws,Wd	Wd = Rotate Left (No Carry) Ws	1	1	N, Z
RRC	RRC	f	f = Rotate Right through Carry f	1	1	C, N, Z
	RRC	f,WREG	WREG = Rotate Right through Carry f	1	1	C, N, Z
	RRC	Ws,Wd	Wd = Rotate Right through Carry Ws	1	1	C, N, Z
RRNC	RRNC	f	f = Rotate Right (No Carry) f	1	1	N, Z
	RRNC	f,WREG	WREG = Rotate Right (No Carry) f	1	1	N, Z
	RRNC	Ws,Wd	Wd = Rotate Right (No Carry) Ws	1	1	N, Z
SE	SE	Ws,Wnd	Wnd = Sign-Extended Ws	1	1	C, N, Z
SETM	SETM	f	f = FFFFh	1	1	None
	SETM	WREG	WREG = FFFFh	1	1	None
	SETM	Ws	Ws = FFFFh	1	1	None
SL	SL	f	f = Left Shift f	1	1	C, N, OV, Z
	SL	f,WREG	WREG = Left Shift f	1	1	C, N, OV, Z
	SL	Ws,Wd	Wd = Left Shift Ws	1	1	C, N, OV, Z
	SL	Wb,Wns,Wnd	Wnd = Left Shift Wb by Wns	1	1	N, Z
	SL	Wb,#lit5,Wnd	Wnd = Left Shift Wb by lit5	1	1	N, Z
SUB	SUB	f	f = f – WREG	1	1	C, DC, N, OV, Z
	SUB	f,WREG	WREG = f – WREG	1	1	C, DC, N, OV, Z
	SUB	#lit10,Wn	Wn = Wn – lit10	1	1	C, DC, N, OV, Z
	SUB	Wb,Ws,Wd	Wd = Wb – Ws	1	1	C, DC, N, OV, Z
	SUB	Wb,#lit5,Wd	Wd = Wb – lit5	1	1	C, DC, N, OV, Z
SUBB	SUBB	f	f = f – WREG – ($\overline{C}$)	1	1	C, DC, N, OV, Z
	SUBB	f,WREG	WREG = f – WREG – ($\overline{C}$)	1	1	C, DC, N, OV, Z
	SUBB	#lit10,Wn	Wn = Wn – lit10 – ($\overline{C}$)	1	1	C, DC, N, OV, Z
	SUBB	Wb,Ws,Wd	Wd = Wb – Ws – ($\overline{C}$)	1	1	C, DC, N, OV, Z
	SUBB	Wb,#lit5,Wd	Wd = Wb – lit5 – ($\overline{C}$)	1	1	C, DC, N, OV, Z
SUBR	SUBR	f	f = WREG – f	1	1	C, DC, N, OV, Z
	SUBR	f,WREG	WREG = WREG – f	1	1	C, DC, N, OV, Z
	SUBR	Wb,Ws,Wd	Wd = Ws – Wb	1	1	C, DC, N, OV, Z
	SUBR	Wb,#lit5,Wd	Wd = lit5 – Wb	1	1	C, DC, N, OV, Z
SUBBR	SUBBR	f	f = WREG – f – ($\overline{C}$)	1	1	C, DC, N, OV, Z
	SUBBR	f,WREG	WREG = WREG – f – ($\overline{C}$)	1	1	C, DC, N, OV, Z
	SUBBR	Wb,Ws,Wd	Wd = Ws – Wb – ($\overline{C}$)	1	1	C, DC, N, OV, Z
	SUBBR	Wb,#lit5,Wd	Wd = lit5 – Wb – ($\overline{C}$)	1	1	C, DC, N, OV, Z
SWAP	SWAP.b	Wn	Wn = Nibble Swap Wn	1	1	None
	SWAP	Wn	Wn = Byte Swap Wn	1	1	None

FIGURE 32-13: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 32-2 for load conditions.

TABLE 32-35: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ(2)**	**Max**	**Units**	**Conditions**
SP10	TscL	SCKx Output Low Time	TCY/2	—	—	ns	**(Note 3)**
SP11	TscH	SCKx Output High Time	TCY/2	—	—	ns	**(Note 3)**
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge	—	6	20	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	23	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

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