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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	AES, Brown-out Detect/Reset, DMA, I <sup>2</sup> S, HLVD, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128ga202t-i-ss">https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128ga202t-i-ss</a>

# PIC24FJ128GA204 FAMILY

## 1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC24FJ64GA202
- PIC24FJ128GA202
- PIC24FJ64GA204
- PIC24FJ128GA204

The PIC24FJ128GA204 family expands the capabilities of the PIC24F family by adding a complete selection of Cryptographic Engines, ISO 7816 support and I<sup>2</sup>S support to its existing features. This combination, along with its ultra low-power features and Direct Memory Access (DMA) for peripherals, make this family the new standard for mixed-signal PIC® microcontrollers in one economical and power-saving package.

### 1.1 Core Features

#### 1.1.1 16-BIT ARCHITECTURE

Central to all PIC24F devices is the 16-bit modified Harvard architecture, first introduced with Microchip's dsPIC® Digital Signal Controllers (DSCs). The PIC24F CPU core offers a wide range of enhancements, such as:

- 16-bit data and 24-bit address paths with the ability to move information between data and memory spaces
- Linear addressing of up to 12 Mbytes (program space) and 32 Kbytes (data)
- A 16-element Working register array with built-in software stack support
- A 17 x 17 hardware multiplier with support for integer math
- Hardware support for 32 by 16-bit division
- An instruction set that supports multiple addressing modes and is optimized for high-level languages, such as 'C'
- Operational performance up to 16 MIPS

#### 1.1.2 XLP POWER-SAVING TECHNOLOGY

The PIC24FJ128GA204 family of devices introduces a greatly expanded range of power-saving operating modes for the ultimate in power conservation. The new modes include:

- Retention Sleep, with essential circuits being powered from a separate low-voltage regulator
- Deep Sleep without RTCC, for the lowest possible power consumption under software control
- VBAT mode (with or without RTCC), to continue limited operation from a backup battery when VDD is removed

Many of these new low-power modes also support the continuous operation of the low-power, on-chip Real-Time Clock/Calendar (RTCC), making it possible for an application to keep time while the device is otherwise asleep.

Aside from these new features, PIC24FJ128GA204 family devices also include all of the legacy power-saving features of previous PIC24F microcontrollers, such as:

- On-the-Fly Clock Switching, allowing the selection of a lower power clock during run time
- Doze Mode Operation, for maintaining peripheral clock speed while slowing the CPU clock
- Instruction-Based Power-Saving Modes, for quick invocation of Idle and the many Sleep modes

#### 1.1.3 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC24FJ128GA204 family offer five different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes
- Two External Clock modes
- A Phase-Locked Loop (PLL) frequency multiplier, which allows clock speeds of up to 32 MHz
- A Fast Internal Oscillator (FRC) – nominal 8 MHz output with multiple frequency divider options and automatic frequency self-calibration during run time
- A separate, Low-Power Internal RC Oscillator (LPRC) – 31 kHz nominal, for low-power, timing-insensitive applications.

The internal oscillator block also provides a stable reference source for the Fail-Safe Clock Monitor (FSCM). This option constantly monitors the main clock source against a reference signal provided by the internal oscillator and enables the controller to switch to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.

#### 1.1.4 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve. This extends the ability of applications to grow from the relatively simple, to the powerful and complex, yet still selecting a Microchip device.

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## 2.4 Voltage Regulator Pins (ENVREG/ DISVREG and VCAP/VDDCORE)

**Note:** This section applies only to PIC24FJ devices with an on-chip voltage regulator.

The on-chip voltage regulator enable/disable pin (ENVREG or DISVREG, depending on the device family) must always be connected directly to either a supply voltage or to ground. The particular connection is determined by whether or not the regulator is to be used:

- For ENVREG, tie to VDD to enable the regulator, or to ground to disable the regulator
- For DISVREG, tie to ground to enable the regulator or to VDD to disable the regulator

Refer to [Section 29.2 “On-Chip Voltage Regulator”](#) for details on connecting and using the on-chip regulator.

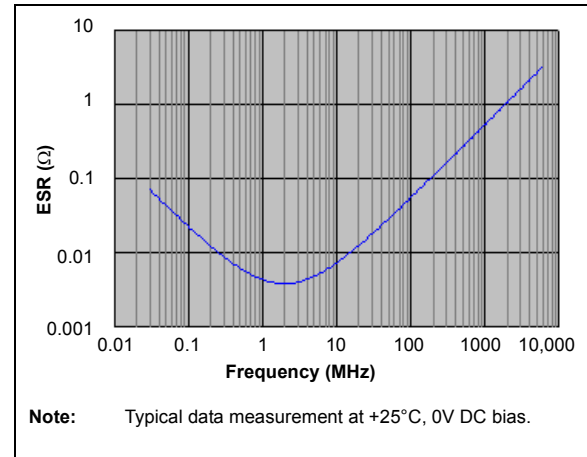
When the regulator is enabled, a low-ESR ( $< 5\Omega$ ) capacitor is required on the VCAP/VDDCORE pin to stabilize the voltage regulator output voltage. The VCAP/VDDCORE pin must not be connected to VDD and must use a capacitor of 10  $\mu\text{F}$  connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in [Table 2-1](#). Capacitors with equivalent specifications can be used.

Designers may use [Figure 2-3](#) to evaluate ESR equivalence of candidate devices.

The placement of this capacitor should be close to VCAP/VDDCORE. It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to [Section 32.0 “Electrical Characteristics”](#) for additional information.

When the regulator is disabled, the VCAP/VDDCORE pin must be tied to a voltage supply at the VDDCORE level. Refer to [Section 32.0 “Electrical Characteristics”](#) for information on VDD and VDDCORE.

**FIGURE 2-3: FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP**

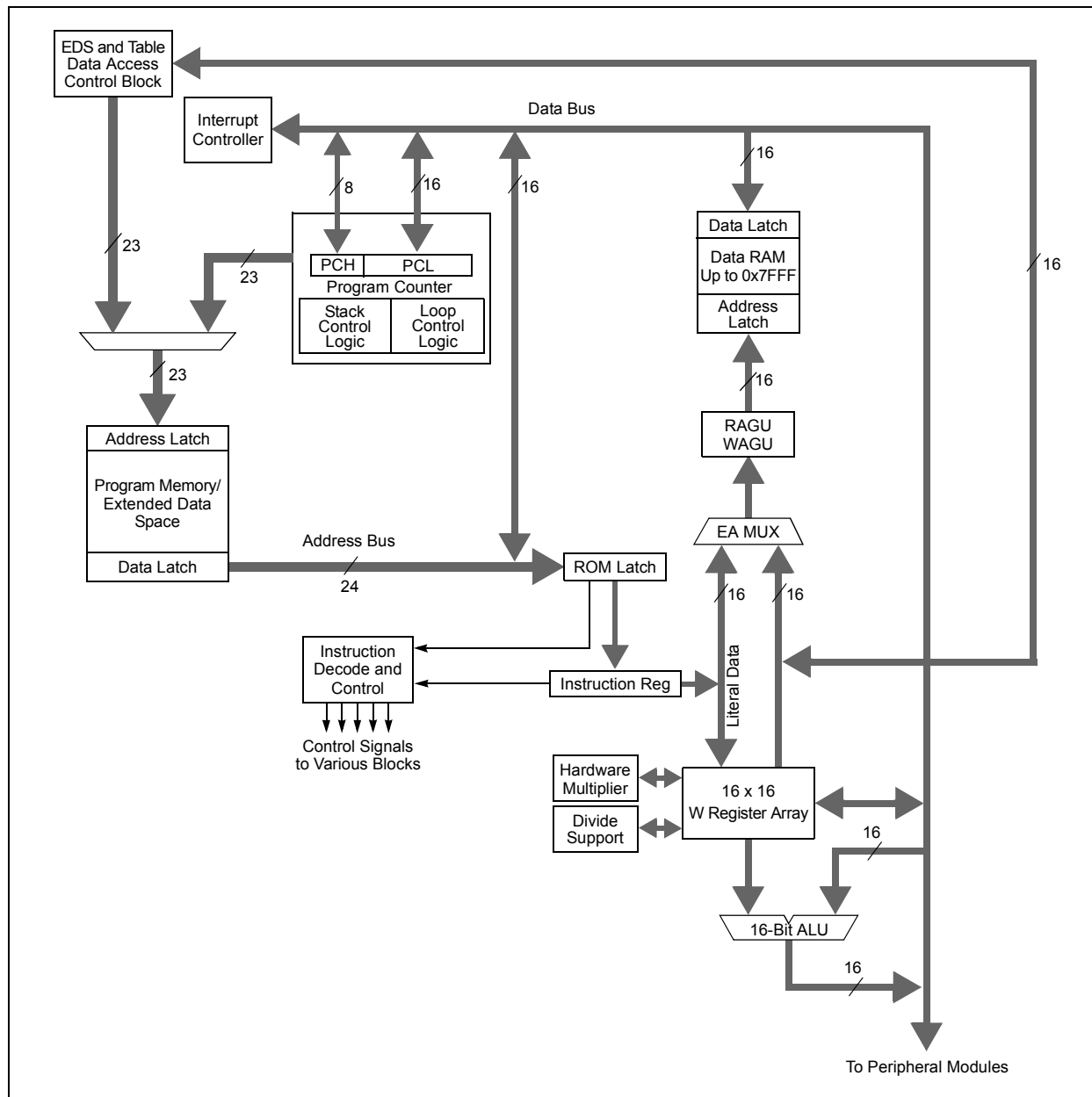


**TABLE 2-1: SUITABLE CAPACITOR EQUIVALENTS**

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 $\mu\text{F}$	$\pm 10\%$	16V	-55 to +125°C
TDK	C3216X5R1C106K	10 $\mu\text{F}$	$\pm 10\%$	16V	-55 to +85°C
Panasonic	ECJ-3YX1C106K	10 $\mu\text{F}$	$\pm 10\%$	16V	-55 to +125°C
Panasonic	ECJ-4YB1C106K	10 $\mu\text{F}$	$\pm 10\%$	16V	-55 to +85°C
Murata	GRM32DR71C106KA01L	10 $\mu\text{F}$	$\pm 10\%$	16V	-55 to +125°C
Murata	GRM31CR61C106KC31L	10 $\mu\text{F}$	$\pm 10\%$	16V	-55 to +85°C

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**FIGURE 3-1: PIC24F CPU CORE BLOCK DIAGRAM**



**TABLE 3-1: CPU CORE REGISTERS**

Register(s) Name	Description
W0 through W15	Working Register Array
PC	23-Bit Program Counter
SR	ALU STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
RCOUNT	REPEAT Loop Counter Register
CORCON	CPU Control Register
DISICNT	Disable Interrupt Count Register
DSRPAG	Data Space Read Page Register
DSWPAG	Data Space Write Page Register

**TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP**

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	0080	NSTDIS	—	—	—	—	—	—	—	—	—	—	MATHERR	ADDRERR	STKERR	OSCFail	—	0000
INTCON2	0082	ALTVT	DISI	—	—	—	—	—	—	—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
IFS0	0084	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1TXIF	SPI1IF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0086	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	—	—	—	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0088	—	DMA4IF	PMPIF	—	—	OC6IF	OC5IF	IC6IF	IC5IF	IC4IF	IC3IF	DMA3IF	CRYROLLIF	CRYFREEIF	SPI2TXIF	SPI2IF	0000
IFS3	008A	—	RTCIF	DMA5IF	SPI3RXIF	SPI2RXIF	SPI1RXIF	—	KEYSTRIF	CRYDNIF	INT4IF	INT3IF	—	—	MI2C2IF	SI2C2IF	—	0000
IFS4	008C	—	—	CTMUIF	—	—	—	—	HLVDIF	—	—	—	—	CRCIF	U2ERIF	U1ERIF	—	0000
IFS5	008E	—	—	—	—	SPI3TXIF	SPI3IF	U4TXIF	U4RXIF	U4ERIF	—	I2C2BCIF	I2C1BCIF	U3TXIF	U3RXIF	U3ERIF	—	0000
IFS6	0090	—	—	—	—	—	FSTIF	—	—	—	—	—	—	—	—	—	—	0000
IFS7	0092	—	—	—	—	—	—	—	—	—	—	JTAGIF	—	—	—	—	—	0000
IEC0	0094	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1TXIE	SPI1IE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0096	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	—	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0098	—	DMA4IE	PMPIE	—	—	OC6IE	OC5IE	IC6IE	IC5IE	IC4IE	IC3IE	DMA3IE	CRYROLLIE	CRYFREEIE	SPI2TXIE	SPI2IE	0000
IEC3	009A	—	RTCIE	DMA5IE	SPI3RXIE	SPI2RXIE	SPI1RXIE	—	KEYSTRIE	CRYDNIE	INT4IE	INT3IE	—	—	MI2C2IE	SI2C2IE	—	0000
IEC4	009C	—	—	CTMUIE	—	—	—	—	HLVDIE	—	—	—	—	CRCIE	U2ERIE	U1ERIE	—	0000
IEC5	009E	—	—	—	—	SPI3TXIE	SPI3IE	U4TXIE	U4RXIE	U4ERIE	—	I2C2BCIE	I2C1BCIE	U3TXIE	U3RXIE	U3ERIE	—	0000
IEC6	00A0	—	—	—	—	—	FSTIE	—	—	—	—	—	—	—	—	—	—	0000
IEC7	00A2	—	—	—	—	—	—	—	—	—	—	JTAGIE	—	—	—	—	—	0000
IPC0	00A4	—	T1IP2	T1IP1	T1IP0	—	OC1IP2	OC1IP1	OC1IP0	—	IC1IP2	IC1IP1	IC1IP0	—	INT0IP2	INT0IP1	INT0IP0	4444
IPC1	00A6	—	T2IP2	T2IP1	T2IP0	—	OC2IP2	OC2IP1	OC2IP0	—	IC2IP2	IC2IP1	IC2IP0	—	DMA0IP2	DMA0IP1	DMA0IP0	4444
IPC2	00A8	—	U1RXIP2	U1RXIP1	U1RXIP0	—	SPI1TXIP2	SPI1TXIP1	SPI1TXIP0	—	SPI1IP2	SPI1IP1	SPI1IP0	—	T3IP2	T3IP1	T3IP0	4444
IPC3	00AA	—	—	—	—	—	DMA1IP2	DMA1IP1	DMA1IP0	—	AD1IP2	AD1IP1	AD1IP0	—	U1TXIP2	U1TXIP1	U1TXIP0	0444
IPC4	00AC	—	CNIP2	CNIP1	CNIP0	—	CMIP2	CMIP1	CMIP0	—	MI2C1IP2	MI2C1IP1	MI2C1IP0	—	SI2C1IP2	SI2C1IP1	SI2C1IP0	4444
IPC5	00AE	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP<2:0>			0004
IPC6	00B0	—	T4IP2	T4IP1	T4IP0	—	OC4IP2	OC4IP1	OC4IP0	—	OC3IP2	OC3IP1	OC3IP0	—	DMA2IP2	DMA2IP1	DMA2IP0	4444
IPC7	00B2	—	U2TXIP2	U2TXIP1	U2TXIP0	—	U2RXIP2	U2RXIP1	U2RXIP0	—	INT2IP2	INT2IP1	INT2IP0	—	T5IP2	T5IP1	T5IP0	4444
IPC8	00B4	—	CRYROLLIP2	CRYROLLIP1	CRYROLLIP0	—	CRYFREEIP2	CRYFREEIP1	CRYFREEIP0	—	SPI2TXIP2	SPI2TXIP1	SPI2TXIP0	—	SPI2IP2	SPI2IP1	SPI2IP0	4444
IPC9	00B6	—	IC5IP2	IC5IP1	IC5IP0	—	IC4IP2	IC4IP1	IC4IP0	—	IC3IP2	IC3IP1	IC3IP0	—	DMA3IP2	DMA3IP1	DMA3IP0	4444
IPC10	00B8	—	—	—	—	—	OC6IP2	OC6IP1	OC6IP0	—	OC5IP2	OC5IP1	OC5IP0	—	IC6IP2	IC6IP1	IC6IP0	0444
IPC11	00BA	—	—	—	—	—	DMA4IP2	DMA4IP1	DMA4IP0	—	PMPIP2	PMPIP1	PMPIP0	—	—	—	—	0440
IPC12	00BC	—	—	—	—	—	MI2C2IP2	MI2C2IP1	MI2C2IP0	—	SI2C2IP2	SI2C2IP1	SI2C2IP0	—	—	—	—	0440
IPC13	00BE	—	CRYDNIP2	CRYDNIP1	CRYDNIP0	—	INT4IP2	INT4IP1	INT4IP0	—	INT3IP2	INT3IP1	INT3IP0	—	—	—	—	4440
IPC14	00C0	—	SPI2RXIP2	SPI2RXIP1	SPI2RXIP0	—	SPI1RXIP2	SPI1RXIP1	SPI1RXIP0	—	—	—	—	—	KEYSTRIP2	KEYSTRIP1	KEYSTRIP0	4404
IPC15	00C2	—	—	—	—	—	RTCIP2	RTCIP1	RTCIP0	—	DMA5IP2	DMA5IP1	DMA5IP0	—	SPI3RXIP2	SPI3RXIP1	SPI3RXIP0	0444

**Legend:** — = unimplemented, read as '0'; r = reserved, maintain as '0'. Reset values are shown in hexadecimal.

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## 4.3 Interfacing Program and Data Memory Spaces

The PIC24F architecture uses a 24-bit wide program space and 16-bit wide Data Space. The architecture is also a modified Harvard scheme, meaning that data can also be present in the program space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the PIC24F architecture provides two methods by which program space can be accessed during operation:

- Using table instructions to access individual bytes or words anywhere in the program space
- Remapping a portion of the program space into the Data Space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This makes the method ideal for accessing data tables that need to be updated from time to time. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. It can only access the least significant word of the program word.

### 4.3.1 ADDRESSING PROGRAM SPACE

Since the address ranges for the data and program spaces are 16 and 24 bits, respectively, a method is needed to create a 23-bit or 24-bit program address from 16-bit Data registers. The solution depends on the interface method to be used.

For table operations, the 8-bit Table Memory Page Address register (TBLPAG) is used to define a 32K word region within the program space. This is concatenated with a 16-bit EA to arrive at a full 24-bit program space address. In this format, the MSBs of TBLPAG are used to determine if the operation occurs in the user memory (TBLPAG<7> = 0) or the configuration memory (TBLPAG<7> = 1).

For remapping operations, the 10-bit Extended Data Space Read register (DSRPAG) is used to define a 16K word page in the program space. When the Most Significant bit (MSb) of the EA is '1' and the MSb (bit 9) of DSRPAG is '1', the lower 8 bits of DSRPAG are concatenated with the lower 15 bits of the EA to form a 23-bit program space address. The DSRPAG<8> bit decides whether the lower word (when the bit is '0') or the higher word (when the bit is '1') of program memory is mapped. Unlike table operations, this strictly limits remapping operations to the user memory area.

Table 4-35 and Figure 4-8 show how the program EA is created for table operations and remapping accesses from the data EA. Here, the P<23:0> bits refer to a program space word, whereas the D<15:0> bits refer to a Data Space word.

**TABLE 4-35: PROGRAM SPACE ADDRESS CONSTRUCTION**

Access Type	Access Space	Program Space Address				
		<23>	<22:16>	<15>	<14:1>	<0>
Instruction Access (Code Execution)	User	0	PC<22:1>			0
		0xx xxxx xxxx xxxx xxxx xxx0				
TBLRD/TBLWT (Byte/Word Read/Write)	User	TBLPAG<7:0>		Data EA<15:0>		
		0xxx xxxx		xxxx xxxx xxxx xxxx		
	Configuration	TBLPAG<7:0>		Data EA<15:0>		
		1xxx xxxx		xxxx xxxx xxxx xxxx		
Program Space Visibility (Block Remap/Read)	User	0	DSRPAG<7:0> <sup>(2)</sup>		Data EA<14:0> <sup>(1)</sup>	
		0	xxxx xxxx		xxx xxxx xxxx xxxx	

**Note 1:** Data EA<15> is always '1' in this case, but is not used in calculating the program space address. Bit 15 of the address is DSRPAG<0>.

**2:** DSRPAG<9> is always '1' in this case. DSRPAG<8> decides whether the lower word or higher word of program memory is read. When DSRPAG<8> is '0', the lower word is read and when it is '1', the higher word is read.

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## 5.1 Summary of DMA Operations

The DMA Controller is capable of moving data between addresses according to a number of different parameters. Each of these parameters can be independently configured for any transaction. In addition, any or all of the DMA channels can independently perform a different transaction at the same time. Transactions are classified by these parameters:

- Source and destination (SFRs and data RAM)
- Data size (byte or word)
- Trigger source
- Transfer mode (One-Shot, Repeated or Continuous)
- Addressing modes (Fixed Address or Address Blocks with or without Address Increment/Decrement)

In addition, the DMA Controller provides channel priority arbitration for all channels.

### 5.1.1 SOURCE AND DESTINATION

Using the DMA Controller, data may be moved between any two addresses in the Data Space. The SFR space (0000h to 07FFh), or the data RAM space (0800h to FFFFh) can serve as either the source or the destination. Data can be moved between these areas in either direction or between addresses in either area. The four different combinations are shown in [Figure 5-2](#).

If it is necessary to protect areas of data RAM, the DMA Controller allows the user to set upper and lower address boundaries for operations in the Data Space above the SFR space. The boundaries are set by the DMAH and DMAL High/Low Address Limit registers. If a DMA channel attempts an operation outside of the address boundaries, the transaction is terminated and an interrupt is generated.

### 5.1.2 DATA SIZE

The DMA Controller can handle both 8-bit and 16-bit transactions. Size is user-selectable using the SIZE bit (DMACHn<1>). By default, each channel is configured for word-size transactions. When byte-size transactions are chosen, the LSb of the source and/or destination address determines if the data represents the upper or lower byte of the data RAM location.

### 5.1.3 TRIGGER SOURCE

The DMA Controller can use 63 of the device's interrupt sources to initiate a transaction. The DMA trigger sources occur in reverse order than their natural interrupt priority and are shown in [Table 5-1](#).

Since the source and destination addresses for any transaction can be programmed independently of the trigger source, the DMA Controller can use any trigger to perform an operation on any peripheral. This also allows DMA channels to be cascaded to perform more complex transfer operations.

### 5.1.4 TRANSFER MODE

The DMA Controller supports four types of data transfers, based on the volume of data to be moved for each trigger:

- One-Shot: A single transaction occurs for each trigger.
- Continuous: A series of back-to-back transactions occur for each trigger; the number of transactions is determined by the DMACNTn transaction counter.
- Repeated One-Shot: A single transaction is performed repeatedly, once per trigger, until the DMA channel is disabled.
- Repeated Continuous: A series of transactions are performed repeatedly, one cycle per trigger, until the DMA channel is disabled.

All Transfer modes allow the option to have the source and destination addresses, and counter value, automatically reloaded after the completion of a transaction; Repeated mode transfers do this automatically.

### 5.1.5 ADDRESSING MODES

The DMA Controller also supports transfers between single addresses or address ranges. The four basic options are:

- Fixed-to-Fixed: Between two constant addresses
- Fixed-to-Block: From a constant source address to a range of destination addresses
- Block-to-Fixed: From a range of source addresses to a single, constant destination address
- Block-to-Block: From a range of source addresses to a range of destination addresses

The option to select auto-increment or auto-decrement of source and/or destination addresses is available for Block Addressing modes.

In addition to the four basic modes, the DMA Controller also supports Peripheral Indirect Addressing (PIA) mode, where the source or destination address is generated jointly by the DMA Controller and a PIA capable peripheral. When enabled, the DMA channel provides a base source and/or destination address, while the peripheral provides a fixed range offset address.

For PIC24FJ128GA204 family devices, the 12-bit A/D Converter module is the only PIA capable peripheral. Details for its use in PIA mode are provided in [Section 24.0 “12-Bit A/D Converter with Threshold Detect”](#).

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## REGISTER 8-26: IPC5: INTERRUPT PRIORITY CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	INT1IP<2:0>		
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-3     **Unimplemented:** Read as '0'

bit 2-0     **INT1IP<2:0>:** External Interrupt 1 Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•  
•  
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled



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## REGISTER 8-43: IPC26: INTERRUPT PRIORITY CONTROL REGISTER 26

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	FSTIP<2:0>		
bit 15					bit 8		

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **FSTIP<2:0>:** FRC Self-Tune Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 7-0 **Unimplemented:** Read as '0'

## REGISTER 8-44: IPC29: INTERRUPT PRIORITY CONTROL REGISTER 29

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	JTAGIP<2:0>			—	—	—	—
bit 7				bit 0			

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-4 **JTAGIP<2:0>:** JTAG Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as '0'

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## REGISTER 13-1: TxCON: TIMER2 AND TIMER4 CONTROL REGISTER<sup>(1)</sup> (CONTINUED)

bit 3	<b>T32:</b> 32-Bit Timer Mode Select bit <sup>(3)</sup> 1 = Timerx and Timery form a single 32-bit timer 0 = Timerx and Timery act as two 16-bit timers In 32-bit mode, T3CON control bits do not affect 32-bit timer operation.
bit 2	<b>Unimplemented:</b> Read as '0'
bit 1	<b>TCS:</b> Timerx Clock Source Select bit <sup>(2)</sup> 1 = Timer source is selected by TECS<1:0> 0 = Internal clock (Fosc/2)
bit 0	<b>Unimplemented:</b> Read as '0'

- Note 1:** Changing the value of TxCON while the timer is running (TON = 1) causes the timer prescale counter to reset and is not recommended.
- 2:** If TCS = 1 and TECS<1:0> = x1, the selected external timer input (TMRCK or TxCK) must be configured to an available RPN/RPIn pin. For more information, see [Section 11.4 “Peripheral Pin Select \(PPS\)”](#).
- 3:** In T4CON, the T45 bit is implemented instead of T32 to select 32-bit mode. In 32-bit mode, the T3CON or T5CON control bits do not affect 32-bit timer operation.

## 14.0 INPUT CAPTURE WITH DEDICATED TIMERS

**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the “dsPIC33/PIC24 Family Reference Manual”, “Input Capture with Dedicated Timer” (DS39722). The information in this data sheet supersedes the information in the FRM.

Devices in the PIC24FJ128GA204 family contain six independent input capture modules. Each of the modules offers a wide range of configuration and operating options for capturing external pulse events and generating interrupts.

Key features of the input capture module include:

- Hardware-configurable for 32-bit operation in all modes by cascading two adjacent modules
- Synchronous and Trigger modes of output compare operation with up to 30 user-selectable sync/trigger sources available
- A 4-level FIFO buffer for capturing and holding timer values for several events
- Configurable interrupt generation
- Up to 6 clock sources available for each module, driving a separate, internal 16-bit counter

The module is controlled through two registers: ICxCON1 (Register 14-1) and ICxCON2 (Register 14-2). A general block diagram of the module is shown in Figure 14-1.

## 14.1 General Operating Modes

### 14.1.1 SYNCHRONOUS AND TRIGGER MODES

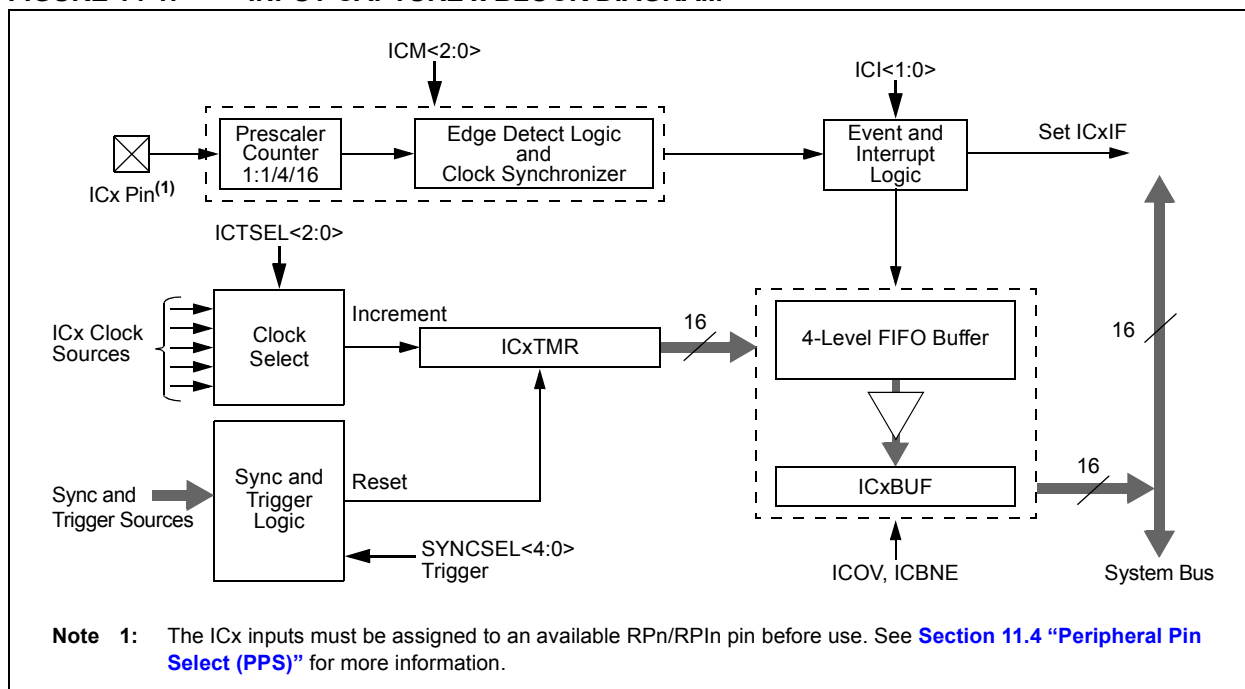
When the input capture module operates in a Free-Running mode, the internal 16-bit counter, ICxTMR, counts up continuously, wrapping around from FFFFh to 0000h on each overflow. Its period is synchronized to the selected external clock source. When a capture event occurs, the current 16-bit value of the internal counter is written to the FIFO buffer.

In Synchronous mode, the module begins capturing events on the ICx pin as soon as its selected clock source is enabled. Whenever an event occurs on the selected sync source, the internal counter is reset. In Trigger mode, the module waits for a sync event from another internal module to occur before allowing the internal counter to run.

Standard, free-running operation is selected by setting the SYNCSEL<4:0> bits (ICxCON2<4:0>) to ‘00000’ and clearing the ICTRIG bit (ICxCON2<7>). Synchronous and Trigger modes are selected any time the SYNCSELx bits are set to any value except ‘00000’. The ICTRIG bit selects either Synchronous or Trigger mode; setting the bit selects Trigger mode operation. In both modes, the SYNCSELx bits determine the sync/trigger source.

When the SYNCSELx bits are set to ‘00000’ and ICTRIG is set, the module operates in Software Trigger mode. In this case, capture operations are started by manually setting the TRIGSTAT bit (ICxCON2<6>).

**FIGURE 14-1: INPUT CAPTURE x BLOCK DIAGRAM**



## 18.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the “dsPIC33/PIC24 Family Reference Manual”, “Universal Asynchronous Receiver Transmitter (UART)” (DS70000582). The information in this data sheet supersedes the information in the FRM.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the PIC24F device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the  $\overline{\text{UxCTS}}$  and  $\overline{\text{UxRTS}}$  pins. The UART module includes the ISO 7816 compliant Smart Card support and the IrDA® encoder/decoder unit.

The PIC24FJ128GA204 family devices are equipped with four UART modules, referred to as UART1, UART2, UART3 and UART4.

The primary features of the UARTx modules are:

- Full-Duplex, 8 or 9-Bit Data Transmission through the  $\text{UxTX}$  and  $\text{UxRX}$  Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with the  $\overline{\text{UxCTS}}$  and  $\overline{\text{UxRTS}}$  Pins
- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Range from 61 bps to 4 Mbps at 16 MIPS in 4x mode

- Baud Rates Range from 15 bps to 1 Mbps at 16 MIPS in 16x mode
- 4-Deep, First-In-First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-Bit mode with Address Detect (9<sup>th</sup> bit = 1)
- Separate Transmit and Receive Interrupts
- Loopback mode for Diagnostic Support
- Polarity Control for Transmit and Receive Lines
- Support for Sync and Break Characters
- Supports Automatic Baud Rate Detection
- IrDA® Encoder and Decoder Logic
- Includes DMA Support
- 16x Baud Clock Output for IrDA Support
- Smart Card ISO 7816 Support (UART1 and UART2 only):
  - T = 0 protocol with automatic error handling
  - T = 1 protocol
  - Dedicated Guard Time Counter (GTC)
  - Dedicated Waiting Time Counter (WTC)

A simplified block diagram of the UARTx module is shown in [Figure 18-1](#). The UARTx module consists of these key important hardware elements:

- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

**Note:** Throughout this section, references to register and bit names that may be associated with a specific UART module are referred to generically by the use of ‘x’ in place of the specific module number. Thus, “UxSTA” might refer to the Status register for either UART1, UART2, UART3 or UART4.

# PIC24FJ128GA204 FAMILY

## REGISTER 20-1: PMCON1: EPMP CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
PMPEN	—	PSIDL	ADRMUX1	ADRMUX0	—	MODE1	MODE0
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
CSF1	CSF0	ALP	ALMODE	—	BUSKEEP	IRQM1	IRQM0
bit 7				bit 0			

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

- bit 15      **PMPEN:** EPMP Enable bit  
             1 = EPMP is enabled  
             0 = EPMP is disabled
- bit 14      **Unimplemented:** Read as '0'
- bit 13      **PSIDL:** EPMP Stop in Idle Mode bit  
             1 = Discontinues module operation when device enters Idle mode  
             0 = Continues module operation in Idle mode
- bit 12-11      **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits  
             11 = Lower address bits are multiplexed with data bits using 3 address phases  
             10 = Lower address bits are multiplexed with data bits using 2 address phases  
             01 = Lower address bits are multiplexed with data bits using 1 address phase  
             00 = Address and data appear on separate pins
- bit 10      **Unimplemented:** Read as '0'
- bit 9-8      **MODE<1:0>:** Parallel Port Mode Select bits  
             11 = Master mode  
             10 = Enhanced PSP: Pins used are PMRD, PMWR, PMCS, PMD<7:0> and PMA<1:0>  
             01 = Buffered PSP: Pins used are PMRD, PMWR, PMCS and PMD<7:0>  
             00 = Legacy Parallel Slave Port: Pins used are PMRD, PMWR, PMCS and PMD<7:0>
- bit 7-6      **CSF<1:0>:** Chip Select Function bits  
             11 = Reserved  
             10 = PMA<14> is used for Chip Select 1  
             01 = Reserved  
             00 = PMCS1 is used for Chip Select 1
- bit 5      **ALP:** Address Latch Polarity bit  
             1 = Active-high (PMALL, PMALH and PMALU)  
             0 = Active-low (PMALL, PMALH and PMALU)
- bit 4      **ALMODE:** Address Latch Strobe Mode bit  
             1 = Enables "smart" address strobes (each address phase is only present if the current access would cause a different address in the latch than the previous address)  
             0 = Disables "smart" address strobes
- bit 3      **Unimplemented:** Read as '0'
- bit 2      **BUSKEEP:** Bus Keeper bit  
             1 = Data bus keeps its last value when not actively being driven  
             0 = Data bus is in a high-impedance state when not actively being driven
- bit 1-0      **IRQM<1:0>:** Interrupt Request Mode bits  
             11 = Interrupt is generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode), or on a read or write operation when PMA<1:0> = 11 (Addressable PSP mode only)  
             10 = Reserved  
             01 = Interrupt is generated at the end of a read/write cycle  
             00 = No interrupt is generated

# PIC24FJ128GA204 FAMILY

## REGISTER 20-6: PMCSxBS: EPMP CHIP SELECT x BASE ADDRESS REGISTER<sup>(2)</sup>

R/W <sup>(1)</sup>	R/W <sup>(1)</sup>	R/W <sup>(1)</sup>	R/W <sup>(1)</sup>	R/W <sup>(1)</sup>	R/W <sup>(1)</sup>	R/W <sup>(1)</sup>	R/W <sup>(1)</sup>
BASE<23:16>							
bit 15				bit 8			

R/W <sup>(1)</sup>	U-0	U-0	U-0	R/W <sup>(1)</sup>	U-0	U-0	U-0
BASE15	—	—	—	BASE11	—	—	—
bit 7				bit 0			

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **BASE<23:15>**: Chip Select x Base Address bits<sup>(1)</sup>

bit 6-4 **Unimplemented**: Read as '0'

bit 3 **BASE11**: Chip Select x Base Address bit<sup>(1)</sup>

bit 2-0 **Unimplemented**: Read as '0'

**Note 1:** The value at POR is 0080h for PMCS1BS and 0880h for PMCS2BS.

**2:** If the whole PMCS2BS register is written together as 0x0000, then the last EDS address for Chip Select 1 will be FFFFFFFh. In this case, Chip Select 2 should not be used. PMCS1BS has no such feature.

## 27.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Charge Time Measurement Unit, refer to the *“dsPIC33/PIC24 Family Reference Manual”*, **“Charge Time Measurement Unit (CTMU) with Threshold Detect”** (DS39743).

The Charge Time Measurement Unit (CTMU) is a flexible analog module that provides charge measurement, accurate differential time measurement between pulse sources and asynchronous pulse generation. Its key features include:

- Thirteen external edge input trigger sources
- Polarity control for each edge source
- Control of edge sequence
- Control of response to edge levels or edge transitions
- Time measurement resolution of one nanosecond
- Accurate current source suitable for capacitive measurement

Together with other on-chip analog modules, the CTMU can be used to precisely measure time, measure capacitance, measure relative changes in capacitance or generate output pulses that are independent of the system clock. The CTMU module is ideal for interfacing with capacitive-based touch sensors.

The CTMU is controlled through three registers: CTMUCON1, CTMUCON2 and CTMUICON. CTMUCON1 enables the module and controls the mode of operation of the CTMU, as well as controlling edge sequencing. CTMUCON2 controls edge source selection and edge source polarity selection. The CTMUICON register selects the current range of current source and trims the current.

## 27.1 Measuring Capacitance

The CTMU module measures capacitance by generating an output pulse, with a width equal to the time between edge events, on two separate input channels. The pulse edge events to both input channels can be selected from four sources: two internal peripheral modules (OC1 and Timer1) and up to 13 external pins (CTED1 through CTED13). This pulse is used with the module's precision current source to calculate capacitance according to the relationship:

### EQUATION 27-1:

$$I = C \cdot \frac{dV}{dT}$$

For capacitance measurements, the A/D Converter samples an external Capacitor (CAPP) on one of its input channels after the CTMU output's pulse. A Precision Resistor (RPR) provides current source calibration on a second A/D channel. After the pulse ends, the converter determines the voltage on the capacitor. The actual calculation of capacitance is performed in software by the application.

Figure 27-1 illustrates the external connections used for capacitance measurements and how the CTMU and A/D modules are related in this application. This example also shows the edge events coming from Timer1, but other configurations using external edge sources are possible. A detailed discussion on measuring capacitance and time with the CTMU module is provided in the *“dsPIC33/PIC24 Family Reference Manual”*, **“Charge Time Measurement Unit (CTMU) with Threshold Detect”** (DS39743).

# PIC24FJ128GA204 FAMILY

## REGISTER 27-2: CTMUCON2: CTMU CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0	—	—
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **EDG1MOD:** Edge 1 Edge-Sensitive Select bit

1 = Input is edge-sensitive

0 = Input is level-sensitive

bit 14 **EDG1POL:** Edge 1 Polarity Select bit

1 = Edge 1 is programmed for a positive edge response

0 = Edge 1 is programmed for a negative edge response

bit 13-10 **EDG1SEL<3:0>:** Edge 1 Source Select bits

1111 = Edge 1 source is Comparator 3 output

1110 = Edge 1 source is Comparator 2 output

1101 = Edge 1 source is Comparator 1 output

1100 = Edge 1 source is IC3

1011 = Edge 1 source is IC2

1010 = Edge 1 source is IC1

1001 = Edge 1 source is CTED8

1000 = Edge 1 source is CTED7<sup>(1)</sup>

0111 = Edge 1 source is CTED6

0110 = Edge 1 source is CTED5

0101 = Edge 1 source is CTED4

0100 = Edge 1 source is CTED3

0011 = Edge 1 source is CTED1

0010 = Edge 1 source is CTED2

0001 = Edge 1 source is OC1

0000 = Edge 1 source is Timer1

bit 9 **EDG2STAT:** Edge 2 Status bit

Indicates the status of Edge 2 and can be written to control current source.

1 = Edge 2 has occurred

0 = Edge 2 has not occurred

bit 8 **EDG1STAT:** Edge 1 Status bit

Indicates the status of Edge 1 and can be written to control current source.

1 = Edge 1 has occurred

0 = Edge 1 has not occurred

bit 7 **EDG2MOD:** Edge 2 Edge-Sensitive Select bit

1 = Input is edge-sensitive

0 = Input is level-sensitive

bit 6 **EDG2POL:** Edge 2 Polarity Select bit

1 = Edge 2 is programmed for a positive edge response

0 = Edge 2 is programmed for a negative edge response

**Note 1:** Edge source, CTED7, is not available in 28-pin packages.



# PIC24FJ128GA204 FAMILY

## REGISTER 28-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
HLVDEN	—	LSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
VDIR	BGVST	IRVST	—	HLVDL3	HLVDL2	HLVDL1	HLVDL0
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15      **HLVDEN:** High/Low-Voltage Detect Power Enable bit  
1 = HLVD is enabled  
0 = HLVD is disabled
- bit 14      **Unimplemented:** Read as '0'
- bit 13      **LSIDL:** High/Low-Voltage Detect Stop in Idle Mode bit  
1 = Discontinues module operation when device enters Idle mode  
0 = Continues module operation in Idle mode
- bit 12-8    **Unimplemented:** Read as '0'
- bit 7      **VDIR:** Voltage Change Direction Select bit  
1 = Event occurs when voltage equals or exceeds trip point (HLVDL<3:0>)  
0 = Event occurs when voltage equals or falls below trip point (HLVDL<3:0>)
- bit 6      **BGVST:** Band Gap Voltage Stable Flag bit  
1 = Indicates that the band gap voltage is stable  
0 = Indicates that the band gap voltage is unstable
- bit 5      **IRVST:** Internal Reference Voltage Stable Flag bit  
1 = Internal reference voltage is stable; the High-Voltage Detect logic generates the interrupt flag at the specified voltage range  
0 = Internal reference voltage is unstable; the High-Voltage Detect logic will not generate the interrupt flag at the specified voltage range and the HLVD interrupt should not be enabled
- bit 4      **Unimplemented:** Read as '0'
- bit 3-0    **HLVDL<3:0>:** High/Low-Voltage Detection Limit bits  
1111 = External analog input is used (input comes from the HLVDIN pin)  
1110 = Trip Point 1<sup>(1)</sup>  
1101 = Trip Point 2<sup>(1)</sup>  
1100 = Trip Point 3<sup>(1)</sup>  
•  
•  
•  
0100 = Trip Point 11<sup>(1)</sup>  
00xx = Unused

**Note 1:** For the actual trip point, see [Section 32.0 “Electrical Characteristics”](#).

# PIC24FJ128GA204 FAMILY

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## 29.4.3 CONFIGURATION REGISTER PROTECTION

The Configuration registers are protected against inadvertent or unwanted changes or reads in two ways. The primary protection method is the same as that of the RP registers – shadow registers contain a complimentary value which is constantly compared with the actual value.

To safeguard against unpredictable events, Configuration bit changes resulting from individual cell-level disruptions (such as ESD events) will cause a parity error and trigger a device Reset.

The data for the Configuration registers is derived from the Flash Configuration Words in program memory. When the GCP bit is set, the source data for device configuration is also protected as a consequence. Even if General Segment protection is not enabled, the device configuration can be protected by using the appropriate Code Segment protection setting.

## 29.5 JTAG Interface

PIC24FJ128GA204 family devices implement a JTAG interface, which supports boundary scan device testing and programming.

## 29.6 In-Circuit Serial Programming

PIC24FJ128GA204 family microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock (PGECx) and data (PGEDx), and three other lines for power (VDD), ground (VSS) and MCLR. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

## 29.7 In-Circuit Debugger

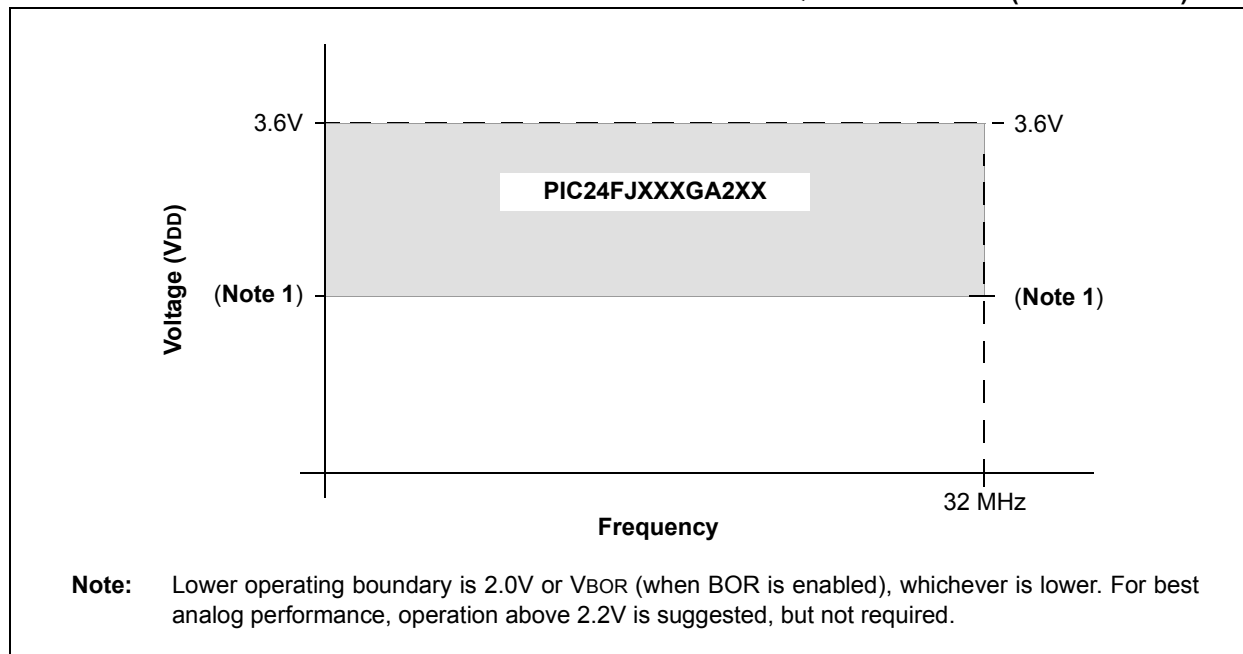
When MPLAB® ICD 3 is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB IDE. Debugging functionality is controlled through the PGECx (Emulation/Debug Clock) and PGEDx (Emulation/Debug Data) pins.

To use the in-circuit debugger function of the device, the design must implement ICSP connections to MCLR, VDD, VSS and the PGECx/PGEDx pin pair, designated by the ICSx Configuration bits. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins.

# PIC24FJ128GA204 FAMILY

## 32.1 DC Characteristics

**FIGURE 32-1: PIC24FJ128GA204 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)**



**TABLE 32-1: THERMAL OPERATING CONDITIONS**

Rating	Symbol	Min	Typ	Max	Unit
PIC24FJ128GA204:					
Operating Junction Temperature Range	T <sub>J</sub>	-40	—	+125	°C
Operating Ambient Temperature Range	T <sub>A</sub>	-40	—	+85	°C
Power Dissipation:					
Internal Chip Power Dissipation: P <sub>INT</sub> = V <sub>DD</sub> × (I <sub>DD</sub> – Σ I <sub>OH</sub> )	P <sub>D</sub>	P <sub>INT</sub> + P <sub>I/O</sub>			W
I/O Pin Power Dissipation: P <sub>I/O</sub> = Σ ({V <sub>DD</sub> – V <sub>OH</sub> } × I <sub>OH</sub> ) + Σ (V <sub>OL</sub> × I <sub>OL</sub> )					
Maximum Allowed Power Dissipation	P <sub>DMAX</sub>	(T <sub>J</sub> – T <sub>A</sub> )/θ <sub>JA</sub>			W

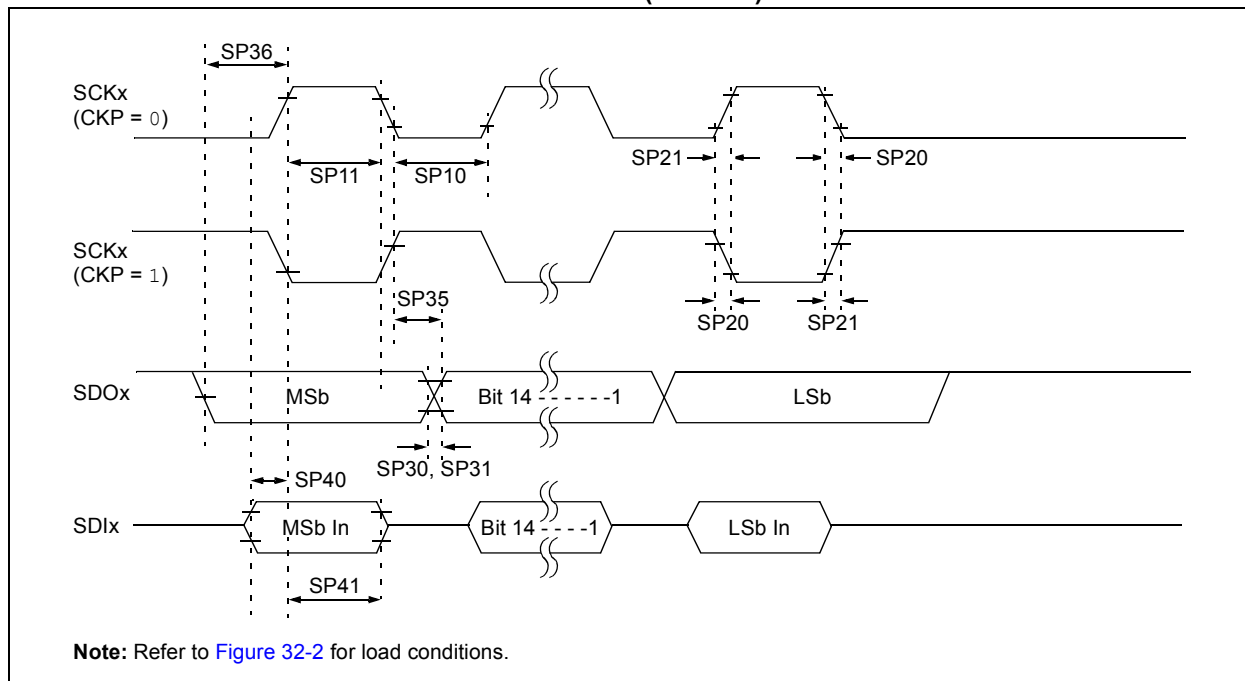
**TABLE 32-2: THERMAL PACKAGING CHARACTERISTICS**

Characteristic	Symbol	Typ	Max	Unit	Notes
Package Thermal Resistance, 7.50 mm 28-Pin SOIC	θ <sub>JA</sub>	49	—	°C/W	(Note 1)
Package Thermal Resistance, 6x6x0.9 mm 28-Pin QFN-S	θ <sub>JA</sub>	33.7	—	°C/W	(Note 1)
Package Thermal Resistance, 8x8 mm 44-Pin QFN	θ <sub>JA</sub>	28	—	°C/W	(Note 1)
Package Thermal Resistance, 10x10x1 mm 44-Pin TQFP	θ <sub>JA</sub>	39.3	—	°C/W	(Note 1)
Package Thermal Resistance, 5.30 mm 28-Pin SSOP	θ <sub>JA</sub>	—	—	°C/W	(Note 1)
Package Thermal Resistance, 300 mil 28-Pin SPDIP	θ <sub>JA</sub>	—	—	°C/W	(Note 1)

**Note 1:** Junction to ambient thermal resistance; Theta-JA (θ<sub>JA</sub>) numbers are achieved by package simulations.

# PIC24FJ128GA204 FAMILY

**FIGURE 32-14: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS**



**TABLE 32-36: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min	Typ <sup>(2)</sup>	Max	Units	Conditions
SP10	TscL	SCKx Output Low Time <sup>(3)</sup>	Tcy/2	—	—	ns	
SP11	TscH	SCKx Output High Time <sup>(3)</sup>	Tcy/2	—	—	ns	
SP20	TscF	SCKx Output Fall Time <sup>(4)</sup>	—	—	—	ns	See Parameter DO32
SP21	TscR	SCKx Output Rise Time <sup>(4)</sup>	—	—	—	ns	See Parameter DO31
SP30	TdoF	SDOx Data Output Fall Time <sup>(4)</sup>	—	—	—	ns	See Parameter DO32
SP31	TdoR	SDOx Data Output Rise Time <sup>(4)</sup>	—	—	—	ns	See Parameter DO31
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge	—	6	20	ns	
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	23	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

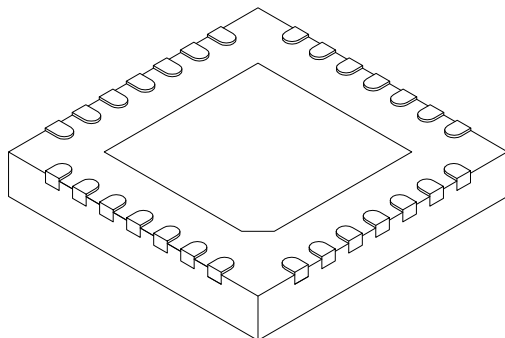
**3:** The minimum clock period for SCKx is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

# PIC24FJ128GA204 FAMILY

## 28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	3.65	3.70	4.70
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	3.65	3.70	4.70
Terminal Width	b	0.23	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed Pad	K	0.20	-	-

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-124C Sheet 2 of 2