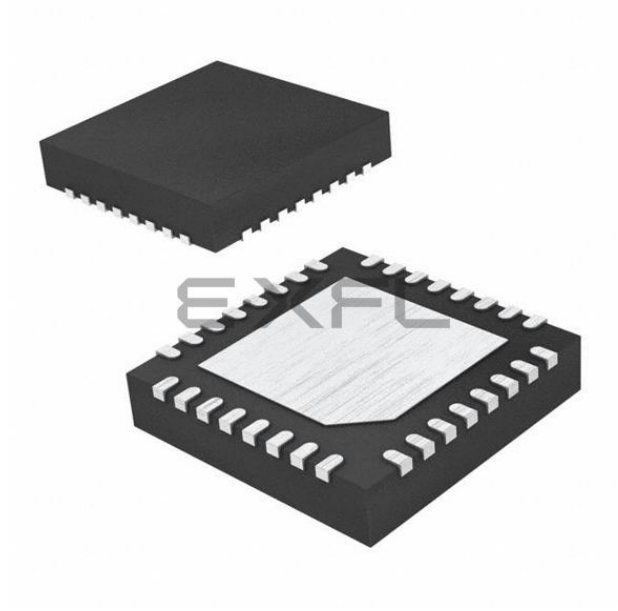

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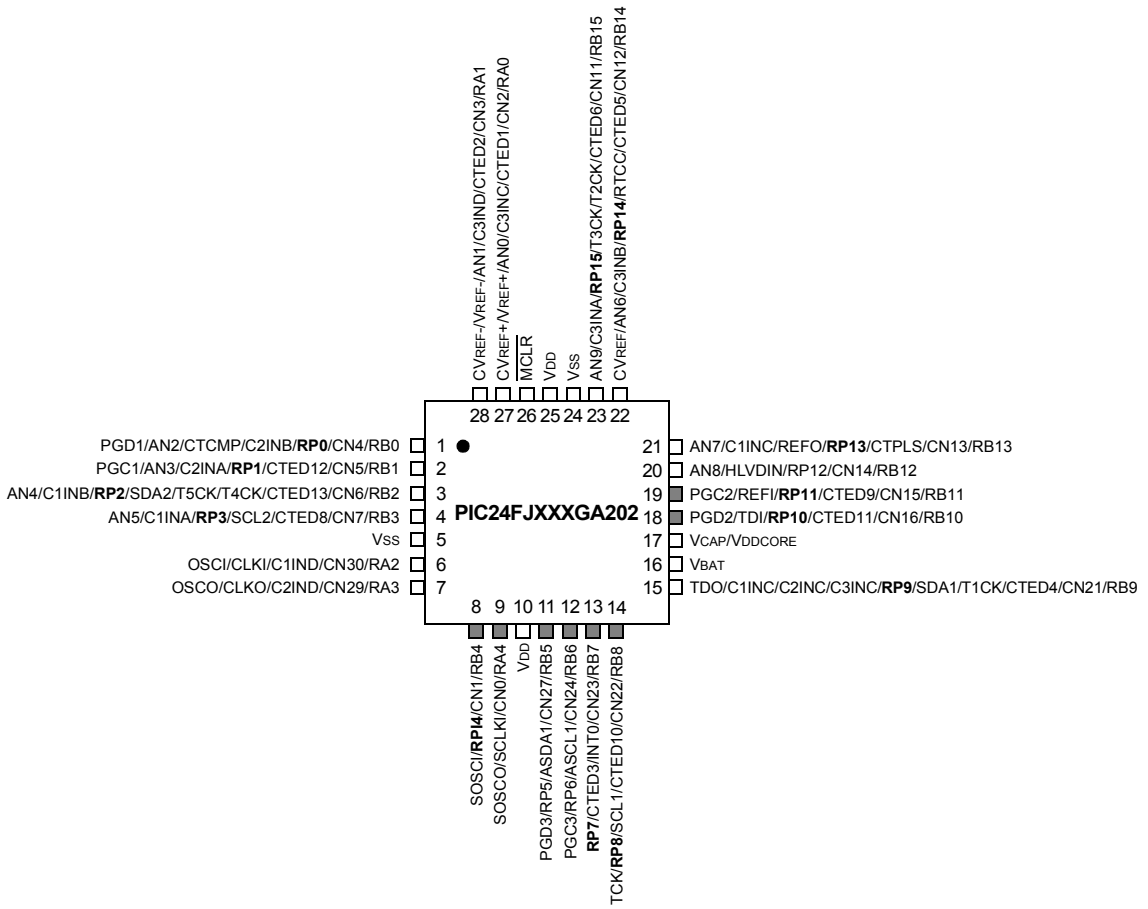
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	AES, Brown-out Detect/Reset, DMA, I²S, HLVD, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj64ga202-e-mm

Pin Diagrams (Continued)

28-Pin QFN-S(1,2)

5V tolerant



Legend: **RPn** represents remappable peripheral pins.

Note 1: The back pad on QFN devices should be connected to VSS.

TABLE 1-1: DEVICE FEATURES FOR THE PIC24FJ128GA204 FAMILY: 44-PIN DEVICES

Features	PIC24FJ64GA204	PIC24FJ128GA204
Operating Frequency	DC – 32 MHz	
Program Memory (bytes)	64K	128K
Program Memory (instructions)	22,016	44,032
Data Memory (bytes)	8K	
Interrupt Sources (soft vectors/ NMI traps)	71 (67/4)	
I/O Ports	Ports A, B, C	
Total I/O Pins	35	
Remappable Pins	25 (24 I/Os, 1 Input only)	
Timers: Total Number (16-bit)	5(1)	
32-Bit (from paired 16-bit timers)	2	
Input Capture w/Timer Channels	6(1)	
Output Compare/PWM Channels	6(1)	
Input Change Notification Interrupt	35	
Serial Communications: UART	4(1)	
SPI (3-wire/4-wire)	3(1)	
I^2C™	2	
Digital Signal Modulator (DSM)	Yes	
Parallel Communications (EPMP/PSP)	Yes	
JTAG Boundary Scan	Yes	
12-Bit SAR Analog-to-Digital Converter (A/D) (input channels)	13	
Analog Comparators	3	
CTMU Interface	13 Channels	
Resets (and Delays)	Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, MCLR, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)	
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations	
Packages	44-Pin TQFP and QFN	
Cryptographic Engine	Supports AES with 128, 192 and 256-Bit Key, DES and TDES, True Random and Pseudorandom Number Generator, On-Chip OTP Storage	
RTCC	Yes	

Note 1: Peripherals are accessible through remappable pins.

4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-2).

Program memory addresses are always word-aligned on the lower word and addresses are incremented or decremented by two during code execution. This arrangement also provides compatibility with data memory space addressing and makes it possible to access data in the program memory space.

4.1.2 HARD MEMORY VECTORS

All PIC24F devices reserve the addresses between 000000h and 000200h for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user at 000000h with the actual address for the start of code at 000002h.

PIC24F devices also have two Interrupt Vector Tables, (IVTs), located from 000004h to 0000FFh and 000100h to 0001FFh. These vector tables allow each of the many device interrupt sources to be handled by separate ISRs. A more detailed discussion of the Interrupt Vector Tables is provided in **Section 8.1 "Interrupt Vector Table"**.

4.1.3 FLASH CONFIGURATION WORDS

In PIC24FJ128GA204 family devices, the top four words of on-chip program memory are reserved for configuration information. On device Reset, the configuration information is copied into the appropriate Configuration register. The addresses of the Flash Configuration Word for devices in the PIC24FJ128GA204 family are shown in Table 4-1. Their location in the memory map is shown with the other memory vectors in Figure 4-1.

The Configuration Words in program memory are a compact format. The actual Configuration bits are mapped in several different registers in the configuration memory space. Their order in the Flash Configuration Words does not reflect a corresponding arrangement in the configuration space. Additional details on the device Configuration Words are provided in **Section 29.0 "Special Features"**.

TABLE 4-1: FLASH CONFIGURATION WORDS FOR PIC24FJ128GA204 FAMILY DEVICES

Device	Program Memory (Words)	Configuration Word Addresses
PIC24FJ64GA2XX	22,016	00ABF8h:00ABFEh
PIC24FJ128GA2XX	44,032	0157F8h:0157FEh

FIGURE 4-2: PROGRAM MEMORY ORGANIZATION

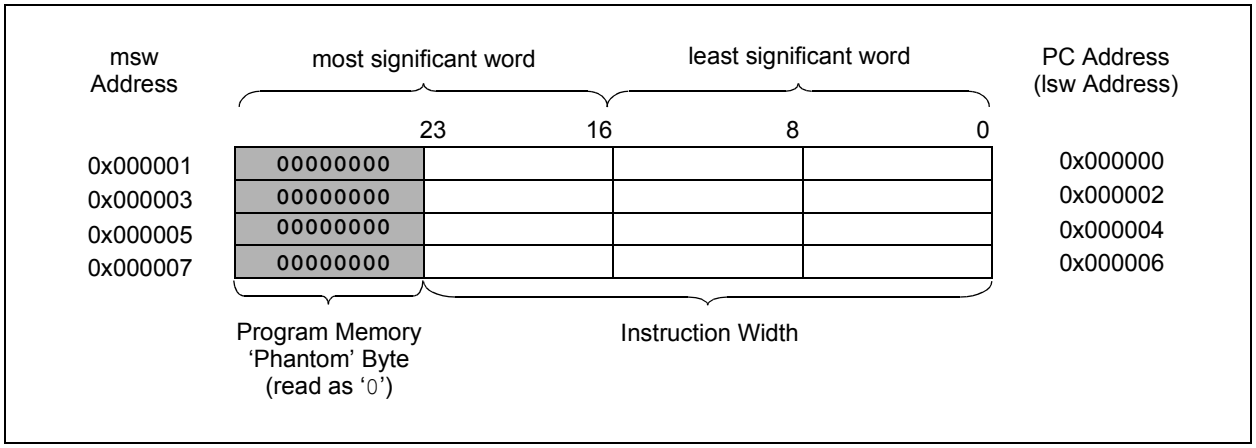


TABLE 4-22: ENHANCED PARALLEL MASTER/SLAVE PORT REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMCON1	0128	PMPEN	—	PSIDL	ADRMUX1	ADRMUX0	—	MODE1	MODE0	CSF1	CSF0	ALP	ALMODE	—	BUSKEEP	IRQM1	IRQM0	0000
PMCON2	012A	PMPBUSY	—	ERROR	TIMEOUT	—	—	—	—	RADDR23	RADDR22	RADDR21	RADDR20	RADDR19	RADDR18	RADDR17	RADDR16	0000
PMCON3	012C	PTWREN	PTRDEN	PTBE1EN	PTBE0EN	—	AWAITM1	AWAITM0	AWAITE	—	—	—	—	—	—	—	—	0000
PMCON4	012E	—	PTEN14	—	—	—	—	PTEN<9:0>										0000
PMCS1CF	0130	CSDIS	CSP	CSPTEN	BEP	—	WRSP	RDSP	SM	ACKP	PTSZ1	PTSZ0	—	—	—	—	—	0000
PMCS1BS	0132	BASE<23:15>									—	—	—	BASE11	—	—	—	0200
PMCS1MD	0134	ACKM1	ACKM0	AMWAIT2	AMWAIT1	AMWAIT0	—	—	—	DWAITB1	DWAITB0	DWAITM3	DWAITM2	DWAITM1	DWAITM0	DWAITE1	DWAITE0	0000
PMCS2CF	0136	CSDIS	CSP	CSPTEN	BEP	—	WRSP	RDSP	SM	ACKP	PTSZ1	PTSZ0	—	—	—	—	—	0000
PMCS2BS	0138	BASE<23:15>									—	—	—	BASE11	—	—	—	0600
PMCS2MD	013A	ACKM1	ACKM0	AMWAIT2	AMWAIT1	AMWAIT0	—	—	—	DWAITB1	DWAITB0	DWAITM3	DWAITM2	DWAITM1	DWAITM0	DWAITE1	DWAITE0	0000
PMDOUT1	013C	EPMP Data Out Register 1<15:8>								EPMP Data Out Register 1<7:0>								xxxx
PMDOUT2	013E	EPMP Data Out Register 2<15:8>								EPMP Data Out Register 2<7:0>								xxxx
PMDIN1	0140	EPMP Data In Register 1<15:8>								EPMP Data In Register 1<7:0>								xxxx
PMDIN2	0142	EPMP Data In Register 2<15:8>								EPMP Data In Register 2<7:0>								xxxx
PMSTAT	0144	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	008F

Legend: — = unimplemented, read as '0'; x = unknown value on Reset. Reset values are shown in hexadecimal.

REGISTER 5-3: DMAINTn: DMA CHANNEL n INTERRUPT REGISTER

R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DBUFWF(1)	—	CHSEL5	CHSEL4	CHSEL3	CHSEL2	CHSEL1	CHSEL0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
HIGHIF(1,2)	LOWIF(1,2)	DONEIF(1)	HALFIF(1)	OVRUNIF(1)	—	—	HALFEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **DBUFWF:** DMA Buffered Data Write Flag bit(1)
- 1 = The content of the DMA buffer has not been written to the location specified in DMADSTn or DMASRCn in Null Write mode
- 0 = The content of the DMA buffer has been written to the location specified in DMADSTn or DMASRCn in Null Write mode

bit 14 **Unimplemented:** Read as '0'

bit 13-8 **CHSEL<5:0>:** DMA Channel Trigger Selection bits

See Table 5-1 for a complete list.

bit 7 **HIGHIF:** DMA High Address Limit Interrupt Flag bit(1,2)
- 1 = The DMA channel has attempted to access an address higher than DMAH or the upper limit of the data RAM space
- 0 = The DMA channel has not invoked the high address limit interrupt

bit 6 **LOWIF:** DMA Low Address Limit Interrupt Flag bit(1,2)
- 1 = The DMA channel has attempted to access the DMA SFR address lower than DMAL, but above the SFR range (07FFh)
- 0 = The DMA channel has not invoked the low address limit interrupt

bit 5 **DONEIF:** DMA Complete Operation Interrupt Flag bit(1)

If CHEN = 1:
- 1 = The previous DMA session has ended with completion
- 0 = The current DMA session has not yet completed

If CHEN = 0:
- 1 = The previous DMA session has ended with completion
- 0 = The previous DMA session has ended without completion

bit 4 **HALFIF:** DMA 50% Watermark Level Interrupt Flag bit(1)
- 1 = DMACNTn has reached the halfway point to 0000h
- 0 = DMACNTn has not reached the halfway point

bit 3 **OVRUNIF:** DMA Channel Overrun Flag bit(1)
- 1 = The DMA channel is triggered while it is still completing the operation based on the previous trigger
- 0 = The overrun condition has not occurred

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **HALFEN:** DMA Halfway Completion Watermark bit
- 1 = Interrupts are invoked when DMACNTn has reached its halfway point and at completion
- 0 = An interrupt is invoked only at the completion of the transfer

Note 1: Setting these flags in software does not generate an interrupt.

2: Testing for address limit violations (DMASRCn or DMADSTn is either greater than DMAH or less than DMAL) is NOT done before the actual access.

REGISTER 8-25: IPC4: INTERRUPT PRIORITY CONTROL REGISTER 4

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	CNIP2	CNIP1	CNIP0	—	CMIP2	CMIP1	CMIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	MI2C1IP2	MI2C1IP1	MI2C1IP0	—	SI2C1IP2	SI2C1IP1	SI2C1IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **CNIP<2:0>:** Input Change Notification Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **CMIP<2:0>:** Comparator Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **MI2C1IP<2:0>:** Master I2C1 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **SI2C1IP<2:0>:** Slave I2C1 Event Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-30: IPC9: INTERRUPT PRIORITY CONTROL REGISTER 9

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	IC5IP2	IC5IP1	IC5IP0	—	IC4IP2	IC4IP1	IC4IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	IC3IP2	IC3IP1	IC3IP0	—	DMA3IP2	DMA3IP1	DMA3IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **IC5IP<2:0>:** Input Capture Channel 5 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **IC4IP<2:0>:** Input Capture Channel 4 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **IC3IP<2:0>:** Input Capture Channel 3 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **DMA3IP<2:0>:** DMA Channel 3 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 9-3: OSCTUN: FRC OSCILLATOR TUNE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R-0	R/W-0	R-0	R/W-0
STEN	—	STSIDL	STSRC(1)	STLOCK	STLPOL	STOR	STORPOL
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **STEN:** FRC Self-Tune Enable bit
1 = FRC self-tuning is enabled; TUNx bits are controlled by hardware
0 = FRC self-tuning is disabled; application may optionally control TUNx bits

bit 14 **Unimplemented:** Read as '0'

bit 13 **STSIDL:** FRC Self-Tune Stop in Idle bit
1 = Self-tuning stops during Idle mode
0 = Self-tuning continues during Idle mode

bit 12 **STSRC:** FRC Self-Tune Reference Clock Source bit(1)
1 = Reserved
0 = FRC is tuned to approximately match the 32.768 kHz SOSC tolerance

bit 11 **STLOCK:** FRC Self-Tune Lock Status bit
1 = FRC accuracy is currently within ±0.2% of the STSRC reference accuracy
0 = FRC accuracy may not be within ±0.2% of the STSRC reference accuracy

bit 10 **STLPOL:** FRC Self-Tune Lock Interrupt Polarity bit
1 = A self-tune lock interrupt is generated when STLOCK = 0
0 = A self-tune lock interrupt is generated when STLOCK = 1

bit 9 **STOR:** FRC Self-Tune Out of Range Status bit
1 = STSRC reference clock error is beyond the range of TUN<5:0>; no tuning is performed
0 = STSRC reference clock is within the tunable range; tuning is performed

bit 8 **STORPOL:** FRC Self-Tune Out of Range Interrupt Polarity bit
1 = A self-tune out of range interrupt is generated when STOR is = 0
0 = A self-tune out of range interrupt is generated when STOR is = 1

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits
011111 = Maximum frequency deviation
011110 =
•
•
•
000001 =
000000 = Center frequency, oscillator is running at factory calibrated frequency
111111 =
•
•
•
100001 =
100000 = Minimum frequency deviation

Note 1: Use of either clock recovery source has specific application requirements. For more information, see **Section 9.5 "FRC Self-Tuning"**.

9.6 Reference Clock Output

In addition to the CLKO output (FOSC/2) available in certain Oscillator modes, the device clock in the PIC24FJ128GA204 family devices can also be configured to provide a reference clock output signal to a port pin. This feature is available in all oscillator configurations and allows the user to select a greater range of clock submultiples to drive external devices in the application.

This reference clock output is controlled by the REFOCONL, REFOCONH and REFOTRIML registers (Register 9-4, Register 9-5 and Register 9-6). Setting the ROEN bit (REFOCONL<15>) enables the module. Setting the ROOUT bit (REFOCONL<12>) makes the clock signal available on the REFO pin.

The RODIVx bits (REFOCONH<14:0>) enable the selection of 32768 different clock divider options.

9.6.1 CLOCK SOURCE REQUEST

The ROSEL<3:0> bits determine different base clock sources for the module.

If the selected clock source has a global device enable (via device Configuration Fuse settings), the user must enable the clock source before selecting it as a base clock source.

The ROACTIVE bit (REFOCONL<8>) synchronizes the REFO module during the turn on and turn off of the module.

Note:	Once the ROEN bit is set, it should not be cleared until the ROACTIVE bit is read as '1'.

9.6.2 CLOCK SWITCHING

The base clock to the module can be switched. First, turn off the module by clearing the ROEN bit (REFOCONL<15> = 0) and wait for the ROACTIVE (REFOCONL<8>) bit to be cleared by the hardware.

This avoids a glitch in the REFO output.

The ROTRIMx and RODIVx bits can be changed on-the-fly. Follow the below mentioned steps before changing the ROTRIMx and RODIVx bits.

- REFO is not actively performing the divider switch (ROSWEN = 0).
- Update the ROTRIMx and RODIVx bits with the latest values.
- Set the ROSWEN bit.
- Wait for the ROSWEN bit to be cleared by hardware.

The ROTRIMx bits allow a fractional divisor to be added to the integer divisor, specified in the RODIVx bits.

EQUATION 9-1: FRACTIONAL DIVISOR FOR ROTRIMx BITS

For RODIV<14:0> = 0, No Divide:
RODIV<14:0> > 0, Period = 2 * (RODIVx + ROTRIMx)

9.6.3 OPERATION IN SLEEP MODE

The ROSLP and ROSELx bits (REFOCONL<11,3:0>) control the availability of the reference output during Sleep mode.

The ROSLP bit determines if the reference source is available on the REFO pin when the device is in Sleep mode.

To use the reference clock output in Sleep mode, the ROSLP bit must be set and the reference base clock should not be the system clock or peripheral clock (ROSELx bits should not be '0b0000' or '0b0001').

The device clock must also be configured for either:

- One of the Primary modes (EC, HS or XT); the POSCEN bit should be set
- The Secondary Oscillator bit (SOSCEN) should be set
- The LPRC Oscillator

If one of the above conditions is not met, then the oscillators on OSC1, OSC2 and SOSCI will be powered down when the device enters Sleep mode.

REGISTER 9-4: REFOCONL: REFERENCE OSCILLATOR CONTROL LOW REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
ROEN	—	ROSIDL	ROOUT	ROSLP	—	ROSWEN	ROACTIVE
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	ROSEL3	ROSEL2	ROSEL1	ROSEL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ROEN:** Reference Oscillator Output Enable bit
1 = Reference oscillator is enabled
0 = Reference oscillator is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **ROSIDL:** Reference Oscillator Output in Idle Mode bit
1 = Reference oscillator is disabled in Idle mode
0 = Reference oscillator continues to run in Idle mode

bit 12 **ROOUT:** Reference Clock Output Enable bit
1 = REFO clock output is driven on the REFO pin
0 = REFO clock output is disabled

bit 11 **ROSLP:** Reference Oscillator Output in Sleep Mode bit
1 = Reference oscillator output continues to run in Sleep mode
0 = Reference oscillator output is disabled in Sleep mode

bit 10 **Unimplemented:** Read as '0'

bit 9 **ROSWEN:** Reference Oscillator Clock Source Switch Enable bit
1 = Reference clock source switching is currently in progress
0 = Reference clock source switching has completed

bit 8 **ROACTIVE:** Reference Clock Request Status bit
1 = Reference clock request is active (user should not update the REFOCONL register)
0 = Reference clock request is not active (user can update the REFOCONL register)

bit 7-4 **Unimplemented:** Read as '0'
(Reserved for additional ROSELx bits.)

bit 3-0 **ROSEL<3:0>:** Reference Clock Source Select bits
Selects one of the various clock sources to be used as the reference clock:
1001-1111 = Reserved
1000 = REFI (Reference Clock Input)
0111 = Reserved
0110 = 8x PLL
0101 = Secondary Oscillator (SOSC)
0100 = Low-Power RC Oscillator (LPRC)
0011 = Fast RC Oscillator (FRC)
0010 = Primary Oscillator (XT, HS, EC)
0001 = Peripheral Clock (PBCLK) – internal instruction cycle clock, FCY
0000 = System Clock (FOSC)

15.0 OUTPUT COMPARE WITH DEDICATED TIMERS

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual",* **"Output Compare with Dedicated Timer"** (DS70005159). The information in this data sheet supersedes the information in the FRM.

Devices in the PIC24FJ128GA204 family all feature six independent output compare modules. Each of these modules offers a wide range of configuration and operating options for generating pulse trains on internal device events, and can produce Pulse-Width Modulated (PWM) waveforms for driving power applications.

Key features of the output compare module include:

- Hardware-configurable for 32-bit operation in all modes by cascading two adjacent modules
- Synchronous and Trigger modes of output compare operation, with up to 31 user-selectable trigger/sync sources available
- Two separate Period registers (a main register, OCxR, and a secondary register, OCxRS) for greater flexibility in generating pulses of varying widths
- Configurable for single pulse or continuous pulse generation on an output event, or continuous PWM waveform generation
- Up to 6 clock sources available for each module, driving a separate internal 16-bit counter

15.1 General Operating Modes

15.1.1 SYNCHRONOUS AND TRIGGER MODES

When the output compare module operates in a Free-Running mode, the internal 16-bit counter, OCxTMR, runs counts up continuously, wrapping around from 0xFFFF to 0x0000 on each overflow. Its period is synchronized to the selected external clock source. Compare or PWM events are generated each time a match between the internal counter and one of the Period registers occurs.

In Synchronous mode, the module begins performing its compare or PWM operation as soon as its selected clock source is enabled. Whenever an event occurs on the selected sync source, the module's internal counter is reset. In Trigger mode, the module waits for a sync event from another internal module to occur before allowing the counter to run.

Free-Running mode is selected by default or any time that the SYNCSEL<4:0> bits (OCxCON2<4:0>) are set to '00000'. Synchronous or Trigger modes are selected any time the SYNCSELx bits are set to any value except '00000'. The OCTRIG bit (OCxCON2<7>) selects either Synchronous or Trigger mode; setting the bit selects Trigger mode operation. In both modes, the SYNCSELx bits determine the sync/trigger source.

15.1.2 CASCADED (32-BIT) MODE

By default, each module operates independently with its own set of 16-bit Timer and Duty Cycle registers. To increase resolution, adjacent even and odd modules can be configured to function as a single 32-bit module. (For example, Modules 1 and 2 are paired, as are Modules 3 and 4, and so on.) The odd numbered module, Output Compare x (OCx), provides the Least Significant 16 bits of the 32-bit register pairs and the even numbered module, Output Compare y (OCy), provides the Most Significant 16 bits. Wrap arounds of the OCx registers cause an increment of their corresponding OCy registers.

Cascaded operation is configured in hardware by setting the OC32 bit (OCxCON2<8>) for both modules. For more information on cascading, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Output Compare with Dedicated Timer"** (DS70005159).

18.7.2 BUILT-IN IrDA ENCODER AND DECODER

The UARTx has full implementation of the IrDA encoder and decoder as part of the UARTx module. The built-in IrDA encoder and decoder functionality is enabled using the IREN bit (UxMODE<12>). When enabled (IREN = 1), the receive pin (UxRX) acts as the input from the infrared receiver. The transmit pin (UxTX) acts as the output to the infrared transmitter.

18.8 Smart Card ISO 7816 Support

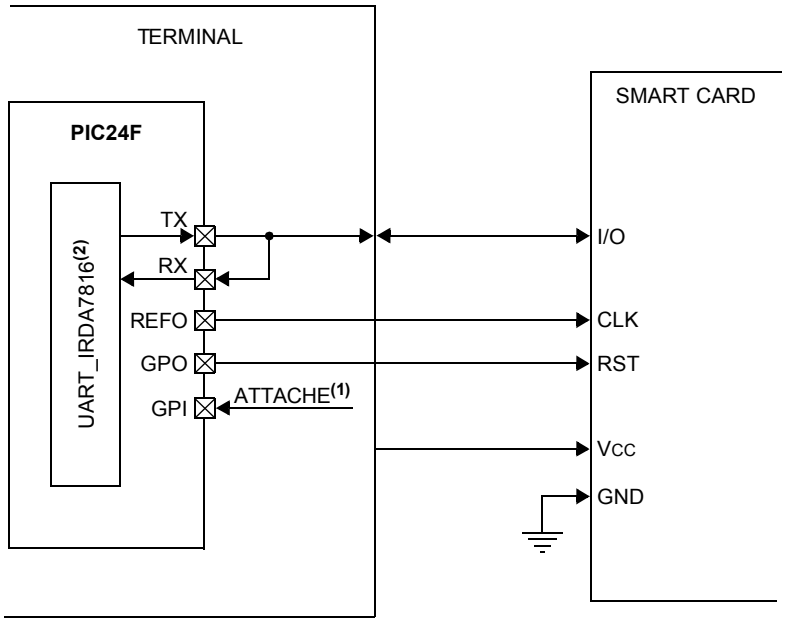
Figure 18-2 shows a Smart Card subsystem using a PIC24F microcontroller with a UARTx module for Smart Card data communication. Vcc to power the Smart Card can be supplied through a terminal or an external power supply. The terminal is also responsible for clocking and resetting the Smart Card. The TX and RX line of the PIC24F device has to be shorted externally and then connected to the I/O line of the Smart Card.

There are two protocols which are widely used for Smart Card communication between terminal and Smart Card:

- T = 0 (asynchronous, half-duplex, byte-oriented protocol)
- T = 1 (asynchronous, half-duplex, block-oriented protocol)

The selection of T = 0 or T = 1 protocol is done using the PTRCL bit in UxSCCON register.

FIGURE 18-2: SMART CARD SUBSYSTEM CONNECTION



Note 1: Driven high upon card insertion.

2: Only UART1 and UART2 support Smart Card ISO 7816.

REGISTER 18-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0	R-0, HSC	R-1, HSC
UTXISEL1	UTXINV(1)	UTXISEL0	URXEN	UTXBRK	UTXEN(2)	UTXBF	TRMT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-1, HSC	R-0, HSC	R-0, HSC	R/C-0, HS	R-0, HSC
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7							bit 0

Legend:	C = Clearable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
HS = Hardware Settable bit	HC = Hardware Clearable bit		

bit 15,13 **UTXISEL<1:0>:** UARTx Transmission Interrupt Mode Selection bits
- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR), and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)

bit 14 **UTXINV:** UARTx IrDA® Encoder Transmit Polarity Inversion bit(1)

IREN = 0:
- 1 = UxTX Idle state is '0'
- 0 = UxTX Idle state is '1'

IREN = 1:
- 1 = UxTX Idle state is '1'
- 0 = UxTX Idle state is '0'

bit 12 **URXEN:** UARTx Receive Enable bit
- 1 = Receive is enabled, UxRX pin is controlled by UARTx
- 0 = Receive is disabled, UxRX pin is controlled by the port

bit 11 **UTXBRK:** UARTx Transmit Break bit
- 1 = Sends Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
- 0 = Sync Break transmission is disabled or completed

bit 10 **UTXEN:** UARTx Transmit Enable bit(2)
- 1 = Transmit is enabled, UxTX pin is controlled by UARTx
- 0 = Transmit is disabled, any pending transmission is aborted and the buffer is reset; UxTX pin is controlled by the port

bit 9 **UTXBF:** UARTx Transmit Buffer Full Status bit (read-only)
- 1 = Transmit buffer is full
- 0 = Transmit buffer is not full, at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only)
- 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
- 0 = Transmit Shift Register is not empty, a transmission is in progress or queued

Note 1: The value of this bit only affects the transmit properties of the module when the IrDA® encoder is enabled (IREN = 1).

2: If UARTEN = 1, the peripheral inputs and outputs must be configured to an available RPn/RPIn pin. For more information, see **Section 11.4 "Peripheral Pin Select (PPS)"**.

REGISTER 20-2: PMCON2: EPMP CONTROL REGISTER 2

R-0, HSC	U-0	R/C-0, HS	R/C-0, HS	U-0	U-0	U-0	U-0
PMPBUSY	—	ERROR	TIMEOUT	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RADDR23(1)	RADDR22(1)	RADDR21(1)	RADDR20(1)	RADDR19(1)	RADDR18(1)	RADDR17(1)	RADDR16(1)
bit 7							bit 0

Legend:	HS = Hardware Settable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	C = Clearable bit

bit 15 **PMPBUSY:** EPMP Busy bit (Master mode only)
1 = Port is busy
0 = Port is not busy

bit 14 **Unimplemented:** Read as '0'

bit 13 **ERROR:** EPMP Error bit
1 = Transaction error (illegal transaction was requested)
0 = Transaction completed successfully

bit 12 **TIMEOUT:** EPMP Time-out bit
1 = Transaction timed out
0 = Transaction completed successfully

bit 11-8 **Unimplemented:** Read as '0'

bit 7-0 **RADDR<23:16>:** EPMP Reserved Address Space bits(1)

Note 1: If RADDR<23:16> = 00000000, then the last EDS address for Chip Select 2 will be FFFFFFh.

21.2 RTCC Module Registers

The RTCC module registers are organized into three categories:

- RTCC Control Registers
- RTCC Value Registers
- Alarm Value Registers

21.2.1 REGISTER MAPPING

To limit the register interface, the RTCC Timer and Alarm Time registers are accessed through corresponding Register Pointers. The RTCC Value register window (RTCVALH and RTCVALL) uses the RTCPTR<1:0> bits (RCFGCAL<9:8>) to select the desired Timer register pair (see Table 21-1).

By writing the RTCVALH byte, the RTCC Pointer value, the RTCPTR<1:0> bits decrement by one until they reach '00'. Once they reach '00', the MINUTES and SECONDS value will be accessible through RTCVALH and RTCVALL until the pointer value is manually changed.

TABLE 21-1: RTCVAL REGISTER MAPPING

RTCPTR<1:0>	RTCC Value Register Window	
	RTCVAL<15:8>	RTCVAL<7:0>
00	MINUTES	SECONDS
01	WEEKDAY	HOURS
10	MONTH	DAY
11	—	YEAR

The Alarm Value register window (ALRMVALH and ALRMVALL) uses the ALRMPTR<1:0> bits (ALCFGRPT<9:8>) to select the desired Alarm register pair (see Table 21-2).

By writing the ALRMVALH byte, the ALRMPTR<1:0> bits (the Alarm Pointer value) decrement by one until they reach '00'. Once they reach '00', the ALRMMIN and ALRMSEC value will be accessible through ALRMVALH and ALRMVALL until the pointer value is manually changed.

TABLE 21-2: ALRMVAL REGISTER MAPPING

ALRMPTR <1:0>	Alarm Value Register Window	
	ALRMVAL<15:8>	ALRMVAL<7:0>
00	ALRMMIN	ALRMSEC
01	ALRMWD	ALRMHR
10	ALRMMNTH	ALRMDAY
11	—	—

Considering that the 16-bit core does not distinguish between 8-bit and 16-bit read operations, the user must be aware that when reading either the ALRMVALH or ALRMVALL bytes, the ALRMPTR<1:0> value will be decremented. The same applies to the RTCVALH or RTCVALL bytes with the RTCPTR<1:0> being decremented.

Note: This only applies to read operations and not write operations.

21.2.2 WRITE LOCK

In order to perform a write to any of the RTCC Timer registers, the RTCWREN bit (RCFGCAL<13>) must be set (see Example 21-1).

Note: To avoid accidental writes to the timer, it is recommended that the RTCWREN bit (RCFGCAL<13>) is kept clear at any other time. For the RTCWREN bit to be set, there is only one instruction cycle time window allowed between the 55h/AA sequence and the setting of RTCWREN; therefore, it is recommended that code follow the procedure in Example 21-1.

21.2.3 SELECTING RTCC CLOCK SOURCE

The clock source for the RTCC module can be selected using the RTCLK<1:0> bits in the RTCPWC register. When the bits are set to '00', the Secondary Oscillator (SOSC) is used as the reference clock and when the bits are '01', LPRC is used as the reference clock. When RTCLK<1:0> = 10 and 11, the external power line (50 Hz and 60 Hz) is used as the clock source.

EXAMPLE 21-1: SETTING THE RTCWREN BIT

```
asm    volatile("push w7");
asm    volatile("push w8");
asm    volatile("disi #5");
asm    volatile("mov #0x55, w7");
asm    volatile("mov w7, _NVMKEY");
asm    volatile("mov #0xAA, w8");
asm    volatile("mov w8, _NVMKEY");
asm    volatile("bset _RCFGCAL, #13");   //set the RTCWREN bit
asm    volatile("pop w8");
asm    volatile("pop w7");
```

REGISTER 22-5: CFGPAGE: SECURE ARRAY CONFIGURATION BITS (OTP PAGE 0) REGISTER

r-x	R/PO-x	U-x	U-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x
—	TSTPGM(1)	—	—	KEY4TYPE1	KEY4TYPE0	KEY3TYPE1	KEY3TYPE0
bit 31							bit 24

R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x
KEY2TYPE1	KEY2TYPE0	KEY1TYPE1	KEY1TYPE0	SKEYEN	LKYSRC7	LKYSRC6	LKYSRC5
bit 23							bit 16

R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x
LKYSRC4	LKYSRC3	LKYSRC2	LKYSRC1	LKYSRC0	SRCLCK	WRLOCK8	WRLOCK7
bit 15							bit 8

R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x
WRLOCK6	WRLOCK5	WRLOCK74	WRLOCK3	WRLOCK2	WRLOCK1	WRLOCK0	SWKYDIS
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	PO = Program Once bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** Do not modify

bit 30 **TSTPGM:** Customer Program Test bit(1)
1 = CFGPAGE has been programmed
0 = CFGPAGE has not been programmed

bit 29-28 **Unimplemented:** Read as '0'

bit 27-26 **KEY4TYPE<1:0>:** Key Type for OTP Pages 7 and 8 bits
00 = Keys in these pages are for DES/2DES operations only
01 = Keys in these pages are for 3DES operations only
10 = Keys in these pages are for 128-bit AES operations only
11 = Keys in these pages are for 192-bit/256-bit AES operations only

bit 25-24 **KEY3TYPE<1:0>:** Key Type for OTP Pages 5 and 6 bits
00 = Keys in these pages are for DES/2DES operations only
01 = Keys in these pages are for 3DES operations only
10 = Keys in these pages are for 128-bit AES operations only
11 = Keys in these pages are for 192-bit/256-bit AES operations only

bit 23-22 **KEY2TYPE<1:0>:** Key Type for OTP Pages 3 and 4 bits
00 = Keys in these pages are for DES/2DES operations only
01 = Keys in these pages are for 3DES operations only
10 = Keys in these pages are for 128-bit AES operations only
11 = Keys in these pages are for 192-bit/256-bit AES operations only

bit 21-20 **KEY1TYPE<1:0>:** Key Type for OTP Pages 1 and 2 bits
00 = Keys in these pages are for DES/2DES operations only
01 = Keys in these pages are for 3DES operations only
10 = Keys in these pages are for 128-bit AES operations only
11 = Keys in these pages are for 192-bit/256-bit AES operations only

Note 1: This bit's state is mirrored by the PGMTST bit (CRYOTP<7>).

REGISTER 22-5: CFGPAGE: SECURE ARRAY CONFIGURATION BITS (OTP PAGE 0) REGISTER (CONTINUED)

bit 19 **SKEYEN:** Session Key Enable bit

1 = Stored Key #1 may be used only as a Key Encryption Key
0 = Stored Key #1 may be used for any operation

bit 18-11 **LKYSRC<7:0>:** Locked Key Source Configuration bits

If SRCLCK = 1:
1xxxxxxx = Key Source is as if KEYSRC<3:0> = 1111
01xxxxxx = Key Source is as if KEYSRC<3:0> = 0111
001xxxxx = Key Source is as if KEYSRC<3:0> = 0110
0001xxxx = Key Source is as if KEYSRC<3:0> = 0101
00001xxx = Key Source is as if KEYSRC<3:0> = 0100
000001xx = Key Source is as if KEYSRC<3:0> = 0011
0000001x = Key Source is as if KEYSRC<3:0> = 0010
00000001 = Key Source is as if KEYSRC<3:0> = 0001
00000000 = Key Source is as if KEYSRC<3:0> = 0000

If SRCLCK = 0:
These bits are ignored.

bit 10 **SRCLCK:** Key Source Lock bit

1 = The key source is determined by the KEYSRC<3:0> (CRYCONH<3:0>) bits (software key selection is disabled)
0 = The key source is determined by the KEYSRC<3:0> (CRYCONH<3:0>) bits (locked key selection is disabled)

bit 9-1 **WRLOCK<8:0>:** Write Lock Page Enable bits

For OTP Pages 0 (CFGPAGE) through 8:
1 = OTP Page is permanently locked and may not be programmed
0 = OTP Page is unlocked and may be programmed

bit 0 **SWKYDIS:** Software Key Disable bit

1 = Software key (CRYKEY register) is disabled; when KEYSRC<3:0> = 0000, the KEYFAIL status bit will be set and no encryption/decryption/session key operations can be started until KEYSRC<3:0> bits are changed to a value other than '0000'
0 = Software key (CRYKEY register) can be used as a key source when KEYSRC<3:0> = 0000

Note 1: This bit's state is mirrored by the PGMTST bit (CRYOTP<7>).

REGISTER 24-5: AD1CON5: A/D CONTROL REGISTER 5

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
ASEN	LPEN	CTMREQ	BGREQ	—	—	ASINT1	ASINT0
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	WM1	WM0	CM1	CM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ASEN:** Auto-Scan Enable bit
1 = Auto-scan is enabled
0 = Auto-scan is disabled

bit 14 **LPEN:** Low-Power Enable bit
1 = Low power is enabled after scan
0 = Full power is enabled after scan

bit 13 **CTMREQ:** CTMU Request bit
1 = CTMU is enabled when the A/D is enabled and active
0 = CTMU is not enabled by the A/D

bit 12 **BGREQ:** Band Gap Request bit
1 = Band gap is enabled when the A/D is enabled and active
0 = Band gap is not enabled by the A/D

bit 11-10 **Unimplemented:** Read as '0'

bit 9-8 **ASINT<1:0>:** Auto-Scan (Threshold Detect) Interrupt Mode bits
11 = Interrupt after Threshold Detect sequence has completed and valid compare has occurred
10 = Interrupt after valid compare has occurred
01 = Interrupt after Threshold Detect sequence has completed
00 = No interrupt

bit 7-4 **Unimplemented:** Read as '0'

bit 3-2 **WM<1:0>:** Write Mode bits
11 = Reserved
10 = Auto-compare only (conversion results are not saved, but interrupts are generated when a valid match occurs, as defined by the CMx and ASINTx bits)
01 = Convert and save (conversion results are saved to locations as determined by the register bits when a match occurs, as defined by the CMx bits)
00 = Legacy operation (conversion data is saved to a location determined by the buffer register bits)

bit 1-0 **CM<1:0>:** Compare Mode bits
11 = Outside Window mode (valid match occurs if the conversion result is outside of the window defined by the corresponding buffer pair)
10 = Inside Window mode (valid match occurs if the conversion result is inside the window defined by the corresponding buffer pair)
01 = Greater Than mode (valid match occurs if the result is greater than the value in the corresponding buffer register)
00 = Less Than mode (valid match occurs if the result is less than the value in the corresponding buffer register)

REGISTER 24-6: AD1CHS: A/D SAMPLE SELECT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB2	CH0NB1	CH0NB0	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NA2	CH0NA1	CH0NA0	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **CH0NB<2:0>:** Sample B Channel 0 Negative Input Select bits
1xx = Unimplemented
011 = Unimplemented
010 = AN1
001 = Unimplemented
000 = VREF-/AVSS

bit 12-8 **CH0SB<4:0>:** Sample B Channel 0 Positive Input Select bits
11111 = VBAT/2(1)
11110 = AVDD(1)
11101 = AVSS(1)
11100 = Band Gap Voltage (VBG) reference(1)
11011 = VBG/2(1)
01110 = CTMU
01101 = CTMU temperature sensor input (does not require AD1CTMENL<12> to be set)
01100 = AN12(2)
01011 = AN11(2)
01010 = AN10(2)
01001 = AN9
01000 = AN8
00111 = AN7
00110 = AN6
00101 = AN5
00100 = AN4
00011 = AN3
00010 = AN2
00001 = AN1
00000 = AN0

bit 7-5 **CH0NA<2:0>:** Sample A Channel 0 Negative Input Select bits
Same definitions as for CHONB<2:0>.

bit 4-0 **CH0SA<4:0>:** Sample A Channel 0 Positive Input Select bits
Same definitions as for CHOSB<4:0>.

Note 1: These input channels do not have corresponding memory-mapped result buffers.
2: These channels are unimplemented in 28-pin devices.

NOTES: