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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SmartCard, SPI, UART/USART |
| Peripherals | AES, Brown-out Detect/Reset, DMA, I²S, HLVD, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 10x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 28-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic24fj64ga202-e-ss |

**TABLE 1-1: DEVICE FEATURES FOR THE PIC24FJ128GA204 FAMILY: 44-PIN DEVICES**

| Features | PIC24FJ64GA204 | PIC24FJ128GA204 |
|---|---|---|
| Operating Frequency | DC – 32 MHz | |
| Program Memory (bytes) | 64K | 128K |
| Program Memory (instructions) | 22,016 | 44,032 |
| Data Memory (bytes) | 8K | |
| Interrupt Sources (soft vectors/ NMI traps) | 71 (67/4) | |
| I/O Ports | Ports A, B, C | |
| Total I/O Pins | 35 | |
| Remappable Pins | 25 (24 I/Os, 1 Input only) | |
| Timers: Total Number (16-bit) | 5(1) | |
| 32-Bit (from paired 16-bit timers) | 2 | |
| Input Capture w/Timer Channels | 6(1) | |
| Output Compare/PWM Channels | 6(1) | |
| Input Change Notification Interrupt | 35 | |
| Serial Communications: UART | 4(1) | |
| SPI (3-wire/4-wire) | 3(1) | |
| $I^2C$™ | 2 | |
| Digital Signal Modulator (DSM) | Yes | |
| Parallel Communications (EPMP/PSP) | Yes | |
| JTAG Boundary Scan | Yes | |
| 12-Bit SAR Analog-to-Digital Converter (A/D) (input channels) | 13 | |
| Analog Comparators | 3 | |
| CTMU Interface | 13 Channels | |
| Resets (and Delays) | Core POR, VDD POR, VBAT POR, BOR, RESET Instruction, MCLR, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock) | |
| Instruction Set | 76 Base Instructions, Multiple Addressing Mode Variations | |
| Packages | 44-Pin TQFP and QFN | |
| Cryptographic Engine | Supports AES with 128, 192 and 256-Bit Key, DES and TDES, True Random and Pseudorandom Number Generator, On-Chip OTP Storage | |
| RTCC | Yes | |

**Note 1:** Peripherals are accessible through remappable pins.

## 2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT MICROCONTROLLERS

### 2.1 Basic Connection Requirements

Getting started with the PIC24FJ128GA204 family of 16-bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development.

The following pins must always be connected:

- All VDD and VSS pins
  (see **Section 2.2 "Power Supply Pins"**)
- All AVDD and AVSS pins, regardless of whether or not the analog device features are used
  (see **Section 2.2 "Power Supply Pins"**)
- MCLR pin
  (see **Section 2.3 "Master Clear (MCLR) Pin"**)
- ENVREG/DISVREG and VCAP/VDDCORE pins
  (see **Section 2.4 "Voltage Regulator Pins (ENVREG/DISVREG and VCAP/VDDCORE)"**)

These pins must also be connected if they are being used in the end application:

- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes
  (see **Section 2.5 "ICSP Pins"**)
- OSCI and OSCO pins when an external oscillator source is used
  (see **Section 2.6 "External Oscillator Pins"**)

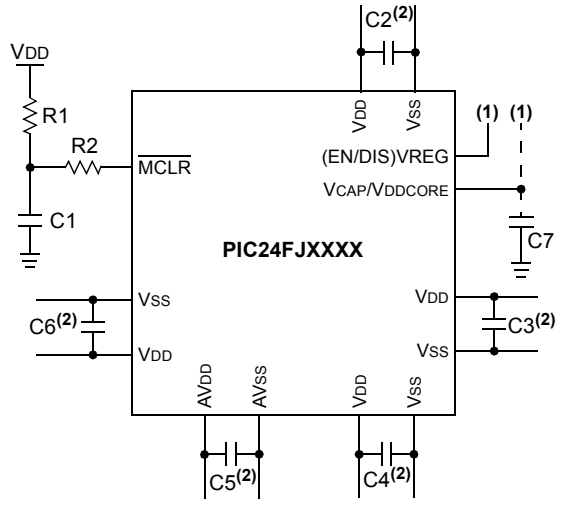
Additionally, the following pins may be required:

- VREF+/VREF- pins used when external voltage reference for analog modules is implemented

| **Note:** | The AVDD and AVSS pins must always be connected, regardless of whether any of the analog modules are being used. |
|---|---|

The minimum mandatory connections are shown in Figure 2-1.

**FIGURE 2-1: RECOMMENDED MINIMUM CONNECTIONS**




**Key (all values are recommendations):**

C1 through C6: 0.1 µF, 20V ceramic

C7: 10 µF, 6.3V or greater, tantalum or ceramic

R1: 10 kΩ

R2: 100Ω to 470Ω

**Note 1:** See **Section 2.4 "Voltage Regulator Pins (ENVREG/DISVREG and VCAP/VDDCORE)"** for explanation of the ENVREG/DISVREG pin connections.

**2:** The example shown is for a PIC24F device with five VDD/VSS and AVDD/AVSS pairs. Other devices may have more or less pairs; adjust the number of decoupling capacitors appropriately.

**FIGURE 3-2: PROGRAMMER'S MODEL**

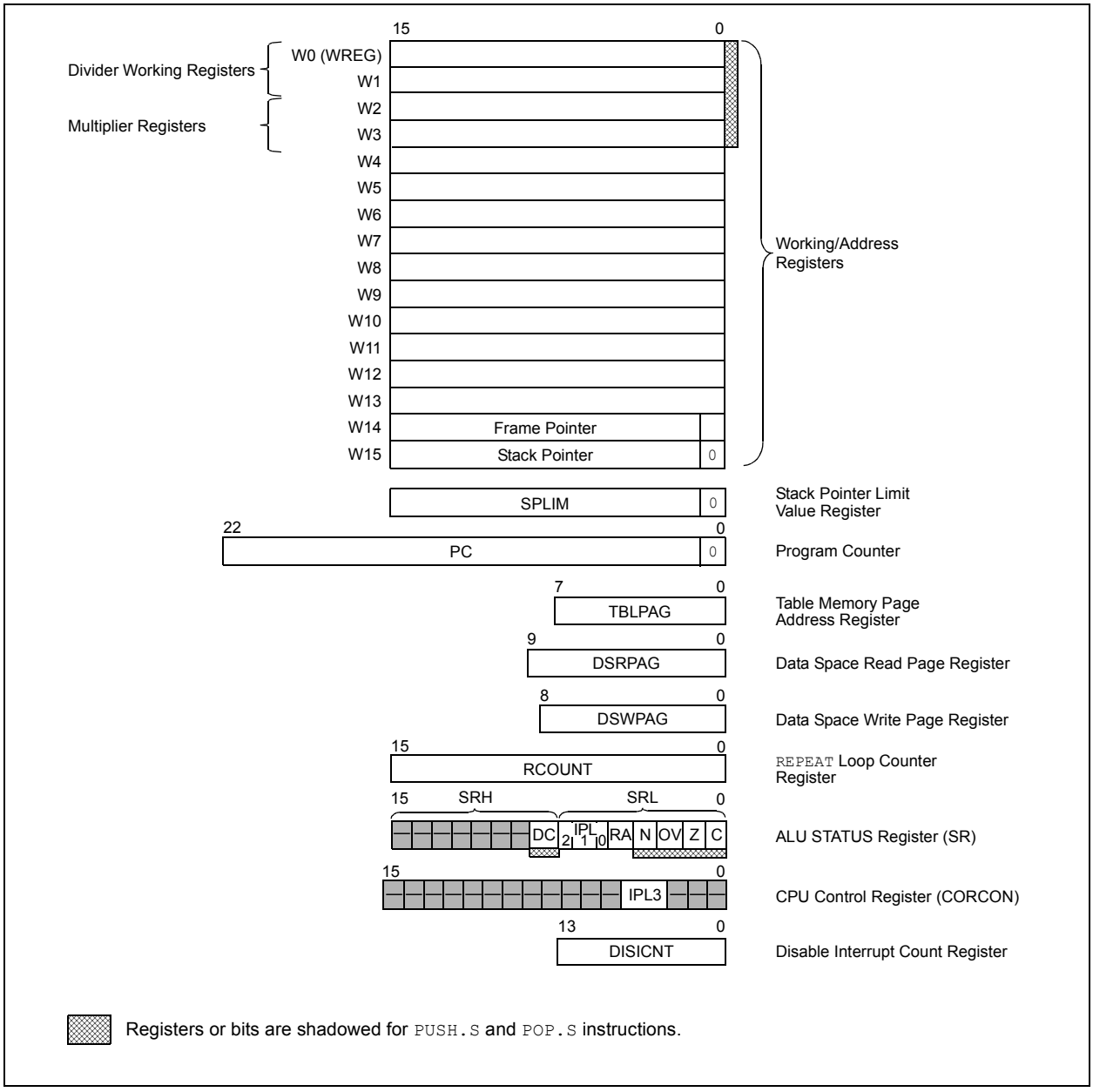


**TABLE 4-4: ICN REGISTER MAP**

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CNPD1 | 0056 | CN15PDE | CN14PDE | CN13PDE | CN12PDE | CN11PDE | CN10PDE(1) | CN9PDE(1) | CN8PDE(1) | CN7PDE | CN6PDE | CN5PDE | CN4PDE | CN3PDE | CN2PDE | CN1PDE | CN0PDE | 0000 |
| CNPD2 | 0058 | — | CN30PDE | CN29PDE | CN28PDE(1) | CN27PDE | CN26PDE(1) | CN25PDE(1) | CN24PDE | CN23PDE | CN22PDE | CN21PDE | CN20PDE(1) | CN19PDE(1) | CN18PDE(1) | CN17PDE(1) | CN16PDE | 0000 |
| CNPD3 | 005A | — | — | — | — | — | — | — | — | — | — | — | CN36PDE(1) | CN35PDE(1) | CN34PDE(1) | CN33PDE(1) | — | 0000 |
| CNEN1 | 0062 | CN15IE | CN14IE | CN13IE | CN12IE | CN11IE | CN10IE(1) | CN9IE(1) | CN8IE(1) | CN7IE | CN6IE | CN5IE | CN4IE | CN3IE | CN2IE | CN1IE | CN0IE | 0000 |
| CNEN2 | 0064 | — | CN30IE | CN29IE | CN28IE(1) | CN27IE | CN26IE(1) | CN25IE(1) | CN24IE | CN23IE | CN22IE | CN21IE | CN20IE(1) | CN19IE(1) | CN18IE(1) | CN17IE(1) | CN16IE | 0000 |
| CNEN3 | 0066 | — | — | — | — | — | — | — | — | — | — | — | CN36IE(1) | CN35IE(1) | CN34IE(1) | CN33IE(1) | — | 0000 |
| CNPU1 | 006E | CN15PUE | CN14PUE | CN13PUE | CN12PUE | CN11PUE | CN10PUE(1) | CN9PUE(1) | CN8PUE(1) | CN7PUE | CN6PUE | CN5PUE | CN4PUE | CN3PUE | CN2PUE | CN1PUE | CN0PUE | 0000 |
| CNPU2 | 0070 | — | CN30PUE | CN29PUE | CN28PUE(1) | CN27PUE | CN26PUE(1) | CN25PUE(1) | CN24PUE | CN23PUE | CN22PUE | CN21PUE | CN20PUE(1) | CN19PUE(1) | CN18PUE(1) | CN17PUE(1) | CN16PUE | 0000 |
| CNPU3 | 0072 | — | — | — | — | — | — | — | — | — | — | — | CN36PUE(1) | CN35PUE(1) | CN34PUE(1) | CN33PUE(1) | — | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** These bits are unimplemented in 28-pin devices, read as '0'.

**REGISTER 8-14: IEC1: INTERRUPT ENABLE CONTROL REGISTER 1 (CONTINUED)**

bit 2 **CMIE:** Comparator Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **MI2C1IE:** Master I2C1 Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **SI2C1IE:** Slave I2C1 Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

**Note 1:** If an external interrupt is enabled, the interrupt input must also be configured to an available RPn or RPIn pin. For more information, see **Section 11.4 "Peripheral Pin Select (PPS)"**.

**REGISTER 8-15: IEC2: INTERRUPT ENABLE CONTROL REGISTER 2 (CONTINUED)**

bit 1 **SPI2TXIE:** SPI2 Transmit Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **SPI2IE:** SPI2 General Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

**REGISTER 8-16: IEC3: INTERRUPT ENABLE CONTROL REGISTER 3**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | RTCIE | DMA5IE | SPI3RXIE | SPI2RXIE | SPI1RXIE | — | KEYSTRIE |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| CRYDNIE | INT4IE(1) | INT3IE(1) | — | — | MI2C2IE | SI2C2IE | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14 **RTCIE:** Real-Time Clock/Calendar Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 13 **DMA5IE:** DMA Channel 5 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 12 **SPI3RXIE:** SPI3 Receive Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 11 **SPI2RXIE:** SPI2 Receive Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 10 **SPI1RXIE:** SPI1 Receive Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 9 **Unimplemented:** Read as '0'

bit 8 **KEYSTRIE:** Cryptographic Key Store Program Done Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 7 **CRYDNIE:** Cryptographic Operation Done Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 6 **INT4IE:** External Interrupt 4 Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 5 **INT3IE:** External Interrupt 3 Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **MI2C2IE:** Master I2C2 Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

**Note 1:** If an external interrupt is enabled, the interrupt input must also be configured to an available RPn or RPIn pin. For more information, see **Section 11.4 "Peripheral Pin Select (PPS)"**.

#### 11.4.3.3 Mapping Limitations

The control schema of the Peripheral Pin Select is extremely flexible. Other than systematic blocks that prevent signal contention caused by two physical pins being configured as the same functional input or two functional outputs configured as the same pin, there are no hardware enforced lockouts. The flexibility extends to the point of allowing a single input to drive multiple peripherals or a single functional output to drive multiple output pins.

#### 11.4.3.4 Mapping Exceptions for PIC24FJ128GA204 Family Devices

Although the PPS registers theoretically allow for up to 24 remappable I/O pins, not all of these are implemented in all devices. For PIC24FJ128GA204 family devices, the maximum number of remappable pins available is 24, which includes one input only pin. The differences in available remappable pins are summarized in Table 11-5.

When developing applications that use remappable pins, users should also keep these things in mind:

- For the RPINRx registers, bit combinations corresponding to an unimplemented pin for a particular device are treated as invalid; the corresponding module will not have an input mapped to it.
- For RPORx registers, the bit fields corresponding to an unimplemented pin will also be unimplemented; writing to these fields will have no effect.

### 11.4.4 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC24F devices include three features to prevent alterations to the peripheral map:

- Control register lock sequence
- Continuous state monitoring
- Configuration bit remapping lock

#### 11.4.4.1 Control Register Lock

Under normal operation, writes to the RPINRx and RPORx registers are not allowed. Attempted writes will appear to execute normally, but the contents of the registers will remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK bit (OSCCON<6>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear IOLOCK, a specific command sequence must be executed:

1. Write 46h to OSCCON<7:0>.
2. Write 57h to OSCCON<7:0>.
3. Clear (or set) IOLOCK as a single operation.

Unlike the similar sequence with the oscillator's LOCK bit, IOLOCK remains in one state until changed. This allows all of the Peripheral Pin Selects to be configured with a single unlock sequence, followed by an update to all control registers, then locked with a second lock sequence.

#### 11.4.4.2 Continuous State Monitoring

In addition to being protected from direct writes, the contents of the RPINRx and RPORx registers are constantly monitored in hardware by shadow registers. If an unexpected change in any of the registers occurs (such as cell disturbances caused by ESD or other external events), a Configuration Mismatch Reset will be triggered.

#### 11.4.4.3 Configuration Bit Pin Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPINRx and RPORx registers. The IOL1WAY (CW4<15>) Configuration bit blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure will not execute and the Peripheral Pin Select Control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session. Programming IOL1WAY allows users unlimited access (with the proper use of the unlock sequence) to the Peripheral Pin Select registers.

**TABLE 11-5: REMAPPABLE PIN EXCEPTIONS FOR PIC24FJ128GA204 FAMILY DEVICES**

| Device | RPn Pins (I/O) | | RPIn Pins | |
|---|---|---|---|---|
| | Total | Unimplemented | Total | Unimplemented |
| PIC24FJXXXGA202 | 14 | RP4, RP12 | 1 | — |
| PIC24FJXXXGA204 | 24 | RP4, RP12 | 1 | — |

### 11.4.6 PERIPHERAL PIN SELECT REGISTERS

The PIC24FJ128GA204 family of devices implements a total of 32 registers for remappable peripheral configuration:

- Input Remappable Peripheral Registers (19)
- Output Remappable Peripheral Registers (13)

**Note:** Input and output register values can only be changed if IOLOCK (OSCCON<6>) = 0. See **Section 11.4.4.1 "Control Register Lock"** for a specific command sequence.

**REGISTER 11-4: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0**

| U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | INT1R5 | INT1R4 | INT1R3 | INT1R2 | INT1R1 | INT1R0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | OCTRIG1R5 | OCTRIG1R4 | OCTRIG1R3 | OCTRIG1R2 | OCTRIG1R1 | OCTRIG1R0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **INT1R<5:0>:** Assign External Interrupt 1 (INT1) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **OCTRIG1R<5:0>:** Assign Output Compare Trigger 1 to Corresponding RPn or RPIn Pin bits

**REGISTER 11-5: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1**

| U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | INT3R5 | INT3R4 | INT3R3 | INT3R2 | INT3R1 | INT3R0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | INT2R5 | INT2R4 | INT2R3 | INT2R2 | INT2R1 | INT2R0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **INT3R<5:0>:** Assign External Interrupt 3 (INT3) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **INT2R<5:0>:** Assign External Interrupt 2 (INT2) to Corresponding RPn or RPIn Pin bits

**REGISTER 11-18: RPINR27: PERIPHERAL PIN SELECT INPUT REGISTER 27**

| U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | U4CTSR5 | U4CTSR4 | U4CTSR3 | U4CTSR2 | U4CTSR1 | U4CTSR0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | U4RXR5 | U4RXR4 | U4RXR3 | U4RXR2 | U4RXR1 | U4RXR0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **U4CTSR<5:0>:** Assign UART4 Clear-to-Send Input ($\overline{\text{U4CTS}}$) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **U4RXR<5:0>:** Assign UART4 Receive Input (U4RX) to Corresponding RPn or RPIn Pin bits

**REGISTER 11-19: RPINR28: PERIPHERAL PIN SELECT INPUT REGISTER 28**

| U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | SCK3R5 | SCK3R4 | SCK3R3 | SCK3R2 | SCK3R1 | SCK3R0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | SDI3R5 | SDI3R4 | SDI3R3 | SDI3R2 | SDI3R1 | SDI3R0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **SCK3R<5:0>:** Assign SPI3 Clock Input (SCK3IN) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **SDI3R<5:0>:** Assign SPI3 Data Input (SDI3) to Corresponding RPn or RPIn Pin bits

## 12.0 TIMER1

**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Timers"** (DS39704). The information in this data sheet supersedes the information in the FRM.

The Timer1 module is a 16-bit timer, which can serve as the time counter for the Real-Time Clock (RTC) or operate as a free-running, interval timer/counter. Timer1 can operate in three modes:

- 16-Bit Timer
- 16-Bit Synchronous Counter
- 16-Bit Asynchronous Counter

Timer1 also supports these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during CPU Idle and Sleep modes
- Interrupt on 16-Bit Period Register Match or Falling Edge of External Gate Signal

Figure 12-1 shows a block diagram of the 16-bit timer module.

To configure Timer1 for operation:

1. Set the TON bit (= 1).
2. Select the timer prescaler ratio using the TCKPS<1:0> bits.
3. Set the Clock and Gating modes using the TCS, TECS<1:0> and TGATE bits.
4. Set or clear the TSYNC bit to configure synchronous or asynchronous operation.
5. Load the timer period value into the PR1 register.
6. If interrupts are required, set the Timer1 Interrupt Enable bit, T1IE. Use the Timer1 Interrupt Priority bits, T1IP<2:0>, to set the interrupt priority.

**FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM**

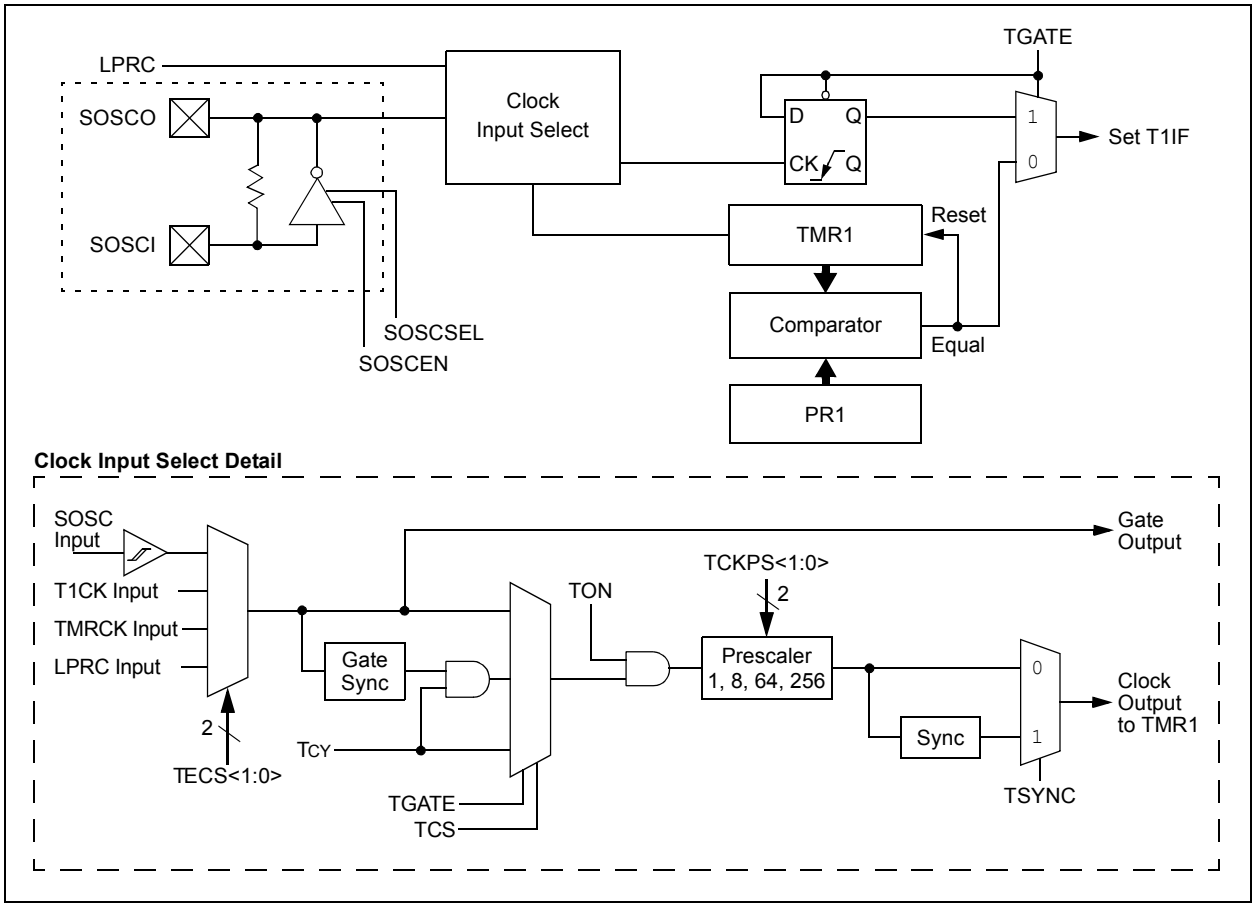
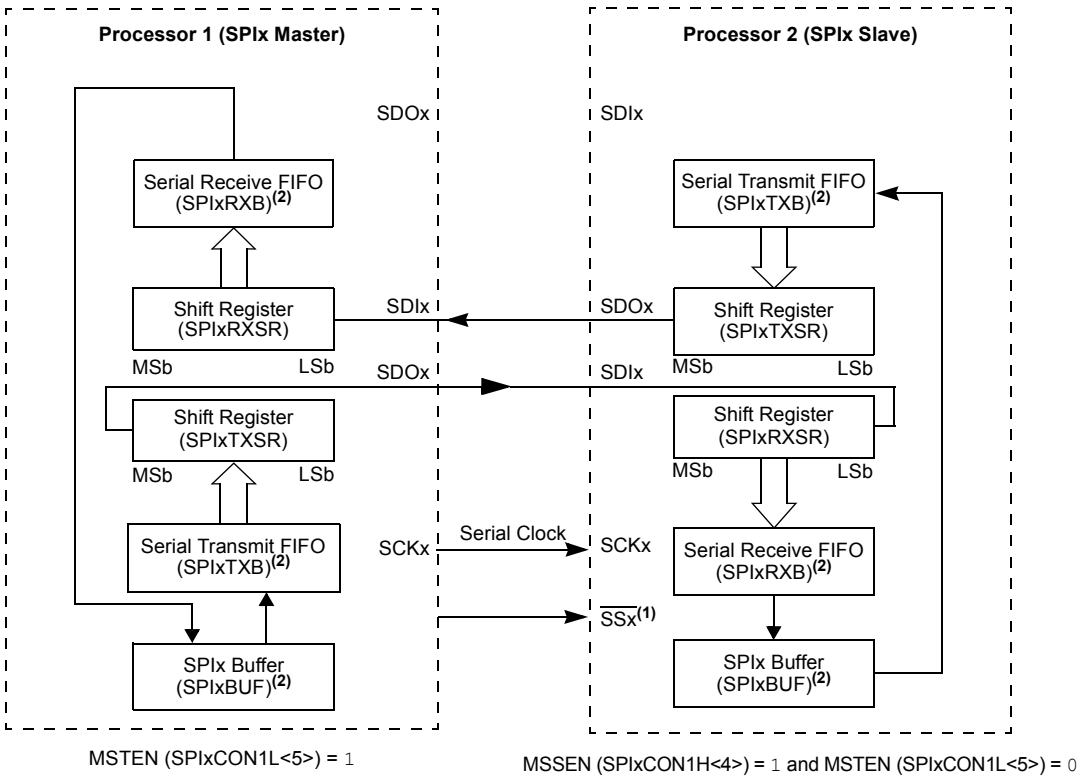


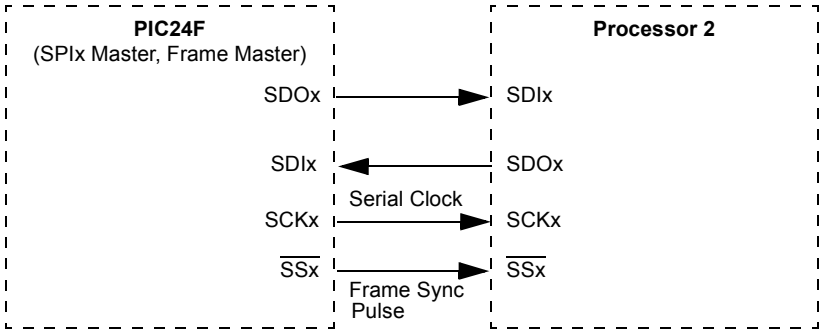
**FIGURE 16-4: SPIx MASTER/SLAVE CONNECTION (ENHANCED BUFFER MODES)**




**Note 1:** Using the $\overline{SSx}$ pin in Slave mode of operation is optional.

**2:** User must write transmit data to read the received data from SPIxBUF. The SPIxTXB and SPIxRXB registers are memory-mapped to SPIxBUF.

**FIGURE 16-5: SPIx MASTER, FRAME MASTER CONNECTION DIAGRAM**



## 18.9 Registers

The UART module consists of the following Special Function Registers (SFRs):

- UxMODE: UARTx Mode Register (Register 18-1)
- UxSTA: UARTx Status and Control Register (Register 18-2)
- UxRXREG: UARTx Receive Register
- UxTXREG: UARTx Transmit Register (Write-Only) (Register 18-3)
- UxADMD: UARTx Address Mask Detect Register (Register 18-4)
- UxBRG: UARTx Baud Rate Register
- UxSCCON: UARTx Smart Card Control Register (Register 18-5)
- UxSCINT: UARTx Smart Card Interrupt Register (Register 18-6)
- UxGTC: UARTx Guard Time Counter Register
- UxWTCL and UxWTCH: UARTx Waiting Time Counter Registers

**REGISTER 18-1: UxMODE: UARTx MODE REGISTER**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| UARTEN(1) | — | USIDL | IREN(2) | RTSMD | — | UEN1 | UEN0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0, HC | R/W-0 | R/W-0, HC | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| WAKE | LPBACK | ABAUD | URXINV | BRGH | PDSEL1 | PDSEL0 | STSEL |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HC = Hardware Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **UARTEN:** UARTx Enable bit(1)
1 = UARTx is enabled; all UARTx pins are controlled by UARTx as defined by UEN<1:0>
0 = UARTx is disabled; all UARTx pins are controlled by port latches; UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as '0'

bit 13 **USIDL:** UARTx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **IREN:** IrDA® Encoder and Decoder Enable bit(2)
1 = IrDA encoder and decoder are enabled
0 = IrDA encoder and decoder are disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Enable bits
11 = UxTX, UxRX and BCLKx pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by port latches
10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by port latches
00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/BCLKx pins are controlled by port latches

bit 7 **WAKE:** Wake-up on Start Bit Detect During Sleep Mode Enable bit
1 = UARTx continues to sample the UxRX pin; interrupt is generated on the falling edge, bit is cleared in hardware on the following rising edge
0 = No wake-up is enabled

**Note 1:** If UARTEN = 1, the peripheral inputs and outputs must be configured to an available RPn/RPIn pin. For more information, see **Section 11.4 "Peripheral Pin Select (PPS)"**.
**2:** This feature is only available for the 16x BRG mode (BRGH = 0).

**REGISTER 18-3: UxTXREG: UARTx TRANSMIT REGISTER (NORMALLY WRITE-ONLY)**

| W-x | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | W-x |
|---|---|---|---|---|---|---|---|
| LAST(1) | — | — | — | — | — | — | UxTXREG8 |
| bit 15 | | | | | | | bit 8 |

| W-x | W-x | W-x | W-x | W-x | W-x | W-x | W-x |
|---|---|---|---|---|---|---|---|
| UxTXREG7 | UxTXREG6 | UxTXREG5 | UxTXREG4 | UxTXREG3 | UxTXREG2 | UxTXREG1 | UxTXREG0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **LAST:** Last Byte Indicator for Smart Card Support bits(1)

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **UxTXREG8:** Data of the Transmitted Character bit (in 9-bit mode)

bit 7-0 **UxTXREG<7:0>:** Data of the Transmitted Character bits

**Note 1:** This bit is only available for UART1 and UART2.

**REGISTER 18-4: UxADMD: UARTx ADDRESS MATCH DETECT REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADMMASK7 | ADMMASK6 | ADMMASK5 | ADMMASK4 | ADMMASK3 | ADMMASK2 | ADMMASK1 | ADMMASK0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADMADDR7 | ADMADDR6 | ADMADDR5 | ADMADDR4 | ADMADDR3 | ADMADDR2 | ADMADDR1 | ADMADDR0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **ADMMASK<7:0>:** UARTx ADMADDR<7:0> (UxADMD<7:0>) Masking bits

For ADMMASK<x>:

1 = ADMADDR<x> is used to detect the address match

0 = ADMADDR<x> is not used to detect the address match

bit 7-0 **ADMADDR<7:0>:** UARTx Address Detect Task Off-Load bits

Used with the ADMMASK<7:0> bits (UxADMD<15:8>) to off-load the task of detecting the address character from the processor during Address Detect mode.

## 23.0 32-BIT PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

**Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"32-Bit Programmable Cyclic Redundancy Check (CRC)"** (DS30009729). The information in this data sheet supersedes the information in the FRM.

The 32-bit programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-programmable CRC polynomial equation, up to 32 bits
- Programmable shift direction (little or big-endian)
- Independent data and polynomial lengths
- Configurable interrupt output
- Data FIFO

Figure 23-1 displays a simplified block diagram of the CRC generator. A simple version of the CRC shift engine is displayed in Figure 23-2.

**FIGURE 23-1: CRC MODULE BLOCK DIAGRAM**

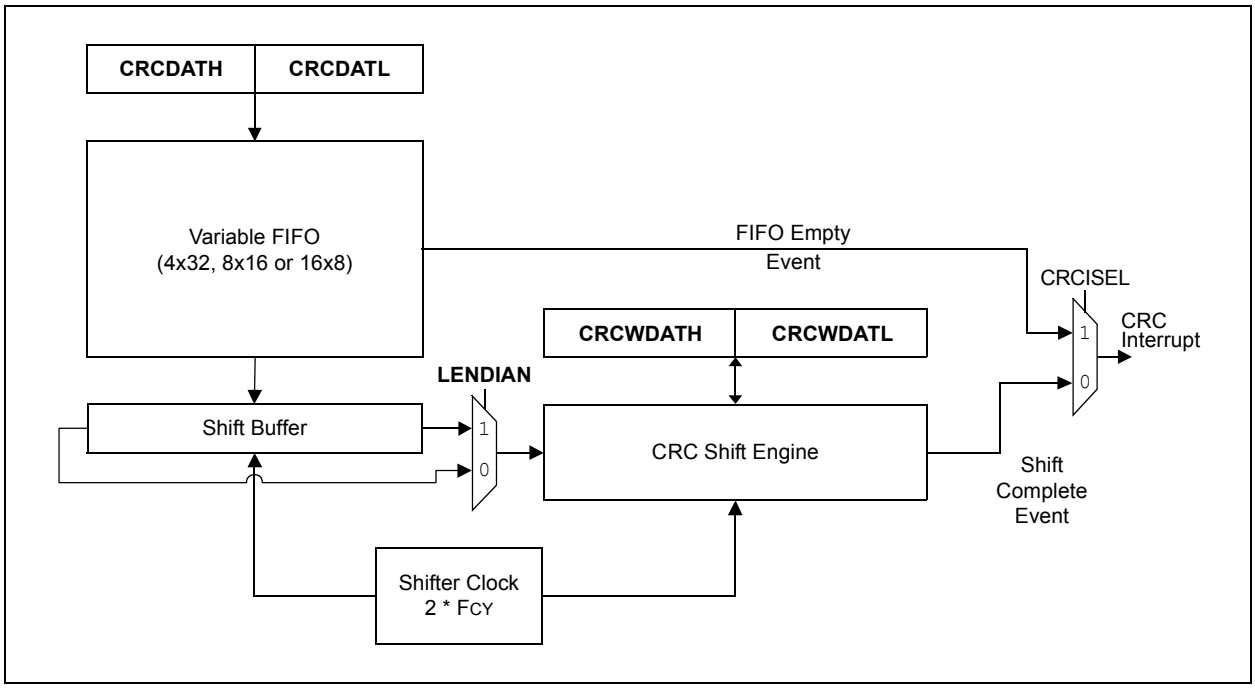
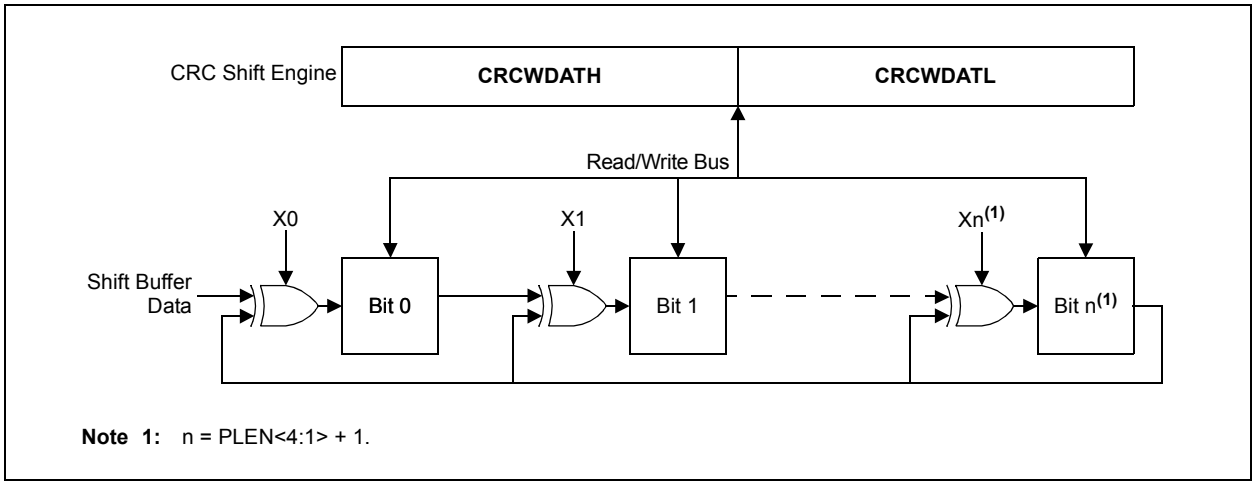



**FIGURE 23-2: CRC SHIFT ENGINE DETAIL**




**Note 1:** n = PLEN<4:1> + 1.

**REGISTER 24-9: AD1CSSH: A/D INPUT SCAN SELECT REGISTER (HIGH WORD)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| CSS<31:27> | | | | | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-11 **CSS<31:27>:** A/D Input Scan Selection bits
1 = Includes corresponding channel for input scan
0 = Skips channel for input scan

bit 10-0 **Unimplemented:** Read as '0'

**REGISTER 24-10: AD1CSSL: A/D INPUT SCAN SELECT REGISTER (LOW WORD)**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | CSS<14:8>(1) | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CSS<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-0 **CSS<14:0>:** A/D Input Scan Selection bits(1)
1 = Includes corresponding channel for input scan
0 = Skips channel for input scan

**Note 1:** The CSS<12:10> bits are unimplemented in 28-pin devices, read as '0'.

## 27.2 Measuring Time

Time measurements on the pulse width can be similarly performed using the A/D module's Internal Capacitor (CAD) and a precision resistor for current calibration. Figure 27-2 displays the external connections used for time measurements, and how the CTMU and A/D modules are related in this application. This example also shows both edge events coming from the external CTEDx pins, but other configurations using internal edge sources are possible.

## 27.3 Pulse Generation and Delay

The CTMU module can also generate an output pulse with edges that are not synchronous with the device's system clock. More specifically, it can generate a pulse with a programmable delay from an edge event input to the module.

When the module is configured for pulse generation delay by setting the TGEN bit (CTMUCON1<12>), the internal current source is connected to the B input of Comparator 2. A Capacitor (CDELAY) is connected to the Comparator 2 pin, C2INB, and the Comparator Voltage Reference, CVREF, is connected to C2INA. CVREF is then configured for a specific trip point. The module begins to charge CDELAY when an edge event is detected. When CDELAY charges above the CVREF trip point, a pulse is output on CTPLS. The length of the pulse delay is determined by the value of CDELAY and the CVREF trip point.

Figure 27-3 illustrates the external connections for pulse generation, as well as the relationship of the different analog modules required. While CTED1 is shown as the input pulse source, other options are available. A detailed discussion on pulse generation with the CTMU module is provided in the *"dsPIC33/PIC24 Family Reference Manual"*.

**FIGURE 27-2: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR TIME MEASUREMENT**

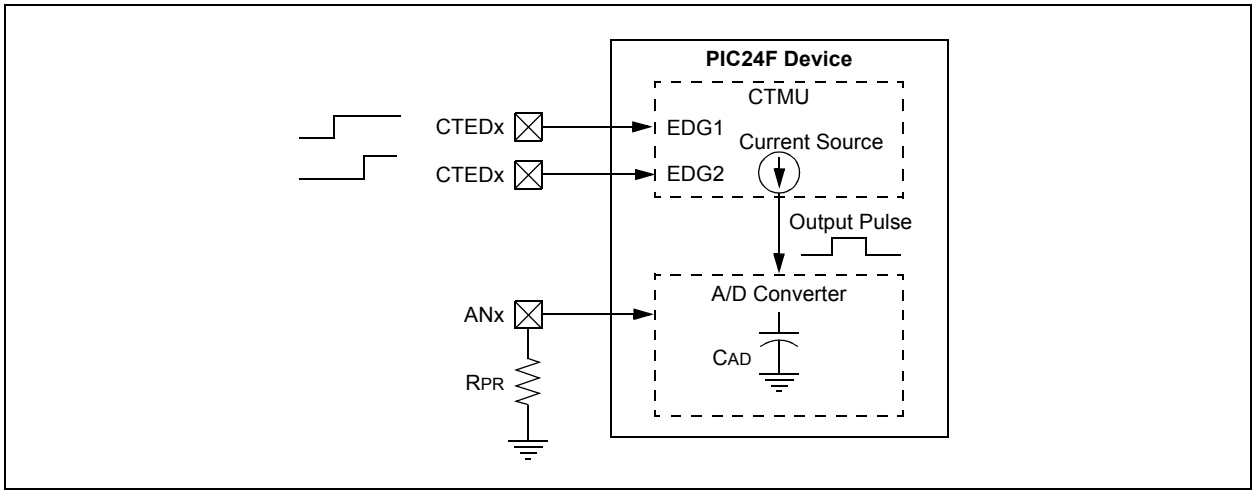
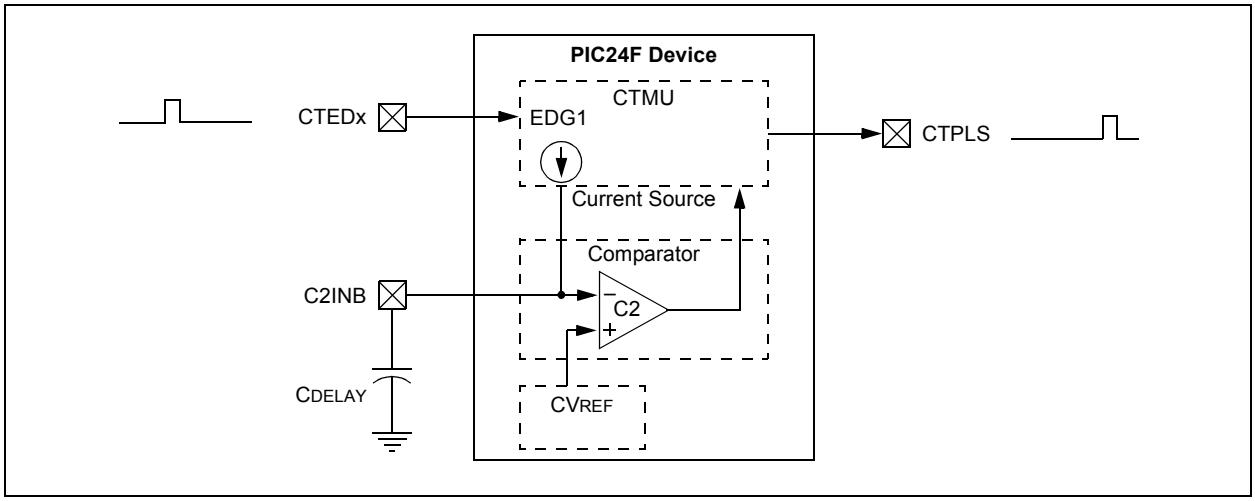
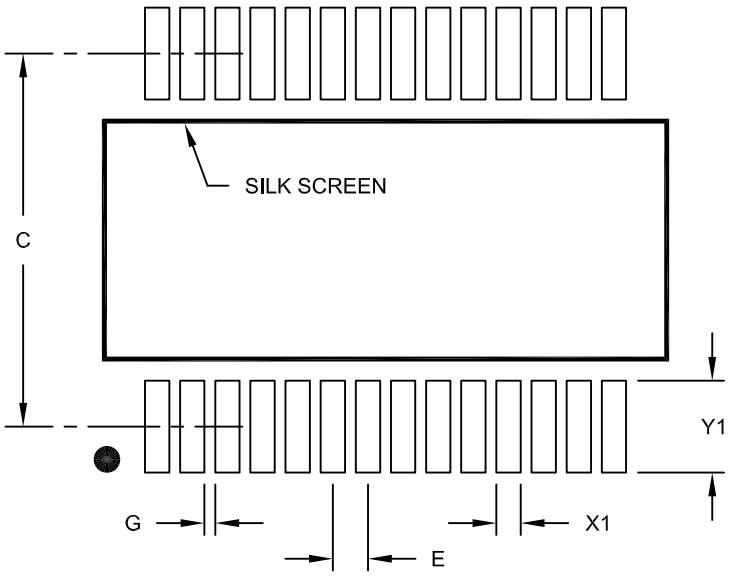



**FIGURE 27-3: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR PULSE DELAY GENERATION**



28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.65 BSC | |
| Contact Pad Spacing | C | | 7.20 | |
| Contact Pad Width (X28) | X1 | | | 0.45 |
| Contact Pad Length (X28) | Y1 | | | 1.75 |
| Distance Between Pads | G | 0.20 | | |

Notes:

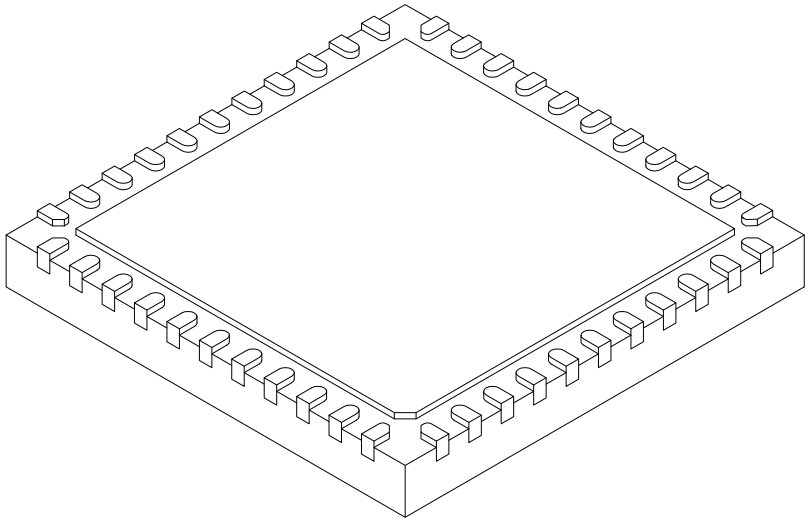
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

## 44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 44 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 8.00 BSC | |
| Exposed Pad Width | E2 | 6.25 | 6.45 | 6.60 |
| Overall Length | D | | 8.00 BSC | |
| Exposed Pad Length | D2 | 6.25 | 6.45 | 6.60 |
| Terminal Width | b | 0.20 | 0.30 | 0.35 |
| Terminal Length | L | 0.30 | 0.40 | 0.50 |
| Terminal-to-Exposed-Pad | K | 0.20 | - | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103C Sheet 2 of 2

**Note the following details of the code protection feature on Microchip devices:**

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