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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	AES, Brown-out Detect/Reset, DMA, I ² S, HLVD, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj64ga202t-i-mm

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3.0 CPU

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the CPU, refer to the "dsPIC33/PIC24 Family Reference Manual", "CPU with Extended Data Space (EDS)" (DS39732). The information in this data sheet supersedes the information in the FRM.

The PIC24F CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set and a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M instructions of user program memory space. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double-word move (MOV.D) instruction and the table instructions. Overhead-free program loop constructs are supported using the REPEAT instructions, which are interruptible at any point.

PIC24F devices have sixteen, 16-bit Working registers in the programmer's model. Each of the Working registers can act as a Data, Address or Address Offset register. The 16th Working register (W15) operates as a Software Stack Pointer (SSP) for interrupts and calls.

The lower 32 Kbytes of the Data Space (DS) can be accessed linearly. The upper 32 Kbytes of the Data Space are referred to as Extended Data Space to which the extended data RAM, EPMP memory space or program memory can be mapped.

The Instruction Set Architecture (ISA) has been significantly enhanced beyond that of the PIC18, but maintains an acceptable level of backward compatibility. All PIC18 instructions and addressing modes are supported, either directly, or through simple macros. Many of the ISA enhancements have been driven by compiler efficiency needs. The core supports Inherent (no operand), Relative, Literal and Memory Direct Addressing modes along with three groups of addressing modes. All modes support Register Direct and various Register Indirect modes. Each group offers up to seven addressing modes. Instructions are associated with predefined addressing modes depending upon their functional requirements.

For most instructions, the core is capable of executing a data (or program data) memory read, a Working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing trinary operations (that is, A + B = C) to be executed in a single cycle.

A high-speed, 17-bit x 17-bit multiplier has been included to significantly enhance the core arithmetic capability and throughput. The multiplier supports Signed, Unsigned and Mixed mode, 16-bit x 16-bit or 8-bit x 8-bit, integer multiplication. All multiply instructions execute in a single cycle.

The 16-bit ALU has been enhanced with integer divide assist hardware that supports an iterative non-restoring divide algorithm. It operates in conjunction with the REPEAT instruction looping mechanism and a selection of iterative divide instructions to support 32-bit (or 16-bit), divided by 16-bit, integer signed and unsigned division. All divide operations require 19 cycles to complete but are interruptible at any cycle boundary.

The PIC24F has a vectored exception scheme with up to 8 sources of non-maskable traps and up to 118 interrupt sources. Each interrupt source can be assigned to one of seven priority levels.

A block diagram of the CPU is shown in Figure 3-1.

3.1 Programmer's Model

The programmer's model for the PIC24F is shown in Figure 3-2. All registers in the programmer's model are memory-mapped and can be manipulated directly by instructions.

A description of each register is provided in Table 3-1. All registers associated with the programmer's model are memory-mapped.

TABLE 4-3: CPU CORE REGISTERS MAP

4 -J.	0.00																
Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
0000								Working	Register 0								0000
0002								Working	Register 1								0000
0004								Working	Register 2								0000
0006								Working	Register 3								0000
0008								Working	Register 4								0000
000A								Working	Register 5								0000
000C								Working	Register 6								0000
000E		Working Register 7											0000				
0010													0000				
0012								Working	Register 9								0000
0014								Working F	Register 10								0000
0016								Working F	Register 11								0000
0018								Working F	Register 12								0000
001A								Working F	Register 13								0000
001C								Working F	Register 14								0000
001E								Working F	Register 15								0800
0020							Stack	Pointer Lin	nit Value Re	egister							XXXX
002E							Progra	m Counter	Low Word F	Register							0000
0030	—	—	—	—	—	—	—	—			Progra	m Counter I	High Word	Register			0000
0032	—	—	—	—	—	—			Ext	ended Data	Space Re	ad Page Ac	ldress Regi	ister			0001
0034	—	—	—	—	—	—	—			Extended	d Data Spa	ce Write Pa	ge Address	s Register			0001
0036							REP	EAT LOOP C	Counter Reg	jister							XXXX
0042	—	-	_	_	—	_	—	DC	IPL2	IPL1	IPL0	RA	Ν	OV	Z	С	0000
0044	—	-	_	—	_	—	_	_	-	_	-	—	IPL3	r	—	—	0004
0052	_	_						Disabl	e Interrupts	Counter R	egister						xxxx
0054	_	— — — — — Table Memory Page Address Register 00										0000					
	Addr 0000 0002 0004 0006 0008 000A 000C 000E 0010 0012 0014 0016 0018 0014 0016 0018 0014 0016 0018 0012 0014 0012 0020 002E 0030 0032 0034 0036 0042 0044 0052	Addr Bit 15 0000	Addr Bit 15 Bit 14 0000	AddrBit 15Bit 14Bit 130000	AddrBit 15Bit 14Bit 13Bit 120000	AddrBit 15Bit 14Bit 13Bit 12Bit 110000	AddrBit 15Bit 14Bit 13Bit 12Bit 11Bit 100000000200040006000800080000400004000500060006000700080009000900090000000100012001200140015001600180016001700180019001900100010001100120013001400140015001600170018001900190019001900100011001200120013001400340034003400340034003400340034003400340034003400340034003400340034003500350036003600360037003800380039003900390039003900390039003900390039003900390	Addr Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 0000	Addr Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 0000	Addr Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 0000	Addr Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 8 Bit 8 Bit 7 Bit 6 0000	AddrBit 15Bit 14Bit 13Bit 12Bit 11Bit 10Bit 9Bit 8Bit 7Bit 6Bit 50000	Addr Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 0000	AddrBit 15Bit 14Bit 13Bit 12Bit 11Bit 10Bit 9Bit 8Bit 7Bit 6Bit 5Bit 4Bit 30000	AddrBit 15Bit 14Bit 13Bit 12Bit 11Bit 10Bit 9Bit 8Bit 7Bit 6Bit 5Bit 4Bit 3Bit 200000002000400060006000700080008000000000000000000000000000000010002000200030004000400050006000600070008000800090009000900090009001000100010001100120012001300140014001500150016001600170018001800190019001900100010001000110012001200130014001400150015001600170018001800190019001900190019001900190019001900190019001900190019001900190	Addr Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 0000	Addr Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0 0000

Legend: — = unimplemented, read as '0'; r = reserved, do not modify; x = unknown value on Reset. Reset values are shown in hexadecimal.

TABLE 4-10: UART REGISTER MAP

IABLE 4	-10:	UARIF	KEGIS I															_
File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0500	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U1STA	0502	UTXISEL1	UTXINV	UTXISEL0	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0504	LAST	_	_	_	—	_	_				U1T	XREG<8:0>	•				XXXX
U1RXREG	0506	_	_	_		_	_					U1R	XREG<8:0>	•				0000
U1BRG	0508								U1BRG	BRG<15:0>							0000	
U1ADMD	050A				ADMMAS	SK<7:0>				ADMADDR<7:0>							0000	
U1SCCON	050C	_	_	_	_	_	_	_	_	_	_	TXRPT1	TXRPT0	CONV	T0PD	PTRCL	SCEN	0000
U1SCINT	050E	_	_	RXRPTIF	TXRPTIF	—	_	WTCIF	GTCIF	_	PARIE	RXRPTIE	TXRPTIE	_	_	WTCIE	GTCIE	0000
U1GTC	0510	_	_	_	_	—	_	_				G	TC<8:0>					0000
U1WTCL	0512								WTC<	15:0>								0000
U1WTCH	0514	_	_	_	_	_	_	_	_				WTC<23	:16>				0000
U2MODE	0516	UARTEN	_	USIDL	IREN	RTSMD	_	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U2STA	0518	UTXISEL1	UTXINV	UTXISEL0	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG	051A	LAST	_	_	_	—	_	_				U2T	XREG<8:0>	•				XXXX
U2RXREG	051C	_	_	_	_	—	_	_				U2R	XREG<8:0>	>				0000
U2BRG	051E								U2BRG	<15:0>								0000
U2ADMD	0520				ADMMAS	SK<7:0>							ADMADDR	R<7:0>				0000
U2SCCON	0522	—	—	—	_	—		_		—	_	TXRPT1	TXRPT0	CONV	T0PD	PTRCL	SCEN	0000
U2SCINT	0524	—	—	RXRPTIF	TXRPTIF	_		WTCIF	GTCIF	—	PARIE	RXRPTIE	TXROTIE		—	WTCIE	GTCIE	0000
U2GTC	0526	—	—	—	_	_		_				G	TC<8:0>					0000
U2WTCL	0528								WTC<	15:0>								0000
U2WTCH	052A	—	—	—	_	_		_					WTC<23	:16>				0000
U3MODE	052C	UARTEN	—	USIDL	IREN	RTSMD		UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U3STA	052E	UTXISEL1	UTXINV	UTXISEL0	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U3TXREG	0530	LAST	—	—	_	_		_				U3T2	XREG<8:0>	•				XXXX
U3RXREG	0532	—	—	—	_	_		_				U3R	XREG<8:0>	•				0000
U3BRG	0534								U3BRG	<15:0>								0000
U3ADMD	0536				ADMMAS	SK<7:0>							ADMADDR	8<7:0>				0000
U4MODE	0538	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	ENO WAKE LPBACK ABAUD URXINV BRGH PDSEL1 PDSEL0 STSEL						0000		
U4STA	053A	UTXISEL1	UTXINV	UTXISEL0	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	RMT URXISEL1 URXISEL0 ADDEN RIDLE PERR FERR OERR URXDA						0110		
U4TXREG	053C	LAST	—	—	_	—	-	_		U4TXREG<8:0>							XXXX	
U4RXREG	053E	_	—	—	—	—	-	_				U4R	XREG<8:0>	•				0000
U4BRG	0540								U4BRG	<15:0>								0000
U4ADMD	0542				ADMMAS	SK<7:0>							ADMADDR	R<7:0>				0000

Legend: — = unimplemented, read as '0'; x = unknown value on Reset. Reset values are shown in hexadecimal.

TABLE 4-13: SPI3 REGISTER MAP

T-10			••••														
Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
0338	SPIEN	—	SPISIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	DISSCK	MCLKEN	SPIFE	ENHBUF	0000
033A	AUDEN	SPISGNEXT	IGNROV	IGNTUR	AUDMONO	URDTEN	AUDMOD1	AUDMOD0	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT2	FRMCNT1	FRMCNT0	0000
033C	_	_												0000			
0340	_	_	_	FRMERR	SPIBUSY	_	_	SPITUR	SRMT	SPIROV	SPIRBE	_	SPITBE	_	SPITBF	SPIRBF	0028
0342	—	-	RXELM5	RXELM4	RXELM3	RXELM2	RXELM1	RXELM0	—	—	TXELM5	TXELM4	TXELM3	TXELM2	TXELM1	TXELM0	0000
0344								SPI3BL	JFL<15:0>								0000
0346								SPI3BU	FH<31:16>								0000
0348	_	_	_						S	PI3BRG<12:0	>						0000
034C	_	_	_	FRMERREN	BUSYEN	_	_	SPITUREN	SRMTEN	SPIROVEN	SPIRBEN	_	SPITBEN	_	SPITBFEN	SPIRBFEN	0000
034E	RXWIEN	IEN - RXMSK5 RXMSK4 RXMSK3 RXMSK2 RXMSK1 RXMSK0 TXWIEN - TXMSK5 TXMSK4 TXMSK3 TXMSK2 TXMSK1 TXMSK0 0000										0000					
0350		SPI3URDTL<15:0> 000											0000				
0352	SPI3URDTH<31:16> 000											0000					
	Addr 0338 033A 033C 0340 0342 0344 0346 0348 0346 0348 0346 0348	Addr Bit 15 0338 SPIEN 033A AUDEN 033C 0340 0342 0344 0345 0346 0347 0348 0349 0340 0341 0342 0343 0344 0345 0346 0347 0348 0349 0340	Addr Bit 15 Bit 14 0338 SPIEN — 033A AUDEN SPISGNEXT 033C — — 0340 — — 0342 — — 0344 — — 0345 — — 0346 — — 0347 — — 0348 — — 0346 — — 0347 — — 0348 — — 0349 — — 0340 — — 0341 — — 0342 — — 0344 — — 0345 — — 0346 — — 0347 — — 0348 — — 0349 — — 0340 — — 0345	Addr Bit 15 Bit 14 Bit 13 0338 SPIEN — SPISIDL 033A AUDEN SPISGNEXT IGNROV 033C — — — 0340 — — — 0342 — — RXELM5 0344 — — — 0346 — — — 0346 — — — 0348 — — — 0346 — — — 0346 — — — 0347 — — — 0348 — — — 0342 — — — 0344 — — — 0345 — — — 0346 — — — 0348 — — — 0345 — — — 0346	Addr Bit 15 Bit 14 Bit 13 Bit 12 0338 SPIEN — SPISIDL DISSDO 033A AUDEN SPISGNEXT IGNROV IGNTUR 033C — — — — 0340 — — — FRMERR 0342 — — RXELM5 RXELM4 0344 — — RXELM5 RXELM4 0344 — — — — 0346 — — RXELM5 RXELM4 0344 — — — — 0346 — — — — 0348 — — — FRMERREN 0342 — — — FRMERREN 0346 — — — FRMERREN 0345 — — — FRMERREN 0346 — — — FRMERREN 0346 —<	Addr Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 0338 SPIEN — SPISIDL DISSDO MODE32 033A AUDEN SPISGNEXT IGNROV IGNTUR AUDMONO 033C — — — — — 0340 — — — FRMERR SPIBUSY 0342 — — RXELM5 RXELM4 RXELM3 0344 — — RXELM5 RXELM4 RXELM3 0344 — — — — — 0346 — — RXELM5 RXELM4 RXELM3 0344 — — — — — — 0344 — — — — — — — 0344 — — — — FRMERREN BUSYEN _ 0344 RXWIEN — RXMSK5 RXMSK4 RXMSK3 _	Addr Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 0338 SPIEN — SPISIDL DISSDO MODE32 MODE16 033A AUDEN SPISGNEXT IGNROV IGNTUR AUDMONO URDTEN 033C — — — — — — 0340 — — — FRMERR SPIBUSY — 0342 — — RXELM5 RXELM4 RXELM3 RXELM2 0344 — — RXELM5 RXELM4 RXELM3 RXELM2 0344 — — — — — — 0344 — — — FRMERREN BUSYEN — 0348 — — — FRMERREN BUSYEN — 0344 RXWIEN — RXMSK5 RXMSK4 RXMSK3 RXMSK2 0345 — — — FRMERREN BUSYEN —	AddrBit 15Bit 14Bit 13Bit 12Bit 11Bit 10Bit 90338SPIEN—SPISIDLDISSDOMODE32MODE16SMP033AAUDENSPISGNEXTIGNROVIGNTURAUDMONOURDTENAUDMOD1033C——————0340———FRMERRSPIBUSY——0342——RXELM5RXELM4RXELM3RXELM2RXELM10344	AddrBit 15Bit 14Bit 13Bit 12Bit 11Bit 10Bit 9Bit 80338SPIEN—SPISIDLDISSDOMODE32MODE16SMPCKE033AAUDENSPISGNEXTIGNROVIGNTURAUDMONOURDTENAUDMOD1AUDMOD0033C————————0340————————0342——RXELM5RXELM4RXELM3RXELM2RXELM1RXELM00342——RXELM5RXELM4RXELM3RXELM2RXELM1RXELM00342———RXELM5RXELM4RXELM3RXELM2RXELM1RXELM00344———RXELM5RXELM4RXELM3RXELM2RXELM1RXELM00348———————SPIJBU0346—————SPIJUREN0346RXWIEN———SPIJUREN0346RXWIEN———SPIJUREN0347M———SPIJUREN0348RXWIEN———SPIJUREN0344RXWIEN———SPIJUREN0345MM———SPIJUREN0346MMMRXMSK5RXMSK3RXMSK2RXMSK10347MMMM <td>Addr Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 0338 SPIEN — SPISIDL DISSDO MODE32 MODE16 SMP CKE SSEN 033A AUDEN SPISGNEXT IGNROV IGNTUR AUDMONO URDTEN AUDMOD1 AUDMOD0 FRMEN 033C — — — — — — — 0340 — — — FRMERR SPIBUSY — — SPITUR SRMT 0342 — — RXELM5 RXELM4 RXELM3 RXELM2 RXELM1 RXELM0 — 0344 — — RXELM5 RXELM4 RXELM3 RXELM2 RXELM1 RXELM0 — 0344 — — — RXELM5 RXELM4 RXELM3 RXELM2 RXELM1 RXELM0 — 0348 — — — FRMERREN BUSYEN — — SPITUREN SRMTEN 0342 — — — FRMERREN BUSYEN — — SPI3BUFL<15:> S 0346 — — — FRMERREN <td< td=""><td>AddrBit 15Bit 14Bit 13Bit 12Bit 11Bit 10Bit 9Bit 8Bit 7Bit 60338SPIENSPISIDLDISSDOMODE32MODE16SMPCKESSENCKP033AAUDENSPISGNEXTIGNROVIGNTURAUDMONOURDTENAUDMOD1AUDMOD0FRMENFRMSYNC033C0340SPITURSRMTSPIROV0342RXELM5RXELM4RXELM3RXELM2RXELM1RXELM00344RXELM5RXELM4RXELM3RXELM2RXELM1RXELM00346SPI3BUFL<15.0>SPI3BUFLSPI3BRG<12:0</td>0346FRMERRENBUSYENSPITURENSRMTENSPIROVEN0346FRMERRENBUSYENSPITURENSRMTENSPIROVEN0346FRMERRENBUSYENSPITURENSRMTENSPIROVEN0346FRMERRENBUSYENSPITURENSRMTENSPIROVEN0347SPITURENSRMTENSPIROVENSPITURENSRMTENSPIROVEN0346SPITURENSRMTENSPIROVEN-</td<></td> <td>AddrBit 15Bit 14Bit 13Bit 12Bit 11Bit 10Bit 9Bit 9Bit 8Bit 7Bit 6Bit 50338SPIEN—SPISIDLDISSDOMODE32MODE16SMPCKESSENCKPMSTEN0334AUDENSPISGNEXTIGNROVIGNTURAUDMONOURDTENAUDMOD1AUDMOD0FRMENFRMSYNCFRMPOL0332———————————0340———FRMERRSPIBUSY——SPITURSRMTSPIROVSPIRBE0342——RXELM5RXELM4RXELM3RXELM2RXELM1RXELM0————0344——RXELM5RXELM4RXELM3RXELM2RXELM1RXELM0——TXELM50348——————SPITURSRMTENSPIROVSPIRBEN0344———————————0346———RXELM5RXELM5RXELM5SPITURENSPIROVSPIRBEN0348———————SPITURENSRMTENSPIROVEN0346————SPITURENSRMTENSPIROVENSPIRBEN0346————SPITURENSRMTENSPIROVENSPIRBEN0346M—<</td> <td>AddrBit 15Bit 14Bit 13Bit 12Bit 11Bit 10Bit 9Bit 9Bit 8Bit 7Bit 6Bit 5Bit 40338SPIENSPISIDLDISSDOMODE32MODE16SMPCKESSENCKPMSTENDISSDI0334AUDENSPISGNEXTIGNROVIGNTURAUDMONOURDTENAUDMOD1AUDMOD0FRMENFRMSYNCFRMPOLMSSEN03320340SPITURSRMTSPIROVSPIRBE0342RXELM5RXELM4RXELM3RXELM2RXELM1RXELM0TXELM5TXELM40344SPI3BUFISRMTSPIROVSPIRBESPI3BEG<12:0>0346SPITURNSRMTENSPIROVENSPIRBEN0346SPITURNSRMTENSPIROVENSPIRBEN0347SPITURNSRMTENSPIROVENSPIRBEN0348SPITURNSRMTENSPIROVENSPIRBEN0346SPITURNSRMTENSPIROVENSPIRBEN0347SPITURN<td>AddrBit 15Bit 14Bit 13Bit 12Bit 11Bit 10Bit 9Bit 8Bit 7Bit 6Bit 6Bit 5Bit 4Bit 30338SPIEN-SPISIDLDISSD0MODE32MODE16SMPCKESSENCKPMSTENDISSD1DISSCK0334AUDENSPISGNEXTIGNROVIGNTURAUDMONOURDTENAUDMOD1AUDMOD0FRMENFRMSYNCFRMPOLMSSENFRMSYPW0332V0340SPITBESPITBESPITBE0342FRMERRSPIBUSYSPITURSRMTSPIROVSPIRBESPITBE0342RXELM5RXELM4RXELM3RXELM2RXELM1RXELM0TXELM5TXELM4TXELM30344SPITURSRMTSPIROVSPIRBESPITBE0346SPITURSRMTENSPIROVENSPIRBENSPITBEN0346SPITBENSPITURSPIROVSPIRBENSPITBEN0346SPITURENSRMTENSPIROVENSPIRBENSPITBENSPITBEN0346SPITURENSRMTENSPI</td><td>AddrBit 13Bit 13Bit 12Bit 11Bit 10Bit 9Bit 8Bit 7Bit 6Bit 5Bit 4Bit 3Bit 3Bit 20338SPIEN—SPISIDLDISSD0MODE32MODE16SMPCKESSENCKPMSTENDISSD1DISSC4MCLKEN0338AUDENSPISGNEXTIGNROVIGNTURAUDMON0URDTENAUDMOD1AUDMOD0FRMENFRMSYNCFRMPOLMSSENFRMSYPWFRMCNT20333VLENGTH<4:0</td>0340SPITURSRMTSPIROVSPIRBESPITBE0342RXELM5RXELM4RXELM3RXELM2RXELM1RXELM0TXELM5TXELM4TXELM3TXELM20344SPITURSRMTSPIROVSPIRBESPITBE</td> <td>AddrBit 15Bit 14Bit 13Bit 12Bit 11Bit 10Bit 9Bit 8Bit 7Bit 6Bit 5Bit 4Bit 3Bit 3Bit 2Bit 10338SPIEN-SPISIDLDISSDOMODE32MODE16SMPCKESSENCKPMSTENDISSDIDISSCKMCLKENSPIFE0334AUDENSPISGNEXTIGNROVIGNTURAUDMONOURDTENAUDMOD1AUDMOD0FRMENFRMSYNCFRMPOLMSSENFRMSYPWFRMCNT2FRMCNT2FRMCNT10336VLENGTH<4.D>0337VLENGTH<4.D>0336VLENGTH<4.D>0336VLENGTH<4.D>0337SPITESPIRT0340RXELMSRXELMSRXELMSRXELMSRXELMSRXELMSSPITUESRMTSPIROVSPIRBESPITBESPITBE0342SPITUESRMTSPIROVENSPIRBESPITBESPITBESPITE0344SPITUESRMTSPIROVE</td> <td>AddrBit 13Bit 13Bit 13Bit 12Bit 10Bit 9Bit 8Bit 7Bit 6Bit 5Bit 4Bit 3Bit 3Bit 2Bit 1Bit 00338SPIENSPISDLDISSD0MODE32MODE16SMPCKESSENCKPMSTENDISSD1DISSD1DISSCKMCLKENSPIFEENHBUF0334AUDENSPISGNEXTIGNROVIGNTURAUDMON0URDTENAUDMOD1AUDMOD0FRMENFRMSYNCFRMCD1MSSENFRMSYPWFRMCNT2FRMCNT2FRMCNT2FRMCNT1FRMCNT00336FRMSYNCFRMC01MSSENFRMSYPWFRMCNT2FRMCNT2FRMCNT1FRMCNT00336FRMCNT2</td>	Addr Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 0338 SPIEN — SPISIDL DISSDO MODE32 MODE16 SMP CKE SSEN 033A AUDEN SPISGNEXT IGNROV IGNTUR AUDMONO URDTEN AUDMOD1 AUDMOD0 FRMEN 033C — — — — — — — 0340 — — — FRMERR SPIBUSY — — SPITUR SRMT 0342 — — RXELM5 RXELM4 RXELM3 RXELM2 RXELM1 RXELM0 — 0344 — — RXELM5 RXELM4 RXELM3 RXELM2 RXELM1 RXELM0 — 0344 — — — RXELM5 RXELM4 RXELM3 RXELM2 RXELM1 RXELM0 — 0348 — — — FRMERREN BUSYEN — — SPITUREN SRMTEN 0342 — — — FRMERREN BUSYEN — — SPI3BUFL<15:> S 0346 — — — FRMERREN <td< td=""><td>AddrBit 15Bit 14Bit 13Bit 12Bit 11Bit 10Bit 9Bit 8Bit 7Bit 60338SPIENSPISIDLDISSDOMODE32MODE16SMPCKESSENCKP033AAUDENSPISGNEXTIGNROVIGNTURAUDMONOURDTENAUDMOD1AUDMOD0FRMENFRMSYNC033C0340SPITURSRMTSPIROV0342RXELM5RXELM4RXELM3RXELM2RXELM1RXELM00344RXELM5RXELM4RXELM3RXELM2RXELM1RXELM00346SPI3BUFL<15.0>SPI3BUFLSPI3BRG<12:0</td>0346FRMERRENBUSYENSPITURENSRMTENSPIROVEN0346FRMERRENBUSYENSPITURENSRMTENSPIROVEN0346FRMERRENBUSYENSPITURENSRMTENSPIROVEN0346FRMERRENBUSYENSPITURENSRMTENSPIROVEN0347SPITURENSRMTENSPIROVENSPITURENSRMTENSPIROVEN0346SPITURENSRMTENSPIROVEN-</td<>	AddrBit 15Bit 14Bit 13Bit 12Bit 11Bit 10Bit 9Bit 8Bit 7Bit 60338SPIENSPISIDLDISSDOMODE32MODE16SMPCKESSENCKP033AAUDENSPISGNEXTIGNROVIGNTURAUDMONOURDTENAUDMOD1AUDMOD0FRMENFRMSYNC033C0340SPITURSRMTSPIROV0342RXELM5RXELM4RXELM3RXELM2RXELM1RXELM00344RXELM5RXELM4RXELM3RXELM2RXELM1RXELM00346SPI3BUFL<15.0>SPI3BUFLSPI3BRG<12:0	AddrBit 15Bit 14Bit 13Bit 12Bit 11Bit 10Bit 9Bit 9Bit 8Bit 7Bit 6Bit 50338SPIEN—SPISIDLDISSDOMODE32MODE16SMPCKESSENCKPMSTEN0334AUDENSPISGNEXTIGNROVIGNTURAUDMONOURDTENAUDMOD1AUDMOD0FRMENFRMSYNCFRMPOL0332———————————0340———FRMERRSPIBUSY——SPITURSRMTSPIROVSPIRBE0342——RXELM5RXELM4RXELM3RXELM2RXELM1RXELM0————0344——RXELM5RXELM4RXELM3RXELM2RXELM1RXELM0——TXELM50348——————SPITURSRMTENSPIROVSPIRBEN0344———————————0346———RXELM5RXELM5RXELM5SPITURENSPIROVSPIRBEN0348———————SPITURENSRMTENSPIROVEN0346————SPITURENSRMTENSPIROVENSPIRBEN0346————SPITURENSRMTENSPIROVENSPIRBEN0346M—<	AddrBit 15Bit 14Bit 13Bit 12Bit 11Bit 10Bit 9Bit 9Bit 8Bit 7Bit 6Bit 5Bit 40338SPIENSPISIDLDISSDOMODE32MODE16SMPCKESSENCKPMSTENDISSDI0334AUDENSPISGNEXTIGNROVIGNTURAUDMONOURDTENAUDMOD1AUDMOD0FRMENFRMSYNCFRMPOLMSSEN03320340SPITURSRMTSPIROVSPIRBE0342RXELM5RXELM4RXELM3RXELM2RXELM1RXELM0TXELM5TXELM40344SPI3BUFISRMTSPIROVSPIRBESPI3BEG<12:0>0346SPITURNSRMTENSPIROVENSPIRBEN0346SPITURNSRMTENSPIROVENSPIRBEN0347SPITURNSRMTENSPIROVENSPIRBEN0348SPITURNSRMTENSPIROVENSPIRBEN0346SPITURNSRMTENSPIROVENSPIRBEN0347SPITURN <td>AddrBit 15Bit 14Bit 13Bit 12Bit 11Bit 10Bit 9Bit 8Bit 7Bit 6Bit 6Bit 5Bit 4Bit 30338SPIEN-SPISIDLDISSD0MODE32MODE16SMPCKESSENCKPMSTENDISSD1DISSCK0334AUDENSPISGNEXTIGNROVIGNTURAUDMONOURDTENAUDMOD1AUDMOD0FRMENFRMSYNCFRMPOLMSSENFRMSYPW0332V0340SPITBESPITBESPITBE0342FRMERRSPIBUSYSPITURSRMTSPIROVSPIRBESPITBE0342RXELM5RXELM4RXELM3RXELM2RXELM1RXELM0TXELM5TXELM4TXELM30344SPITURSRMTSPIROVSPIRBESPITBE0346SPITURSRMTENSPIROVENSPIRBENSPITBEN0346SPITBENSPITURSPIROVSPIRBENSPITBEN0346SPITURENSRMTENSPIROVENSPIRBENSPITBENSPITBEN0346SPITURENSRMTENSPI</td> <td>AddrBit 13Bit 13Bit 12Bit 11Bit 10Bit 9Bit 8Bit 7Bit 6Bit 5Bit 4Bit 3Bit 3Bit 20338SPIEN—SPISIDLDISSD0MODE32MODE16SMPCKESSENCKPMSTENDISSD1DISSC4MCLKEN0338AUDENSPISGNEXTIGNROVIGNTURAUDMON0URDTENAUDMOD1AUDMOD0FRMENFRMSYNCFRMPOLMSSENFRMSYPWFRMCNT20333VLENGTH<4:0</td> 0340SPITURSRMTSPIROVSPIRBESPITBE0342RXELM5RXELM4RXELM3RXELM2RXELM1RXELM0TXELM5TXELM4TXELM3TXELM20344SPITURSRMTSPIROVSPIRBESPITBE	AddrBit 15Bit 14Bit 13Bit 12Bit 11Bit 10Bit 9Bit 8Bit 7Bit 6Bit 6Bit 5Bit 4Bit 30338SPIEN-SPISIDLDISSD0MODE32MODE16SMPCKESSENCKPMSTENDISSD1DISSCK0334AUDENSPISGNEXTIGNROVIGNTURAUDMONOURDTENAUDMOD1AUDMOD0FRMENFRMSYNCFRMPOLMSSENFRMSYPW0332V0340SPITBESPITBESPITBE0342FRMERRSPIBUSYSPITURSRMTSPIROVSPIRBESPITBE0342RXELM5RXELM4RXELM3RXELM2RXELM1RXELM0TXELM5TXELM4TXELM30344SPITURSRMTSPIROVSPIRBESPITBE0346SPITURSRMTENSPIROVENSPIRBENSPITBEN0346SPITBENSPITURSPIROVSPIRBENSPITBEN0346SPITURENSRMTENSPIROVENSPIRBENSPITBENSPITBEN0346SPITURENSRMTENSPI	AddrBit 13Bit 13Bit 12Bit 11Bit 10Bit 9Bit 8Bit 7Bit 6Bit 5Bit 4Bit 3Bit 3Bit 20338SPIEN—SPISIDLDISSD0MODE32MODE16SMPCKESSENCKPMSTENDISSD1DISSC4MCLKEN0338AUDENSPISGNEXTIGNROVIGNTURAUDMON0URDTENAUDMOD1AUDMOD0FRMENFRMSYNCFRMPOLMSSENFRMSYPWFRMCNT20333VLENGTH<4:0	AddrBit 15Bit 14Bit 13Bit 12Bit 11Bit 10Bit 9Bit 8Bit 7Bit 6Bit 5Bit 4Bit 3Bit 3Bit 2Bit 10338SPIEN-SPISIDLDISSDOMODE32MODE16SMPCKESSENCKPMSTENDISSDIDISSCKMCLKENSPIFE0334AUDENSPISGNEXTIGNROVIGNTURAUDMONOURDTENAUDMOD1AUDMOD0FRMENFRMSYNCFRMPOLMSSENFRMSYPWFRMCNT2FRMCNT2FRMCNT10336VLENGTH<4.D>0337VLENGTH<4.D>0336VLENGTH<4.D>0336VLENGTH<4.D>0337SPITESPIRT0340RXELMSRXELMSRXELMSRXELMSRXELMSRXELMSSPITUESRMTSPIROVSPIRBESPITBESPITBE0342SPITUESRMTSPIROVENSPIRBESPITBESPITBESPITE0344SPITUESRMTSPIROVE	AddrBit 13Bit 13Bit 13Bit 12Bit 10Bit 9Bit 8Bit 7Bit 6Bit 5Bit 4Bit 3Bit 3Bit 2Bit 1Bit 00338SPIENSPISDLDISSD0MODE32MODE16SMPCKESSENCKPMSTENDISSD1DISSD1DISSCKMCLKENSPIFEENHBUF0334AUDENSPISGNEXTIGNROVIGNTURAUDMON0URDTENAUDMOD1AUDMOD0FRMENFRMSYNCFRMCD1MSSENFRMSYPWFRMCNT2FRMCNT2FRMCNT2FRMCNT1FRMCNT00336FRMSYNCFRMC01MSSENFRMSYPWFRMCNT2FRMCNT2FRMCNT1FRMCNT00336FRMCNT2

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-18 :	A/D CONVERTER REGISTER MAP
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Name Addr Bit 19 Bit 19 Bit 9 Bit 9 Bit 8 Bit 7 Bit 6 Bit 7 Bit 7 Bit 6 Bit 7 Bit 7 <th< th=""><th></th><th>10.</th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th></th<>		10.																	
ADC1BUF1 0202 ADC1BUF2 0204 ADC1BUF2 0204 ADC ADC ADC1BUF2 0206 ADD Data Buffer 3/Threshold for Channel 3 ADC ADC ADC1BUF5 0208 ADD Data Buffer 5/Threshold for Channel 4 XXX ADC1BUF6 0206 ADD Data Buffer 6/Threshold for Channel 6 XXX ADC1BUF6 0206 ADD Data Buffer 6/Threshold for Channel 6 XXX ADC1BUF6 0206 ADD Data Buffer 6/Threshold for Channel 6 XXX ADC1BUF6 0200 ADD Data Buffer 6/Threshold for Channel 0 in Windowed Compare mode XXX ADC1BUF7 0210 ADD Data Buffer 10/Threshold for Channel 1 in Windowed Compare mode ⁽¹⁾ XXX ADC1BUF10 0212 A/D Data Buffer 10/Threshold for Channel 1 in Windowed Compare mode ⁽¹⁾ XXX ADC1BUF10 0212 A/D Data Buffer 10/Threshold for Channel 1 in Windowed Compare mode ⁽¹⁾ XXX ADC1BUF10 0214 A/D Data Buffer 10/Threshold for Channel 1 in Windowed Compare mode ⁽¹⁾ XXX ADC1BUF12 0214 A/D Data Buffer 10/Threshold for Channel 1 in Windowed Compare mode ⁽¹⁾ XXX ADC1BUF12 0214 A/D Data Buffer 10/Threshold for Channel 1 in Win		Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADC18UF2 0204 AVC 18UF2 AVD Data Buffer 2/Threshold for Channel 3 xxxx ADC18UF4 0208 AVC Data Buffer 4/Threshold for Channel 3 xxxx ADC18UF4 0200 AVD Data Buffer 4/Threshold for Channel 5 xxxx ADC18UF6 0200 AVD Data Buffer 6/Threshold for Channel 6 xxxx ADC18UF7 0206 AVD Data Buffer 6/Threshold for Channel 0 in Windowed Compare mode xxxx ADC18UF7 0202 AVD Data Buffer 8/Threshold for Channel 0 in Windowed Compare mode xxxx ADC18UF8 0210 AVD Data Buffer 9/Threshold for Channel 0 in Windowed Compare mode ⁽¹⁾ xxxx ADC18UF10 0214 AVD Data Buffer 9/Threshold for Channel 0 in Windowed Compare mode ⁽¹⁾ xxxx ADC18UF10 0214 AVD Data Buffer 10/Threshold for Channel 10/Threshold for Channel 3 in Windowed Compare mode ⁽¹⁾ xxxx ADC18UF11 0216 AVD Data Buffer 10/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxxx ADC18UF11 0218 AVD Data Buffer 10/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxxx ADC18UF13 0214 AVD Data Buffer 10/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxxx ADC18UF13 0216 A	ADC1BUF0	0200						A/D	Data Buffer	0/Thresho	ld for Chan	nel 0							XXXX
ADC1BUF3 0206 ADC1BUF4 0208 ADC1BUF4 0208 ADC1BUF4 0208 ADC1BUF4 0208 ADD Data Buffer 4Threshold for Channel 4 xxxx ADC1BUF5 0200 ADD Data Buffer 5Threshold for Channel 5 Xxxx Xxxx ADC1BUF5 0200 ADD Data Buffer 6Threshold for Channel 6 Xxxx ADC1BUF7 0202 ADD Data Buffer 9Threshold for Channel 6 Xxxx ADC1BUF7 0202 ADD Data Buffer 9Threshold for Channel 9 Threshold for Channel 1 in Windowed Compare mode Xxxx ADC1BUF10 0214 ADD Data Buffer 10Threshold for Channel 9 Threshold for Channel 2 in Windowed Compare mode ⁽¹⁾ Xxxx ADC1BUF11 0216 ADD Data Buffer 10Threshold for Channel 1 In Windowed Compare mode ⁽¹⁾ Xxxx ADC1BUF12 0218 ADD Data Buffer 112Threshold for Channel 2 in Windowed Compare mode ⁽¹⁾ Xxxx ADC1BUF13 0210 ADD Data Buffer 12Threshold for Channel 2 in Windowed Compare mode ⁽¹⁾ Xxxx ADC1BUF13 0218 ADD Data Buffer 12Threshold for Channel 2 in Windowed Compare mode ⁽¹⁾ Xxxx ADC1BUF14 0216 ADD Data Buffer 12Threshold for Channel 2 in Windowed Compare mode ⁽¹⁾ Xxxx ADC1BUF14 <t< td=""><td>ADC1BUF1</td><td>0202</td><td></td><td></td><td></td><td></td><td></td><td>A/D</td><td>Data Buffer</td><td>1/Thresho</td><td>ld for Chan</td><td>nel 1</td><td></td><td></td><td></td><td></td><td></td><td></td><td>XXXX</td></t<>	ADC1BUF1	0202						A/D	Data Buffer	1/Thresho	ld for Chan	nel 1							XXXX
ADC18UF4 0208 ADC18UF5 20A ADC18UF5 20A ADC18UF5 ADC18UF1 ADC18UF1 ADC18UF1 ADC18UF10 ADC18UF10 ADC18UF10 ADC18UF10 ADC18UF10 ADC18UF11 ADC18UF11 ADC18UF11 ADC18UF12 Q18 ADC18UF11 ADC18UF13 ADC18UF14 ADC18U	ADC1BUF2	0204						A/D	Data Buffer	2/Thresho	ld for Chan	nel 2							XXXX
ADC18UF5 020A ADC18UF6 020C ADC18UF6 020C ADC18UF6 020C ADC18UF7 020E ADC18UF6 021C ADC18UF6 0210 ADD Data Buffer 10/Threshold for Channel 0 in Windowed Compare mode XXX XXX ADC18UF10 0214 ADD Data Buffer 11/Threshold for Channel 10/Threshold for Channel 1 in Windowed Compare mode ⁽¹⁾ XXX XXX ADC18UF12 0218 ADD Data Buffer 12/Threshold for Channel 12/Threshold for Channel 1 in Windowed Compare mode ⁽¹⁾ XXX ADC18UF13 021A ADD Data Buffer 12/Threshold for Channel 12/Threshold for Channel 3 in Windowed Compare mode ⁽¹⁾ XXX ADC18UF13 021A ADC18UF13 021A ADC18UF13 SSSC2 SSSC1 SSSC0 - ASAM SAMP DONE	ADC1BUF3	0206						A/D	Data Buffer	3/Thresho	ld for Chan	nel 3							XXXX
ADC18UF6 020C ADC18UF7 020E ADC18UF7 020E ADC18UF7 020E ADC18UF7 020E ADC18UF7 021E ADC18UF7	ADC1BUF4	0208						A/D	Data Buffer	4/Thresho	ld for Chan	nel 4							XXXX
ADC18UF7 020E ADC18UF8 0210 ADC18UF8 0210 ADC18UF9 0210 ADC18UF9 0210 ADC18UF9 0210 ADC18UF9 0212 ADC18UF9 0212 ADC18UF9 0212 ADC18UF9 0212 ADD Data Buffer 3/Threshold for Channel 3/Threshold for Channel 1/Threshold for Channel 10/Threshold for Channel 3 in Windowed Compare mode ⁽¹⁾ xxx ADC18UF10 0216 ADD Data Buffer 10/Threshold for Channel 10/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxx ADC18UF12 0218 A/D Data Buffer 12/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxx ADC18UF13 0214 A/D Data Buffer 12/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxx ADC18UF14 0210 A/D Data Buffer 12/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxx ADC18UF14 0212 ADON ADD AB AMD Data Buffer 12/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxx ADC18UF14 0216 C116 ADON	ADC1BUF5	020A						A/D	Data Buffer	5/Thresho	ld for Chan	nel 5							XXXX
ADC18UF8 0210 A/D Data Buffer 8/Threshold for Channel 9/Threshold for Channel 0 in Windowed Compare mode xxxx ADC18UF9 0212 A/D Data Buffer 9/Threshold for Channel 1 in Windowed Compare mode xxxx ADC18UF10 0214 A/D Data Buffer 10/Threshold for Channel 1 in/Threshold for Channel 2 in Windowed Compare mode ⁽¹⁾ xxxx ADC18UF11 0216 A/D Data Buffer 11/Threshold for Channel 1 in/Threshold for Channel 3 in Windowed Compare mode ⁽¹⁾ xxxx ADC18UF12 0218 A/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxxx ADC18UF13 021A X/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxxx ADC18UF13 021A X/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxxx ADC18UF13 021A X/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 5 to X/D Data Buffer 13 XXX ADC18UF14 021C X/D CAD X/D DAMAM MAR MODE12 FORM1 FORM0 SSRC3 SSRC2 SSRC1 SSRC0 ASAM SAMP DONE 000 AD1CON1 0222 PVCFG1 PVCFG0 OFFCAL BUFREGEN	ADC1BUF6	020C						A/D	Data Buffer	6/Thresho	ld for Chan	nel 6							XXXX
ADC18UF9 0212 A/D Data Buffer 9/Threshold for Channel 9/Threshold for Channel 1 in Windowed Compare mode xxxx ADC18UF10 0214 A/D Data Buffer 10/Threshold for Channel 10/Threshold for Channel 2 in Windowed Compare mode ⁽¹⁾ xxxx ADC18UF10 0216 A/D Data Buffer 11/Threshold for Channel 10/Threshold for Channel 3 in Windowed Compare mode ⁽¹⁾ xxxx ADC18UF12 0218 A/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxxx ADC18UF13 021A A/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxxx ADC18UF14 021C A/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxxx ADC18UF14 021C A/D Data Buffer 13 XXX XXXX ADC18UF15 021E A/D Data Buffer 14 XXXX ADC10N1 0220 ADON A/D AND MARN MODE12 FORM1 FORM0 SSRC3 SSRC1 SSRC0 ASAM SAMP DONE 000 AD1C0N2 0222 PVCFG1 PVCFG0 NVCFG0 OFFCAL BUFREGEN CSCNA - - BUFS SMPI4 SMPI	ADC1BUF7	020E		A/D Data Buffer 7/Threshold for Channel 7											XXXX				
ADC1BUF10 0214 ADD Data Buffer 10/Threshold for Channel 10/Threshold for Channel 2 in Windowed Compare mode ⁽¹⁾ xxxx ADC1BUF11 0216 A/D Data Buffer 11/Threshold for Channel 11/Threshold for Channel 3 in Windowed Compare mode ⁽¹⁾ xxxx ADC1BUF12 0218 A/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxxx ADC1BUF13 021A A/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxxx ADC1BUF13 021A A/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxxx ADC1BUF13 021A A/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxxx ADC1BUF14 021C A/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxx ADC1BUF15 021E A/D Data Buffer 12/Threshold for Channel 12 Threshold for Channel 5 xxx AD1CON1 0220 ADON ADSID DMABM MODE12 FORM1 FORM0 SSRC3 SSRC1 SSRC1 SMPI2 SMPI1 SMPI0 BUFM ALTS 000 AD1CON2 0222 PVCFG1 PVCFG0 NVCFG0	ADC1BUF8	0210				A/D	Data Buffer 8/	Threshold for	Channel 8/	Threshold	for Channe	0 in Windo	wed Comp	are mode					XXXX
ADC1BUF11 0216 ADD Data Buffer 11/Threshold for Channel 11/Threshold for Channel 3 in Windowed Compare mode ⁽¹⁾ xxxx ADC1BUF12 0218 A/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxxx ADC1BUF13 021A A/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxxx ADC1BUF14 021C A/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxx ADC1BUF14 021C A/D Data Buffer 13 XXX ADC1BUF15 021E A/D Data Buffer 15 XXX AD1CON1 0220 ADON ADSID DMABM DMAEN MODE12 FORM1 FORM0 SSRC3 SSRC1 SSRC0 ASAM SAMP DONE 000 AD1CON1 0220 ADON ADSID DMABM DMAEN MODE12 FORM1 FORM0 SSRC3 SSRC1 SSRC0 ASAM MPI0 BUFM ALTS 000 AD1CON3 0224 ADCC EXTSAM PUMPEN SAMC3 SAMC2 SAMC1 SAMC0 ADCS5 ADCS5 ADCS3 ADCS2 <	ADC1BUF9	0212				A/D	Data Buffer 9/	Threshold for	Channel 9/	Threshold	for Channe	1 in Windo	wed Comp	are mode					xxxx
ADC18UF12 0218 A/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 4 in Windowed Compare mode ⁽¹⁾ xxxx ADC18UF13 021A	ADC1BUF10	0214				A/D Da	ata Buffer 10/T	hreshold for C	Channel 10/	Threshold	for Channe	l 2 in Windo	owed Comp	are mode ⁽¹)				xxxx
ADC1BUF13 021A	ADC1BUF11	0216				A/D Da	ata Buffer 11/T	hreshold for (Channel 11/	Threshold	for Channe	3 in Windo	wed Comp	are mode ⁽¹)				xxxx
ADC1BUF14 021C VACUAL	ADC1BUF12	0218				A/D Da	ata Buffer 12/T	hreshold for C	Channel 12/	Threshold	for Channe	l 4 in Windo	owed Comp	are mode ⁽¹)				xxxx
ADC1BUF15021EO210ADON—ADSIDLDMABMDMAENMODE12FORM1FORM0SSRC3SSRC2SSRC1SSRC0—ASAMSAMPDONE000AD1CON10222PVCFG1PVCFG0NVCFG0OFFCALBUFREGENCSCNA——BUFSSMPI4SMPI3SMPI2SMP11SMP10BUFMALTS000AD1CON20222PVCFG1PVCFG0NVCFG0OFFCALBUFREGENCSCNA———BUFSSMP14SMP13SMP12SMP10BUFMALTS000AD1CON30224ADRCEXTSAMPUMPENSAMC4SAMC3SAMC2SAMC1SAMC0ADC57ADC56ADC55ADC54ADC53ADC52ADC51ADC50000AD1CN30228CH0NB2CH0NB1CH0SB3CH0SB2CH0SB1CH0SB0CH0NA2CH0NA1CH0NA0CH0SA4CH0SA3CH0SA2CH0SA0000AD1CSSL022C—————————————000AD1CON4022E—————————————000AD1CON4022E————————————000AD1CON4022E————————————…000 <td>ADC1BUF13</td> <td>021A</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>A/D</td> <td>Data Buffe</td> <td>er 13</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>xxxx</td>	ADC1BUF13	021A							A/D	Data Buffe	er 13								xxxx
AD1CON1 0220 ADON — ADSIDL DMABM DMAEN MODE12 FORM1 FORM0 SSRC3 SSRC1 SSRC0 — ASAM SAMP DONE 000 AD1CON2 0222 PVCFG1 PVCFG0 NVCFG0 OFFCAL BUFREGEN CSCNA — — BUFS SMPI4 SMPI3 SMPI2 SMPI1 SMP0 BUFM ALTS 000 AD1CON3 0224 ADRC EXTSAM PUMPEN SAMC4 SAMC3 SAMC2 SAMC1 SAMC0 ADCS7 ADCS6 ADCS5 ADCS4 ADCS3 ADCS2 ADCS1 ADCS0 000 AD1CHS 0228 CH0NB1 CH0NB0 CH0SB3 CH0SB3 CH0SB1 CH0SB0 CH0NA2 CH0NA2 CH0NA1 CH0NA3 CH0SA3 CH0SA0 CH0NA2 CH0NA1 CH0NA3 CH0SA3 CH0SB0 CH0NA2 CH0NA1 CH0NA3 CH0SA3 CH0SA0 CH0NA2 CH0NA1 CH0NA3 CH0SA3 CH0SA0 CH0NA3 CH0SA3 CH0SA1 CH0NA0 CH0NA3 CH0SA3 CH0SA0 CH0NA1 <td>ADC1BUF14</td> <td>021C</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>A/D</td> <td>Data Buffe</td> <td>er 14</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>xxxx</td>	ADC1BUF14	021C							A/D	Data Buffe	er 14								xxxx
AD1CON20222PVCFG1PVCFG0NVCFG0OFFCALBUFREGENCSCNA——BUFSSMPI4SMPI3SMPI2SMPI1SMPI0BUFMALTS000AD1CON30224ADRCEXTSAMPUMPENSAMC4SAMC3SAMC2SAMC1SAMC0ADCS7ADCS6ADCS5ADCS4ADCS3ADCS2ADCS1ADCS0000AD1CHS0228CH0NB2CH0NB1CH0NB0CH0SB4CH0SB3CH0SB2CH0SB1CH0SB0CH0NA2CH0NA1CH0NA0CH0SA4CH0SA3CH0SA2CH0SA0000AD1CSH022C——CSS<31:27>——————————000AD1CON4022E—————————————000AD1CON50230ASENLPENCTMREQBGREQ——ASINT1ASINT0—————000AD1CTMENL0238————————————000AD1CON50230ASENLPENCTMREQBGREQ——ASINT1ASINT0——————000AD1CON50238————————————000AD1CON50238ASEN <td< td=""><td>ADC1BUF15</td><td>021E</td><td></td><td></td><td></td><td></td><td></td><td></td><td>A/D</td><td>Data Buffe</td><td>r 15</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>XXXX</td></td<>	ADC1BUF15	021E							A/D	Data Buffe	r 15								XXXX
AD1CON3 0224 ADRC EXTSAM PUMPEN SAMC4 SAMC3 SAMC2 SAMC1 SAMC0 ADCS7 ADCS6 ADCS5 ADCS4 ADCS3 ADCS2 ADCS1 ADCS0 000 AD1CHS 0228 CH0NB2 CH0NB1 CH0NB0 CH0SB4 CH0SB3 CH0SB2 CH0SB1 CH0SB0 CH0NA2 CH0NA1 CH0NA0 CH0SA3 CH0SA2 CH0SA0 000 AD1CSSH 0220 C CSS<31:27> — — — — — — — — — — — 000 ADCS3 ADCS2 ADCS1 ADCS0 000 AD1CSSH 0220 — CSS<31:27> — — — — — — — — — — — 000 AD1CS1 020 … </td <td>AD1CON1</td> <td>0220</td> <td>ADON</td> <td>—</td> <td>ADSIDL</td> <td>DMABM</td> <td>DMAEN</td> <td>MODE12</td> <td>FORM1</td> <td>FORM0</td> <td>SSRC3</td> <td>SSRC2</td> <td>SSRC1</td> <td>SSRC0</td> <td>_</td> <td>ASAM</td> <td>SAMP</td> <td>DONE</td> <td>0000</td>	AD1CON1	0220	ADON	—	ADSIDL	DMABM	DMAEN	MODE12	FORM1	FORM0	SSRC3	SSRC2	SSRC1	SSRC0	_	ASAM	SAMP	DONE	0000
AD1CHS 0228 CH0NB2 CH0NB1 CH0NB0 CH0SB4 CH0SB3 CH0SB2 CH0SB1 CH0SB0 CH0NA2 CH0NA1 CH0NA0 CH0SA4 CH0SA3 CH0SA2 CH0SA1 CH0SA3 CH0SA3 CH0SA4 CH0SA3 CH0SA3 CH0SA4 CH0SA4 CH0SA3 CH0SA4	AD1CON2	0222	PVCFG1	PVCFG0	NVCFG0	OFFCAL	BUFREGEN	CSCNA		_	BUFS	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS	0000
AD1CSSH 022A CSS<31:27> - 000 AD1CSSL 022C - - - - - - - - - - 000 AD1CON4 022E - - - - - - - - DMABL<2:0> 000 AD1CON5 0230 ASEN LPEN CTMREQ BGREQ - - - - - - - DMABL<2:0> 000 AD1CHITL 0234 - D000 D00	AD1CON3	0224	ADRC	EXTSAM	PUMPEN	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0	ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	0000
AD1CSSL 022C CSS<14:0>(1) <th< td=""><td>AD1CHS</td><td>0228</td><td>CH0NB2</td><td>CH0NB1</td><td>CH0NB0</td><td>CH0SB4</td><td>CH0SB3</td><td>CH0SB2</td><td>CH0SB1</td><td>CH0SB0</td><td>CH0NA2</td><td>CH0NA1</td><td>CH0NA0</td><td>CH0SA4</td><td>CH0SA3</td><td>CH0SA2</td><td>CH0SA1</td><td>CH0SA0</td><td>0000</td></th<>	AD1CHS	0228	CH0NB2	CH0NB1	CH0NB0	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0	CH0NA2	CH0NA1	CH0NA0	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0	0000
AD1CON4 022E	AD1CSSH	022A			CSS<31:2	7>		_	_	—		_	—			—	—	—	0000
AD1CON5 0230 ASEN LPEN CTMREQ BGREQ — ASINT1 ASINT0 — — — — WM1 WM0 CM1 CM0 000 AD1CHITL 0234 — — — — ASINT1 ASINT0 — — — — WM1 WM0 CM1 CM0 000 AD1CHITL 0234 — — — — — — — — W00 CM1 CM0 000 AD1CTMENL 0238 — — — — — CTMEN CTMEN CTMEN USDA	AD1CSSL	022C	—							CSS<1	14:0> ⁽¹⁾								0000
AD1CHITL 0234 CHH<12:0>(1) 000 AD1CTMENL 0238 CTMEN<12:0>(1) 000	AD1CON4	022E	—																
AD1CTMENL 0238 CTMEN<12:0> ⁽¹⁾		0230	ASEN	LPEN	CTMREQ	BGREQ	_	_	ASINT1	ASINT0	—	—	—	—	WM1	WM0	CM1	CM0	0000
	AD1CHITL	0234	—	– – – CHH<12:0> ⁽¹⁾ 0000											0000				
AD1DMBUF 023A A/D Conversion Data Buffer (Extended Buffer mode) xxx	AD1CTMENL	0238	—	—	—						CTMEN	<12:0> ⁽¹⁾							0000
	AD1DMBUF	023A						A/D Conv	ersion Data	a Buffer (Ex	tended Buf	fer mode)							XXXX

Legend: — = unimplemented, read as '0'; x = unknown value on Reset. Reset values are shown in hexadecimal.

Note 1: The CSS<12:10>, CHH<12:10> and CTMEN<12:10> bits are unimplemented in 28-pin devices, read as '0'.

REGISTER 8-7: IFS2: INTERRUPT FLAG STATUS REGISTER 2 (CONTINUED)

- bit 1 SPI2TXIF: SPI2 Transmit Interrupt Flag Status bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 0 SPI2IF: SPI2 General Interrupt Flag Status bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred

11.4.6 PERIPHERAL PIN SELECT REGISTERS

The PIC24FJ128GA204 family of devices implements a total of 32 registers for remappable peripheral configuration:

- Input Remappable Peripheral Registers (19)
- Output Remappable Peripheral Registers (13)

Note: Input and output register values can only be changed if IOLOCK (OSCCON<6>) = 0. See Section 11.4.4.1 "Control Register Lock" for a specific command sequence.

REGISTER 11-4: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	INT1R5	INT1R4	INT1R3	INT1R2	INT1R1	INT1R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	OCTRIG1R5	OCTRIG1R4	OCTRIG1R3	OCTRIG1R2	OCTRIG1R1	OCTRIG1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	t, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13-8	INT1R<5:0>: Assign External Interrupt 1 (INT1) to Corresponding RPn or RPIn Pin bits
bit 7-6	Unimplemented: Read as '0'
bit 5-0	OCTRIG1R<5:0>: Assign Output Compare Trigger 1 to Corresponding RPn or RPIn Pin bits

REGISTER 11-5: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	INT3R5	INT3R4	INT3R3	INT3R2	INT3R1	INT3R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	INT2R5	INT2R4	INT2R3	INT2R2	INT2R1	INT2R0
bit 7							bit 0

Legend:						
R = Readab	ole bit	W = Writable bit	U = Unimplemented bit,	, read as '0'		
-n = Value at POR		'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		
bit 15-14	Unimple	Unimplemented: Read as '0'				
bit 13-8	INT3R<5	:0>: Assign External Interrup	ot 3 (INT3) to Corresponding R	Pn or RPIn Pin bits		
bit 7-6	Unimple	Unimplemented: Read as '0'				
bit 5-0		• Accien External Interrun	ot 2 (INT2) to Corresponding R	Dn or DDIn Din hite		

REGISTER 11-25: RPOR2: PERIPHERAL PIN SELECT OUTPUT REGISTER 2

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	—			RP5R	<5:0>		
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	_	—	—		—
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable I	oit	U = Unimplem	nented bit, read	d as '0'	
-n = Value a	It POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15-14	Unimpleme	nted: Read as 'o)'				
bit 13-8	RP5R<5:0>:	RP5 Output Pir	Mapping bits	3			
	Peripheral O	utput Number n	is assigned to	o pin, RP5 (see	Table 11-4 for	peripheral funct	tion numbers).

bit 7-0 Unimplemented: Read as '0'

REGISTER 11-26: RPOR3: PERIPHERAL PIN SELECT OUTPUT REGISTER 3

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP7R5	RP7R4	RP7R3	RP7R2	RP7R1	RP7R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP6R5	RP6R4	RP6R3	RP6R2	RP6R1	RP6R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 Unimplemented: Read as '0'

bit 13-8 **RP7R<5:0>:** RP7 Output Pin Mapping bits

Peripheral Output Number n is assigned to pin, RP7 (see Table 11-4 for peripheral function numbers).

bit 7-6 Unimplemented: Read as '0'

bit 5-0 **RP6R<5:0>:** RP6 Output Pin Mapping bits Peripheral Output Number n is assigned to pin, RP6 (see Table 11-4 for peripheral function numbers).

REGISTER 11-33: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10⁽¹⁾

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RP21R5	RP21R4	RP21R3	RP21R2	RP21R1	RP21R0
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RP20R5	RP20R4	RP20R3	RP20R2	RP20R1	RP20R0
bit 7							bit 0
Legend:							
R = Readabl	e bit	W = Writable	bit	U = Unimplemented bit, read as '0'			
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15-14	Unimpleme	nted: Read as '	0'				
bit 13-8	RP21R<5:0	>: RP21 Output	Pin Mapping b	oits			
	Peripheral C	utput Number n	is assigned to	pin, RP21 (see	Table 11-4 for	peripheral func	tion numbers).

- bit 7-6 Unimplemented: Read as '0'
- bit 5-0 **RP20R<5:0>:** RP20 Output Pin Mapping bits Peripheral Output Number n is assigned to pin, RP20 (see Table 11-4 for peripheral function numbers).

Note 1: These pins are not available in 28-pin devices.

REGISTER 11-34: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11⁽¹⁾

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RP23R5	RP23R4	RP23R3	RP23R2	RP23R1	RP23R0
bit 15				•			bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP22R5	RP22R4	RP22R3	RP22R2	RP22R1	RP22R0
bit 7							bit 0
l edenq.							

Legena:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 Unimplemented: Read as '0'

bit 13-8**RP23R<5:0>:** RP23 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP23 (see Table 11-4 for peripheral function numbers).bit 7-6**Unimplemented:** Read as '0'

bit 5-0 **RP22R<5:0>:** RP22 Output Pin Mapping bits Peripheral Output Number n is assigned to pin, RP22 (see Table 11-4 for peripheral function numbers).

Note 1: These pins are not available in 28-pin devices.

REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)

- bit 4-0 SYNCSEL<4:0>: Synchronization/Trigger Source Selection bits
 - 1111x = Reserved
 - 11101 = Reserved
 - 11100 = CTMU⁽¹⁾
 - 11011 = A/D⁽¹⁾
 - $11010 = \text{Comparator 3}^{(1)}$
 - 11001 = Comparator 2⁽¹⁾
 - 11000 = Comparator 1⁽¹⁾
 - 10111 = Reserved
 - 10110 = Reserved
 - 10101 = Input Capture $6^{(2)}$
 - 10100 = Input Capture 5⁽²⁾ 10011 = Input Capture 4⁽²⁾
 - $10011 = \text{Input Capture 4}^{(1)}$ $10010 = \text{Input Capture 3}^{(2)}$
 - 10010 = Input Capture 3(*)10001 = Input Capture 2(2)
 - $10001 = \text{Input Capture 2}^{(7)}$ $10000 = \text{Input Capture 1}^{(2)}$
 - 01111 = Timer5
 - 01110 = Timer3
 - 01101 = Timer3
 - 01100 = Timer3
 - 01011 = Timer1
 - 01010 = **Reserved**
 - 01001 = Reserved
 - 01000 = Reserved
 - 00111 = **Reserved**
 - 00110 = Output Compare 6
 - 00101 = Output Compare 5
 - 00100 = Output Compare 4
 - 00011 = Output Compare 3
 - 00010 = Output Compare 2
 - 00001 = Output Compare 1
 - 00000 = Not synchronized to any other module
- Note 1: Use these inputs as trigger sources only and never as sync sources.
 - 2: Never use an ICx module as its own trigger source by selecting this mode.

18.1 UARTx Baud Rate Generator (BRG)

The UARTx module includes a dedicated, 16-bit Baud Rate Generator. The UxBRG register controls the period of a free-running, 16-bit timer. Equation 18-1 shows the formula for computation of the baud rate when BRGH = 0.

EQUATION 18-1: UARTx BAUD RATE WITH BRGH = $0^{(1,2)}$

$$Baud Rate = \frac{FCY}{16 \cdot (UxBRG + 1)}$$
$$UxBRG = \frac{FCY}{16 \cdot Baud Rate} - 1$$
Note 1: FCY denotes the instruction cycle clock frequency (FOSC/2).
2: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

Example 18-1 shows the calculation of the baud rate error for the following conditions:

- Fcy = 4 MHz
- Desired Baud Rate = 9600

The maximum baud rate (BRGH = 0) possible is FCY/16 (for UxBRG = 0) and the minimum baud rate possible is FCY/(16 * 65536).

Equation 18-2 shows the formula for computation of the baud rate when BRGH = 1.

EQUATION 18-2: UARTX BAUD RATE WITH BRGH = $1^{(1,2)}$

$$Baud Rate = \frac{FCY}{4 \cdot (UxBRG + 1)}$$
$$UxBRG = \frac{FCY}{4 \cdot Baud Rate} - 1$$

- **Note 1:** FCY denotes the instruction cycle clock frequency.
 - **2:** Based on FCY = FOSC/2; Doze mode and PLL are disabled.

The maximum baud rate (BRGH = 1) possible is FcY/4 (for UxBRG = 0) and the minimum baud rate possible is FcY/(4 * 65536).

Writing a new value to the UxBRG register causes the BRG timer to be reset (cleared). This ensures the BRG does not wait for a timer overflow before generating the new baud rate.

EXAMPLE 18-1: BAUD RATE ERROR CALCULATION (BRGH = 0)⁽¹⁾

Desired Baud Rate = FCY/(16 (UxBRG + 1))Solving for UxBRG Value: **UxBRG** = ((FCY/Desired Baud Rate)/16) - 1**UxBRG** = ((400000/9600)/16) - 1UxBRG = 25 Calculated Baud Rate = 4000000/(16(25+1))= 9615 Error = (Calculated Baud Rate – Desired Baud Rate) Desired Baud Rate = (9615 - 9600)/9600 = 0.16% Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

REGISTER 20-2: PMCON2: EPMP CONTROL REGISTER 2

R-0, HSC	U-0	R/C-0, HS	R/C-0, HS	U-0	U-0	U-0	U-0
PMPBUSY	_	ERROR	TIMEOUT	—	—	—	—
bit 15							bit 8

| R/W-0 |
|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| RADDR23 ⁽¹⁾ | RADDR22 ⁽¹⁾ | RADDR21 ⁽¹⁾ | RADDR20 ⁽¹⁾ | RADDR19 ⁽¹⁾ | RADDR18 ⁽¹⁾ | RADDR17 ⁽¹⁾ | RADDR16 ⁽¹⁾ |
| bit 7 | | | | | | | bit 0 |

Legend:	HS = Hardware Settable bit	IS = Hardware Settable bit HSC = Hardware Settable/Clearable bit		
R = Readable bit W = Writable bit		U = Unimplemented, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	C = Clearable bit	

bit 15 **PMPBUSY:** EPMP Busy bit (Master mode only)

- 1 = Port is busy
 - 0 = Port is not busy
- bit 14 Unimplemented: Read as '0'
- bit 13 ERROR: EPMP Error bit
 - 1 = Transaction error (illegal transaction was requested)
 - 0 = Transaction completed successfully
- bit 12 **TIMEOUT:** EPMP Time-out bit
 - 1 = Transaction timed out
 - 0 = Transaction completed successfully
- bit 11-8 Unimplemented: Read as '0'
- bit 7-0 RADDR<23:16>: EPMP Reserved Address Space bits⁽¹⁾
- **Note 1:** If RADDR<23:16> = 00000000, then the last EDS address for Chip Select 2 will be FFFFFh.

21.3.2 RTCVAL REGISTER MAPPINGS

REGISTER 21-4: YEAR: YEAR VALUE REGISTER⁽¹⁾

| U-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |
| | | | | | | | |
| R/W-x |
| YRTEN3 | YRTEN2 | YRTEN2 | YRTEN1 | YRONE3 | YRONE2 | YRONE1 | YRONE0 |
| bit 7 | | | | | | | bit 0 |

Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 15-8 Unimplemented: Read as '0'

bit 7-4 **YRTEN<3:0>:** Binary Coded Decimal Value of Year's Tens Digit bits Contains a value from 0 to 9.

bit 3-0 **YRONE<3:0>:** Binary Coded Decimal Value of Year's Ones Digit bits Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 21-5: MTHDY: MONTH AND DAY VALUE REGISTER⁽¹⁾

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13	Unimplemented: Read as '0'
bit 12	MTHTEN0: Binary Coded Decimal Value of Month's Tens Digit bit Contains a value of '0' or '1'.
bit 11-8	MTHONE<3:0>: Binary Coded Decimal Value of Month's Ones Digit bits Contains a value from 0 to 9.
bit 7-6	Unimplemented: Read as '0'
bit 5-4	DAYTEN<1:0>: Binary Coded Decimal Value of Day's Tens Digit bits Contains a value from 0 to 3.
bit 3-0	DAYONE<3:0>: Binary Coded Decimal Value of Day's Ones Digit bits Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 22-5: CFGPAGE: SECURE ARRAY CONFIGURATION BITS (OTP PAGE 0) REGISTER

r-x	R/PO-x	U-x	U-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x
—	TSTPGM ⁽¹⁾	—	—	KEY4TYPE1	KEY4TYPE0	KEY3TYPE1	KEY3TYPE0
bit 31							bit 24

R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	
KEY2TYPE1	KEY2TYPE0	KEY1TYPE1	KEY1TYPE0	SKEYEN	LKYSRC7	LKYSRC6	LKYSRC5	
bit 23 bit 1								

R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x
LKYSRC4	LKYSRC3	LKYSRC2	LKYSRC1	LKYSRC0	SRCLCK	WRLOCK8	WRLOCK7
bit 15							bit 8

R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	R/PO-x	
WRLOCK6	WRLOCK5	WRLOCK74	WRLOCK3	WRLOCK2	WRLOCK1	WRLOCK0	SWKYDIS	
bit 7 bit 0								

Legend:	r = Reserved bit				
R = Readable bit	PO = Program Once bit	U = Unimplemented bit, read	d as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

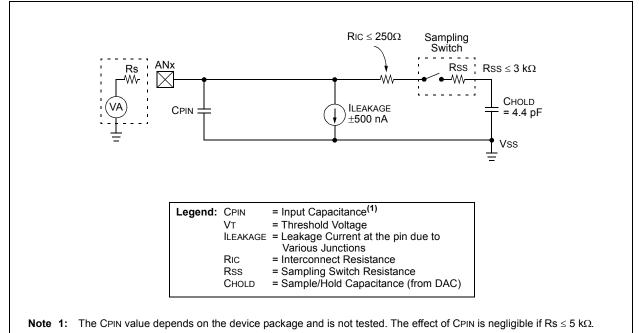
bit 31	Reserved: Do not modify
bit 30	TSTPGM: Customer Program Test bit ⁽¹⁾
	 1 = CFGPAGE has been programmed 0 = CFGPAGE has not been programmed
bit 29-28	Unimplemented: Read as '0'
bit 27-26	KEY4TYPE<1:0>: Key Type for OTP Pages 7 and 8 bits
	 00 = Keys in these pages are for DES/2DES operations only 01 = Keys in these pages are for 3DES operations only 10 = Keys in these pages are for 128-bit AES operations only 11 = Keys in these pages are for 192-bit/256-bit AES operations only
bit 25-24	KEY3TYPE<1:0>: Key Type for OTP Pages 5 and 6 bits
	 00 = Keys in these pages are for DES/2DES operations only 01 = Keys in these pages are for 3DES operations only 10 = Keys in these pages are for 128-bit AES operations only 11 = Keys in these pages are for 192-bit/256-bit AES operations only
bit 23-22	KEY2TYPE<1:0>: Key Type for OTP Pages 3 and 4 bits
	 00 = Keys in these pages are for DES/2DES operations only 01 = Keys in these pages are for 3DES operations only 10 = Keys in these pages are for 128-bit AES operations only 11 = Keys in these pages are for 192-bit/256-bit AES operations only
bit 21-20	KEY1TYPE<1:0>: Key Type for OTP Pages 1 and 2 bits
	 00 = Keys in these pages are for DES/2DES operations only 01 = Keys in these pages are for 3DES operations only 10 = Keys in these pages are for 128-bit AES operations only 11 = Keys in these pages are for 192-bit/256-bit AES operations only
Note 1	This hit's state is mirrored by the PGMTST hit (CRYOTP<7>)

This bit's state is mirrored by the PGMTST bit (CRYOTP<7>). NOTE 1:

REGISTER 2	23-1: CR0	CCON1: CRC	CONTROL RE	GISTER 1	
		-			

R/W-0	U-0	R/W-0	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	
CRCEN	_	CSIDL	VWORD4	VWORD3	VWORD2	VWORD1	VWORD0	
bit 15			•	- -			bit 8	
R-0, HSC	R-1, HSC	R/W-0	R/W-0, HC	R/W-0	U-0	U-0	U-0	
CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN		<u> </u>	—	
bit 7							bit 0	
Legend:		HC = Hardware			are Settable/C			
R = Readab		W = Writable b	it	•	nented bit, read			
-n = Value a	It POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	iown	
bit 15	bit 15 CRCEN: CRC Enable bit 1 = Enables module 0 = Disables module; all state machines, pointers and CRCWDAT/CRCDATH registers are reset; other SFRs are NOT reset							
bit 14	Unimpleme	ented: Read as '	0'					
bit 13	CSIDL: CR	C Stop in Idle Mo	ode bit					
		inues module op es module opera			e mode			
bit 12-8	VWORD<4:	0>: Pointer Valu	e bits					
	Indicates the when PLEN	e number of valid $<4:0> \le 7.$	I words in the FI	FO. Has a max	imum value of	8 when PLEN<	:4:0> ≥ 7 or 16	
bit 7	CRCFUL: F	IFO Full bit						
	1 = FIFO is							
	0 = FIFO is							
bit 6		CRC FIFO Empty	bit					
	1 = FIFO is 0 = FIFO is							
bit 5		CRC Interrupt Se	election bit					
		t on FIFO is emp		d of data is still	shifting throug	h the CRC		
	0 = Interrup	t on shift is comp	lete and results	are ready				
bit 4	CRCGO: St							
		RC serial shifter	od off					
bit 3		Data Shift Directi						
		ord is shifted into		na with the LSh	(little-endian)			
		ord is shifted into		•	, ,			
bit 2-0	Unimpleme	ented: Read as '	0'					

FIGURE 24-3: 10-BIT A/D CONVERTER ANALOG INPUT MODEL



EQUATION 24-1: A/D CONVERSION CLOCK PERIOD

$$T_{AD} = T_{CY} \left(ADCS + 1 \right)$$

$$ADCS = \frac{T_{AD}}{T_{CY}} - 1$$

Note: Based on TCY = 2/FOSC; Doze mode and PLL are disabled.

REGISTER 29-5: DEVID: DEVICE ID REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
_	—	—	—	—	—	—	—
bit 23							bit 16
R	R	R	R	R	R	R	R
FAMID7	FAMID6	FAMID5	FAMID4	FAMID3	FAMID2	FAMID1	FAMID0
bit 15	bit 15 bit 8						
R	R	R	R	R	R	R	R
DEV7	DEV6	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0
bit 7 bit 0							
Legend: F	Legend: R = Readable bit U = Unimplemented bit						
bit 23-16	Unimplement	ted: Read as 'a	L'				

- bit 15-8FAMID<7:0>: Device Family Identifier bits01001100 = PIC24FJ128GA204 familybit 7-0DEV<7:0>: Individual Device Identifier bits
 - 0101 0000 = PIC24FJ64GA202
 - 0101 0010 = PIC24FJ128GA202
 - 0101 0001 = PIC24FJ64GA204
 - 0101 0011 = PIC24FJ128GA204

REGISTER 29-6: DEVREV: DEVICE REVISION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	R	R	R	R
—	—	—	—	REV<3:0>			
bit 7			•				bit 0
Legend: R	= Readable bit			U = Unimplem	nented bit		

bit 23-4 Unimplemented: Read as '0'

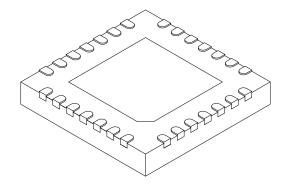
bit 3-0 **REV<3:0>:** Device Revision Identifier bits

Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
TBLRDH	TBLRDH	Ws,Wd	Read Prog<23:16> to Wd<7:0>	1	2	None
TBLRDL	TBLRDL	Ws,Wd	Read Prog<15:0> to Wd	1	2	None
TBLWTH	TBLWTH	Ws,Wd	Write Ws<7:0> to Prog<23:16>	1	2	None
TBLWTL	TBLWTL	Ws,Wd	Write Ws to Prog<15:0>	1	2	None
ULNK	ULNK		Unlink Frame Pointer	1	1	None
XOR	XOR	f	f = f .XOR. WREG	1	1	N, Z
	XOR	f,WREG	WREG = f .XOR. WREG	1	1	N, Z
	XOR	#lit10,Wn	Wd = lit10 .XOR. Wd	1	1	N, Z
	XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1	N, Z
	XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1	N, Z
ZE	ZE	Ws,Wnd	Wnd = Zero-Extend Ws	1	1	C, Z, N

TABLE 31-2: INSTRUCTION SET OVERVIEW (CONTINUED)

28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	Ν	/ILLIMETER	S		
Dimensior	Limits	MIN	NOM	MAX		
Number of Pins	Ν		28			
Pitch	е		0.65 BSC			
Overall Height	А	0.80	0.90	1.00		
Standoff	A1	0.00	0.02	0.05		
Terminal Thickness	A3		0.20 REF			
Overall Width	Е		6.00 BSC			
Exposed Pad Width	E2	3.65	3.70	4.70		
Overall Length	D		6.00 BSC			
Exposed Pad Length	D2	3.65	3.70	4.70		
Terminal Width	b	0.23	0.30	0.35		
Terminal Length	L	0.30	0.40	0.50		
Terminal-to-Exposed Pad	K	0.20	-	-		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated

3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-124C Sheet 2 of 2

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Product Group Pin Count Tape and Reel FI Temperature Rar Package		 Examples: a) PIC24F J128GA202-I/MM: PIC24F device with 128-Kbyte program memory, 8-Kbyte data memory, 28-pin, Industrial temp., QFN-S package. b) PIC24F,128GA204-I/PT: PIC24F device with 128-Kbyte program memory, 8-Kbyte data memory, 44-pin, Industrial temp., TQFP package.
Architecture	24 = 16-bit modified Harvard without DSP	
Flash Memory Family	FJ = Flash program memory	
Product Group	GA2 = General purpose microcontrollers	
Pin Count	02 = 28-pin 04 = 44-pin	
Temperature Range	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)	
Package	MM = 28-lead (6x6x0.9 mm) QFN-S (Quad Flat) ML = 44-lead (8x8 mm) QFN (Quad Flat) PT = 44-lead (10x10x1 mm) TQFP (Thin Quad Flatpack) SO = 28-lead (7.50 mm wide) SOIC (Small Outline) SP = 28-lead (300 mil) SPDIP (Skinny Plastic Dual In-Line) SS = 28-lead (5.30 mm) SSOP (Plastic Shrink Small Outline)	
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) ES = Engineering Sample	