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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	AES, Brown-out Detect/Reset, DMA, I²S, HLVD, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj64ga202t-i-ss

3.2 CPU Control Registers

REGISTER 3-1: SR: ALU STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	DC
bit 15							bit 8

R/W-0(1)	R/W-0(1)	R/W-0(1)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2(2)	IPL1(2)	IPL0(2)	RA	N	OV	Z	C
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **DC:** ALU Half Carry/Borrow bit
1 = A carry out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
0 = No carry out from the 4th or 8th low-order bit of the result has occurred

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits(1,2)
111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

bit 4 **RA:** REPEAT Loop Active bit
1 = REPEAT loop in progress
0 = REPEAT loop not in progress

bit 3 **N:** ALU Negative bit
1 = Result was negative
0 = Result was not negative (zero or positive)

bit 2 **OV:** ALU Overflow bit
1 = Overflow occurred for signed (2's complement) arithmetic in this arithmetic operation
0 = No overflow has occurred

bit 1 **Z:** ALU Zero bit
1 = An operation, which affects the Z bit, has set it at some time in the past
0 = The most recent operation, which affects the Z bit, has cleared it (i.e., a non-zero result)

bit 0 **C:** ALU Carry/$\overline{\text{Borrow}}$ bit
1 = A carry out from the Most Significant bit (MSb) of the result occurred
0 = No carry out from the Most Significant bit of the result occurred

Note 1: The IPLx Status bits are read-only when NSTDIS (INTCON1<15>) = 1.
2: The IPLx Status bits are concatenated with the IPL3 Status (CORCON<3>) bit to form the CPU Interrupt Priority Level (IPL). The value in parentheses indicates the IPL when IPL3 = 1.

TABLE 4-9: I²C™ REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1RCV	02DA	—	—	—	—	—	—	—	—	I2C1 Receive Register								0000
I2C1TRN	02DC	—	—	—	—	—	—	—	—	I2C1 Transmit Register								00FF
I2C1BRG	02DE	—	—	—	—	Baud Rate Generator Register												0000
I2C1CONL	02E0	I2CEN	—	I2CSIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1CONH	02E2	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
I2C1STAT	02E4	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/$\overline{A}$	P	S	R/$\overline{W}$	RBF	TBF	0000
I2C1ADD	02E6	—	—	—	—	—	—	I2C1 Address Register										0000
I2C1MSK	02E8	—	—	—	—	—	—	I2C1 Address Mask Register										0000
I2C2RCV	02EA	—	—	—	—	—	—	—	—	I2C2 Receive Register								0000
I2C2TRN	02EC	—	—	—	—	—	—	—	—	I2C2 Transmit Register								00FF
I2C2BRG	02EE	—	—	—	—	Baud Rate Generator Register												0000
I2C2CONL	02F0	I2CEN	—	I2CSIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C2CONH	02F2	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
I2C2STAT	02F4	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/$\overline{A}$	P	S	R/$\overline{W}$	RBF	TBF	0000
I2C2ADD	02F6	—	—	—	—	—	—	I2C2 Address Register										0000
I2C2MSK	02F8	—	—	—	—	—	—	I2C2 Address Mask Register										0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-18: A/D CONVERTER REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADC1BUF0	0200	A/D Data Buffer 0/Threshold for Channel 0																xxxx
ADC1BUF1	0202	A/D Data Buffer 1/Threshold for Channel 1																xxxx
ADC1BUF2	0204	A/D Data Buffer 2/Threshold for Channel 2																xxxx
ADC1BUF3	0206	A/D Data Buffer 3/Threshold for Channel 3																xxxx
ADC1BUF4	0208	A/D Data Buffer 4/Threshold for Channel 4																xxxx
ADC1BUF5	020A	A/D Data Buffer 5/Threshold for Channel 5																xxxx
ADC1BUF6	020C	A/D Data Buffer 6/Threshold for Channel 6																xxxx
ADC1BUF7	020E	A/D Data Buffer 7/Threshold for Channel 7																xxxx
ADC1BUF8	0210	A/D Data Buffer 8/Threshold for Channel 8/Threshold for Channel 0 in Windowed Compare mode																xxxx
ADC1BUF9	0212	A/D Data Buffer 9/Threshold for Channel 9/Threshold for Channel 1 in Windowed Compare mode																xxxx
ADC1BUF10	0214	A/D Data Buffer 10/Threshold for Channel 10/Threshold for Channel 2 in Windowed Compare mode(1)																xxxx
ADC1BUF11	0216	A/D Data Buffer 11/Threshold for Channel 11/Threshold for Channel 3 in Windowed Compare mode(1)																xxxx
ADC1BUF12	0218	A/D Data Buffer 12/Threshold for Channel 12/Threshold for Channel 4 in Windowed Compare mode(1)																xxxx
ADC1BUF13	021A	A/D Data Buffer 13																xxxx
ADC1BUF14	021C	A/D Data Buffer 14																xxxx
ADC1BUF15	021E	A/D Data Buffer 15																xxxx
AD1CON1	0220	ADON	—	ADSIDL	DMABM	DMAEN	MODE12	FORM1	FORM0	SSRC3	SSRC2	SSRC1	SSRC0	—	ASAM	SAMP	DONE	0000
AD1CON2	0222	PVCFG1	PVCFG0	NVCFG0	OFFCAL	BUFREGEN	CSCNA	—	—	BUFS	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS	0000
AD1CON3	0224	ADRC	EXTSAM	PUMPEN	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0	ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	0000
AD1CHS	0228	CH0NB2	CH0NB1	CH0NB0	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0	CH0NA2	CH0NA1	CH0NA0	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0	0000
AD1CSSH	022A	CSS<31:27>					—	—	—	—	—	—	—	—	—	—	—	0000
AD1CSSL	022C	—	CSS<14:0>(1)															0000
AD1CON4	022E	—	—	—	—	—	—	—	—	—	—	—	—	—	DMABL<2:0>			0000
AD1CON5	0230	ASEN	LPEN	CTMREQ	BGREQ	—	—	ASINT1	ASINT0	—	—	—	—	WM1	WM0	CM1	CM0	0000
AD1CHITL	0234	—	—	—	CHH<12:0>(1)													0000
AD1CTMENL	0238	—	—	—	CTMEN<12:0>(1)													0000
AD1DMBUF	023A	A/D Conversion Data Buffer (Extended Buffer mode)																xxxx

Legend: — = unimplemented, read as '0'; x = unknown value on Reset. Reset values are shown in hexadecimal.

Note 1: The CSS<12:10>, CHH<12:10> and CTMEN<12:10> bits are unimplemented in 28-pin devices, read as '0'.

REGISTER 8-32: IPC11: INTERRUPT PRIORITY CONTROL REGISTER 11

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	DMA4IP2	DMA4IP1	DMA4IP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	PMPIP2	PMPIP1	PMPIP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **DMA4IP<2:0>:** DMA Channel 4 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **PMPIP<2:0>:** Parallel Master Port Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as '0'

REGISTER 8-35: IPC14: INTERRUPT PRIORITY CONTROL REGISTER 14

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	SPI2RXIP2	SPI2RXIP1	SPI2RXIPO	—	SPI1RXIP2	SPI1RXIP1	SPI1RXIPO
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	KEYSTRIP2	KEYSTRIP1	KEYSTRIP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **SPI2RXIP<2:0>:** SPI2 Receive Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **SPI1RXIP<2:0>:** SPI1 Receive Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **KEYSTRIP<2:0>:** Cryptographic Key Store Program Done Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

REGISTER 8-40: IPC20: INTERRUPT PRIORITY CONTROL REGISTER 20

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U3TXIP2	U3TXIP1	U3TXIP0	—	U3RXIP2	U3RXIP1	U3RXIP0
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	U3ERIP2	U3ERIP1	U3ERIP0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **U3TXIP<2:0>:** UART3 Transmitter Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **U3RXIP<2:0>:** UART3 Receiver Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **U3ERIP<2:0>:** UART3 Error Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as '0'

A recommended code sequence for a clock switch includes the following:

1. Disable interrupts during the OSCCON register unlock and write sequence.
2. Execute the unlock sequence for the OSCCON high byte by writing 78h and 9Ah to OSCCON<15:8> in two back-to-back instructions.
3. Write the new oscillator source to the NOSCx bits in the instruction immediately following the unlock sequence.
4. Execute the unlock sequence for the OSCCON low byte by writing 46h and 57h to OSCCON<7:0> in two back-to-back instructions.
5. Set the OSWEN bit in the instruction immediately following the unlock sequence.
6. Continue to execute code that is not clock- sensitive (optional).
7. Invoke an appropriate amount of software delay (cycle counting) to allow the selected oscillator and/or PLL to start and stabilize.
8. Check to see if OSWEN is '0'. If it is, the switch was successful. If OSWEN is still set, then check the LOCK bit to determine the cause of the failure.

The core sequence for unlocking the OSCCON register and initiating a clock switch is shown in Example 9-1.

EXAMPLE 9-1: BASIC CODE SEQUENCE FOR CLOCK SWITCHING

```
;Place the new oscillator selection in W0
;OSCCONH (high byte) Unlock Sequence
MOV         #OSCCONH, w1
MOV         #0x78, w2
MOV         #0x9A, w3
MOV.b       w2, [w1]
MOV.b       w3, [w1]
;Set new oscillator selection
MOV.b       WREG, OSCCONH
;OSCCONL (low byte) unlock sequence
MOV         #OSCCONL, w1
MOV         #0x46, w2
MOV         #0x57, w3
MOV.b       w2, [w1]
MOV.b       w3, [w1]
;Start oscillator switch operation
BSET        OSCCON,#0
```

9.5 FRC Self-Tuning

PIC24FJ128GA204 family devices include an automatic mechanism to calibrate the FRC during run time. This system uses clock recovery from a source of known accuracy to maintain the FRC within a very narrow margin of its nominal 8 MHz frequency. This allows for a frequency accuracy that exceeds 0.25%, which is well within the requirements.

The self-tune system is controlled by the bits in the upper half of the OSCTUN register. Setting the STEN bit (OSCTUN<15>) enables the system, causing it to recover a calibration clock from a source selected by the STSRC bit (OSCTUN<12>). When STSRC = 0, the system uses the crystal controlled SOSC for its calibration source. Regardless of the source, the system uses the TUN<5:0> bits (OSCTUN<5:0>) to change the FRC's frequency. Frequency monitoring and adjustment is dynamic, occurring continuously during run time. While the system is active, the TUNx bits cannot be written to by software.

Note:	If the SOSC is to be used as the clock recovery source (STSRC = 0), the SOSC must always be enabled.

The self-tune system can generate a hardware interrupt, FSTIF. The interrupt can result from a drift of the FRC from the reference by greater than 0.2% in either direction or whenever the frequency deviation is beyond the ability of the TUNx bits to correct (i.e., greater than 1.5%). The STLOCK and STOR status bits (OSCTUN<11,9>) are used to indicate these conditions.

The STLPOL and STORPOL bits (OSCTUN<10,8>) configure the FSTIF interrupt to occur in the presence or the absence of the conditions. It is the user's responsibility to monitor both the STLOCK and STOR bits to determine the exact cause of the interrupt.

Note:	The STLPOL and STORPOL bits should be ignored when the self-tune system is disabled (STEN = 0).

11.4 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. In an application that needs to use more than one peripheral multiplexed on a single pin, inconvenient work arounds in application code, or a complete redesign, may be the only option.

The Peripheral Pin Select (PPS) feature provides an alternative to these choices by enabling the user's peripheral set selection and its placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the microcontroller to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of any one of many digital peripherals to any one of these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.4.1 AVAILABLE PINS

The PPS feature is used with a range of up to 44 pins, depending on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the designation, "RPn" or "RPIn", in their full pin designation, where "n" is the remappable pin number. "RP" is used to designate pins that support both remappable input and output functions, while "RPI" indicates pins that support remappable input functions only.

PIC24FJ128GA204 family devices support a larger number of remappable input only pins than remappable input/output pins. In this device family, there are up to 25 remappable input/output pins, depending on the pin count of the particular device selected. These pins are numbered, RP0 through RP25.

See Table 1-3 for a summary of pinout options in each package offering.

11.4.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digital only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer related peripherals (input capture and output compare) and external interrupt inputs. Also included are the outputs of the comparator module, since these are discrete digital signals.

PPS is not available for these peripherals:

- I^2C™ (input and output)
- Change Notification Inputs
- RTCC Alarm Output(s)
- EPMP Signals (input and output)
- Analog (inputs and outputs)
- INT0

A key difference between pin select and non-pin select peripherals is that pin select peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-pin select peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

11.4.2.1 Peripheral Pin Select Function Priority

Pin-selectable peripheral outputs (e.g., output compare, UART transmit) will take priority over general purpose digital functions on a pin, such as EPMP and port I/O. Specialized digital outputs will take priority over PPS outputs on the same pin. The pin diagrams list peripheral outputs in the order of priority. Refer to them for priority concerns on a particular pin.

Unlike PIC24F devices with fixed peripherals, pin-selectable peripheral inputs will never take ownership of a pin. The pin's output buffer will be controlled by the TRISx setting or by a fixed peripheral on the pin. If the pin is configured in Digital mode, then the PPS input will operate correctly. If an analog function is enabled on the pin, the PPS input will be disabled.

11.4.3 CONTROLLING PERIPHERAL PIN SELECT

PPS features are controlled through two sets of Special Function Registers (SFRs): one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on if an input or an output is being mapped.

NOTES:

16.5 Audio Mode

To set up the SPIx module for Audio mode:

1. Clear the SPIxBUFL and SPIxBUFH registers.
2. If using interrupts:
   a) Clear the interrupt flag bits in the respective IFSx register.
   b) Set the interrupt enable bits in the respective IECx register.
   a) Write the SPIxIP<2:0> bits in the respective IPCx register to set the interrupt priority.
3. Write the desired settings to the SPIxCON1L, SPIxCON1H and SPIxCON2L registers with AUDEN (SPIxCON1H<15>) = 1.
4. Clear the SPIROV bit (SPIxSTATL<6>).
5. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L<15>).
6. Write the data to be transmitted to the SPIxBUFL and SPIxBUFH registers. Transmission (and reception) will start as soon as data is written to the SPIxBUFL and SPIxBUFH registers.

16.6 Registers

The SPI module consists of the following Special Function Registers (SFRs):

- SPIxCON1L, SPIxCON1H and SPIxCON2L: SPIx Control Registers (Register 16-1, Register 16-2 and Register 16-3)
- SPIxSTATL and SPIxSTATH: SPIx Status Registers (Register 16-4 and Register 16-5)
- SPIxBUFL and SPIxBUFH: SPIx Buffer Registers
- SPIxBRGL and SPIxBRGH: SPIx Baud Rate Registers
- SPIxIMSKL and SPIxIMSKH: SPIx Interrupt Mask Registers (Register 16-6 and Register 16-7)
- SPIxURDTL and SPIxURDTH: SPIx Underrun Data Registers

REGISTER 16-1: SPIxCON1L: SPIx CONTROL REGISTER 1 LOW

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPIEN	—	SPISIDL	DISSDO	MODE32(1,4)	MODE16(1,4)	SMP	CKE(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SSEN(2)	CKP	MSTEN	DISSDI	DISSCK	MCLKEN(3)	SPIFE	ENHBUF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **SPIEN:** SPIx On bit
1 = Enables module
0 = Turns off and resets module, disables clocks, disables interrupt event generation, allows SFR modifications

bit 14 **Unimplemented:** Read as '0'

bit 13 **SPISIDL:** SPIx Stop in Idle Mode bit
1 = Halts in CPU Idle mode
0 = Continues to operate in CPU Idle mode

bit 12 **DISSDO:** Disable SDOx Output Port bit
1 = SDOx pin is not used by the module; pin is controlled by the port function
0 = SDOx pin is controlled by the module

Note 1: When AUDEN = 1, this module functions as if CKE = 0, regardless of its actual value.
2: When FRMEN = 1, SSEN is not used.
3: MCLKEN can only be written when the SPIEN bit = 0.
4: This channel is not meaningful for DSP/PCM mode as LRC follows FRMSYPW.

REGISTER 16-4: SPIxSTATL: SPIx STATUS REGISTER LOW (CONTINUED)

bit 2 **Unimplemented:** Read as '0'

bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit

1 = SPIxTXB is full
0 = SPIxTXB not full

Standard Buffer Mode:
Automatically set in hardware when SPIxBUF is written, loading SPIxTXB. Automatically cleared in hardware when SPIx transfers data from SPIxTXB to SPIxTXSR.

Enhanced Buffer Mode:
Indicates TXELM<5:0> = 6'b111111.

bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit

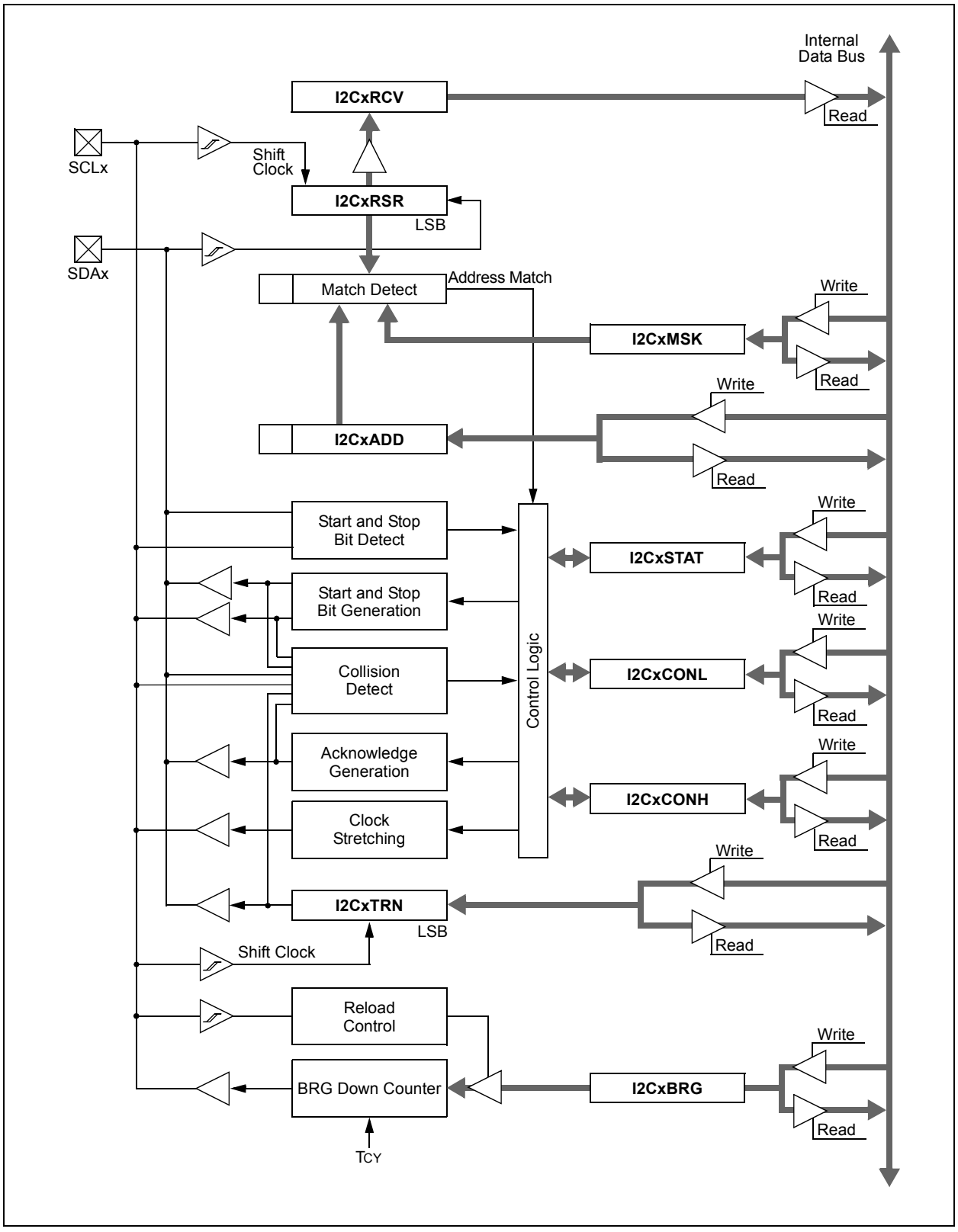
1 = SPIxRXB is full
0 = SPIxRXB is not full

Standard Buffer Mode:
Automatically set in hardware when SPIx transfers data from SPIxRXSR to SPIxRXB. Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.

Enhanced Buffer Mode:
Indicates RXELM<5:0> = 6'b111111.

Note 1: SPITUR is cleared when SPIEN = 0. When IGNTUR = 1, SPITUR provides dynamic status of the Transmit Underrun condition, but does not stop RX/TX operation and does not need to be cleared by software.

FIGURE 17-1: I2Cx BLOCK DIAGRAM



REGISTER 22-5: CFGPAGE: SECURE ARRAY CONFIGURATION BITS (OTP PAGE 0) REGISTER (CONTINUED)

bit 19 **SKEYEN:** Session Key Enable bit

1 = Stored Key #1 may be used only as a Key Encryption Key
0 = Stored Key #1 may be used for any operation

bit 18-11 **LKYSRC<7:0>:** Locked Key Source Configuration bits

If SRCLCK = 1:
1xxxxxxx = Key Source is as if KEYSRC<3:0> = 1111
01xxxxxx = Key Source is as if KEYSRC<3:0> = 0111
001xxxxx = Key Source is as if KEYSRC<3:0> = 0110
0001xxxx = Key Source is as if KEYSRC<3:0> = 0101
00001xxx = Key Source is as if KEYSRC<3:0> = 0100
000001xx = Key Source is as if KEYSRC<3:0> = 0011
0000001x = Key Source is as if KEYSRC<3:0> = 0010
00000001 = Key Source is as if KEYSRC<3:0> = 0001
00000000 = Key Source is as if KEYSRC<3:0> = 0000

If SRCLCK = 0:
These bits are ignored.

bit 10 **SRCLCK:** Key Source Lock bit

1 = The key source is determined by the KEYSRC<3:0> (CRYCONH<3:0>) bits (software key selection is disabled)
0 = The key source is determined by the KEYSRC<3:0> (CRYCONH<3:0>) bits (locked key selection is disabled)

bit 9-1 **WRLOCK<8:0>:** Write Lock Page Enable bits

For OTP Pages 0 (CFGPAGE) through 8:
1 = OTP Page is permanently locked and may not be programmed
0 = OTP Page is unlocked and may be programmed

bit 0 **SWKYDIS:** Software Key Disable bit

1 = Software key (CRYKEY register) is disabled; when KEYSRC<3:0> = 0000, the KEYFAIL status bit will be set and no encryption/decryption/session key operations can be started until KEYSRC<3:0> bits are changed to a value other than '0000'
0 = Software key (CRYKEY register) can be used as a key source when KEYSRC<3:0> = 0000

Note 1: This bit's state is mirrored by the PGMTST bit (CRYOTP<7>).

REGISTER 24-4: AD1CON4: A/D CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	DMABL<2:0>(1)		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2-0 **DMABL<2:0>:** DMA Buffer Size Select bits(1)

111 = Allocates 128 words of buffer to each analog input
110 = Allocates 64 words of buffer to each analog input
101 = Allocates 32 words of buffer to each analog input
100 = Allocates 16 words of buffer to each analog input
011 = Allocates 8 words of buffer to each analog input
010 = Allocates 4 words of buffer to each analog input
001 = Allocates 2 words of buffer to each analog input
000 = Allocates 1 word of buffer to each analog input

Note 1: The DMABL<2:0> bits are only used when AD1CON1<11> = 1 and AD1CON1<12> = 0; otherwise, their value is ignored.

REGISTER 24-8: AD1CHITL: A/D SCAN COMPARE HIT REGISTER (LOW WORD)

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	CHH<12:9>(1)				CHH8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CHH<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-9 **CHH<12:9>:** A/D Compare Hit bits(1)

If CM<1:0> = 11:
1 = A/D Result Buffer n has been written with data or a match has occurred
0 = A/D Result Buffer n has not been written with data

For All Other Values of CM<1:0>:
1 = A match has occurred on A/D Result Channel n
0 = No match has occurred on A/D Result Channel n

bit 8-0 **CHH<8:0>:** A/D Compare Hit bits

If CM<1:0> = 11:
1 = A/D Result Buffer n has been written with data or a match has occurred
0 = A/D Result Buffer n has not been written with data

For All Other Values of CM<1:0>:
1 = A match has occurred on A/D Result Channel n
0 = No match has occurred on A/D Result Channel n

Note 1: The CHH<12:10> bits are unimplemented in 28-pin devices, read as '0'.

REGISTER 24-11: AD1CTMENL: CTMU ENABLE REGISTER (LOW WORD)

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	CTMEN<12:8>(1)				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMEN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-0 **CTMEN<12:0>:** CTMU Enable During Conversion bits(1)
1 = CTMU is enabled and connected to the selected channel during conversion
0 = CTMU is not connected to this channel

Note 1: The CTMEN<12:10> bits are unimplemented in 28-pin devices, read as '0'.

REGISTER 25-1: CMxCON: COMPARATOR x CONTROL REGISTERS (COMPARATORS 1 THROUGH 3)

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0, HS	R-0, HSC
CON	COE	CPOL	—	—	—	CEVT	COUT
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1(1)	EVPOL0(1)	—	CREF	—	—	CCH1	CCH0
bit 7							bit 0

Legend:	HS = Hardware Settable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 14 **COE:** Comparator Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **CEVT:** Comparator Event bit
1 = Comparator event that is defined by EVPOL<1:0> has occurred; subsequent triggers and interrupts are disabled until the bit is cleared
0 = Comparator event has not occurred

bit 8 **COUT:** Comparator Output bit
When CPOL = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits(1)
11 = Trigger/event/interrupt is generated on any change of the comparator output (while CEVT = 0)
10 = Trigger/event/interrupt is generated on the high-to-low transition of the comparator output
01 = Trigger/event/interrupt is generated on the low-to-high transition of the comparator output
00 = Trigger/event/interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Reference Select bit (non-inverting input)
1 = Non-inverting input connects to the internal CVREF voltage
0 = Non-inverting input connects to the CxINA pin

bit 3-2 **Unimplemented:** Read as '0'

Note 1: If the EVPOL<1:0> bits are set to a value other than '00', the first interrupt generated will occur on any transition of COUT. Subsequent interrupts will occur based on the EVPOLx bits setting.

26.0 COMPARATOR VOLTAGE REFERENCE

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Comparator Voltage Reference Module"** (DS39709). The information in this data sheet supersedes the information in the FRM.

26.1 Configuring the Comparator Voltage Reference

The comparator voltage reference module is controlled through the CVRCON register (Register 26-1). The comparator voltage reference provides a range of output voltages with 32 distinct levels. The comparator reference supply voltage can come from either VDD and VSS or the external CVREF+ and CVREF- pins. The voltage source is selected by the CVRSS bit (CVRCON<5>).

The settling time of the comparator voltage reference must be considered when changing the CVREF output.

FIGURE 26-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

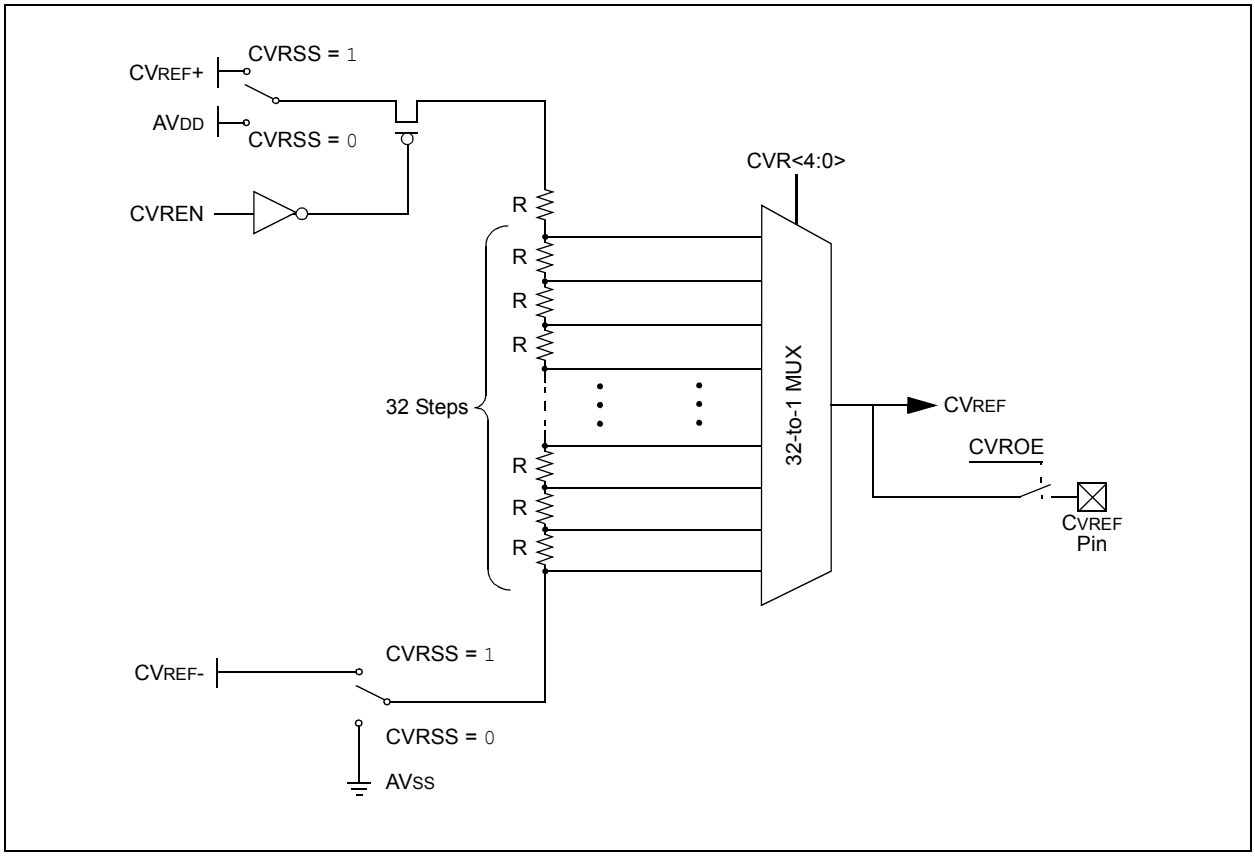


TABLE 32-7: DC CHARACTERISTICS: Δ CURRENT (BOR, WDT, DSBOR, DSWDT)(4)

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Operating Temperature**	**VDD**	**Conditions**
Incremental Current Brown-out Reset (ΔBOR)(2)						
DC25	3.1	5.0	µA	-40°C to +125°C	2.0V	ΔBOR(2)
	4.3	6.0	µA	-40°C to +125°C	3.3V	
Incremental Current Watchdog Timer (ΔWDT)(2)						
DC71	0.8	1.5	µA	-40°C to +125°C	2.0V	ΔWDT(2)
	0.8	1.5	µA	-40°C to +125°C	3.3V	
Incremental Current High/Low-Voltage Detect (ΔHLVD)(2)						
DC75	4.2	15	µA	-40°C to +125°C	2.0V	ΔHLVD(2)
	4.2	15	µA	-40°C to +125°C	3.3V	
Incremental Current Real-Time Clock and Calendar (ΔRTCC)(2)						
DC77	0.3	1.0	µA	-40°C to +125°C	2.0V	ΔRTCC (with SOSC)(2)
	0.35	1.0	µA	-40°C to +125°C	3.3V	
DC77A	0.3	1.0	µA	-40°C to +125°C	2.0V	ΔRTCC (with LPRC)(2)
	0.35	1.0	µA	-40°C to +125°C	3.3V	
Incremental Current Deep Sleep BOR (ΔDSBOR)(2)						
DC81	0.11	0.40	µA	-40°C to +125°C	2.0V	ΔDeep Sleep BOR(2)
	0.12	0.40	µA	-40°C to +125°C	3.3V	
Incremental Current Deep Sleep Watchdog Timer Reset (ΔDSWDT)(2)						
DC80	0.24	0.40	µA	-40°C to +125°C	2.0V	ΔDeep Sleep WDT(2)
	0.24	0.40	µA	-40°C to +125°C	3.3V	
VBAT A/D Monitor(3)						
DC91	1.5	—	µA	-40°C to +125°C	3.3V	VBAT = 2V
	4	—	µA	-40°C to +125°C	3.3V	VBAT = 3.3V

Note 1: Data in the Typical column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Incremental current while the module is enabled and running.

3: The A/D channel is connected to the VBAT pin internally; this is the current during A/D VBAT operation.

4: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

APPENDIX A: REVISION HISTORY

Revision A (July 2013)

Original data sheet for the PIC24FJ128GA204 family of devices.

Revision B (May 2014)

This revision incorporates the following updates:

- Sections:
  - Added **Section 16.5 "Audio Mode"** and **Section 16.6 "Registers" Section 16.1 "Standard Master Mode"**, **Section 16.2 "Standard Slave Mode"**, **Section 16.3 "Enhanced Master Mode"** and **Section 16.4 "Enhanced Slave Mode"**
  - Added **Section 18.9 "Registers"**
  - Updated **Section 17.3 "Slave Address Masking"**,
  - Updated **Section 29.3.1 "Windowed Operation"**
- Registers:
  - Updated Register 8-45, Register 11-2, Register 11-29, Register 16-6, Register 16-7, Register 17-1, Register 17-2, Register 18-2, Register 18-4, Register 18-6, Register 22-5
  - Updated note in **Section 18.0 "Universal Asynchronous Receiver Transmitter (UART)"**
  - Updated Sections: **Section 18.5 "Receiving in 8-Bit or 9-Bit Data Mode"**
- Tables:
  - Included Table 32-22, Table 32-23, Table 32-24 and Table 32-25
  - Updated Tables:Table 4-4, Table 4-6, Table 4-9, Table 4-10, Table 4-11, Table 4-12, Table 4-13, Table 4-28, Table 32-3, Table 32-4, Table 32-5, Table 32-6, Table 32-7, Table 32-8, Table 32-10, Table 32-12, Table 32-13, Table 32-14, Table 32-15, Table 32-16 and Table 32-20
- Figures:
  - Included Figure 32-5, Figure 32-6, Figure 32-7 and Figure 32-8
- Examples:
  - Updated Example 21-1
- Packaging diagrams in **Section 33.0 "Packaging Information"** were updated
- Changes to text and formatting were incorporated throughout the document

Revision C (March 2015)

This revision incorporates the following updates:

- Registers:
  - Register 25-1
- Tables:
  - Table 32-4, Table 32-5, Table 32-6 and Table 32-21
- Package Marking examples in **Section 33.0 "Packaging Information"** were updated