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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	56
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.85V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg230f1024-qfn64

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1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32GG230 devices.

Table 1.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (ºC)	Package
EFM32GG230F512G-E-QFN64	512	128	48	1.98 - 3.8	-40 - 85	QFN64
EFM32GG230F1024G-E-QFN64	1024	128	48	1.98 - 3.8	-40 - 85	QFN64

Adding the suffix 'R' to the part number (e.g. EFM32GG230F512G-E-QFN64R) denotes tape and reel.

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2 System Summary

2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32GG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32GG230 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32GG Reference Manual*.

A block diagram of the EFM32GG230 is shown in Figure 2.1 (p. 3) .



Figure 2.1. Block Diagram

2.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M3 is described in detail in *EFM32 Cortex-M3 Reference Manual*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface and an Embedded Trace Module (ETM) for data/instruction tracing. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

2.1.11 Universal Synchronous/Asynchronous Receiver/Transmitter (US-ART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

2.1.12 Pre-Programmed UART Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Autobaud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

2.1.13 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUARTTM, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

2.1.14 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

2.1.15 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

2.1.16 Backup Real Time Counter (BURTC)

The Backup Real Time Counter (BURTC) contains a 32-bit counter and is clocked either by a 32.768 kHz crystal oscillator, a 32.768 kHz RC oscillator or a 1 kHz ULFRCO. The BURTC is available in all Energy Modes and it can also run in backup mode, making it operational even if the main power should drain out.

2.1.17 Low Energy Timer (LETIMER)

The unique LETIMERTM, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

2.1.18 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

2.1.27 General Purpose Input/Output (GPIO)

In the EFM32GG230, there are 56 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

2.2 Configuration Summary

The features of the EFM32GG230 is a subset of the feature set described in the EFM32GG Reference Manual. Table 2.1 (p. 7) describes device specific implementation of the features.

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
СМU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
I2C1	Full configuration	I2C1_SDA, I2C1_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration with I2S	US2_TX, US2_RX, US2_CLK, US2_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
TIMER3	Full configuration	TIM3_CC[2:0]
RTC	Full configuration	NA
BURTC	Full configuration	NA
LETIMERO	Full configuration	LET0_O[1:0]

Table 2.1. Configuration Summary

Module	Configuration	Pin Connections
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DACO	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
ОРАМР	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	56 pins	Available pins are shown in Table 4.3 (p. 55)

2.3 Memory Map

The *EFM32GG230* memory map is shown in Figure 2.2 (p. 8), with RAM and Flash sizes for the largest memory configuration.

Figure 2.2. EFM32GG230 Memory Map with largest RAM and Flash sizes



3.4.1 EM2 Current Consumption

Figure 3.1. EM2 current consumption. RTC¹ prescaled to 1 Hz, 32.768 kHz LFRCO.



3.4.2 EM3 Current Consumption

Figure 3.2. EM3 current consumption.



¹Using backup RTC.

3.8 General Purpose Input Output

Table 3.7. GPIO

Symbol	Parameter	Condition	Min	Тур	Max	Unit
V _{IOIL}	Input low voltage				0.30V _{DD}	V
V _{IOIH}	Input high voltage		0.70V _{DD}			V
		Sourcing 0.1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.80V _{DD}		V
		Sourcing 0.1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.90V _{DD}		V
		Sourcing 1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.85V _{DD}		V
Viceu	Output high volt- age (Production test	Sourcing 1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.90V _{DD}		V
VIOOH	DRIVEMODE = STANDARD)	Sourcing 6 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.75V _{DD}			V
		Sourcing 6 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.85V _{DD}			V
		Sourcing 20 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.60V _{DD}			V
		Sourcing 20 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.80V _{DD}			V
		Sinking 0.1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.20V _{DD}		V
		Sinking 0.1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.10V _{DD}		V
		Sinking 1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.10V _{DD}		V
V _{IOOL}	(Production test condition = 3.0V, DRIVEMODE =	Sinking 1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.05V _{DD}		V
	STANDARD)	Sinking 6 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.30V _{DD}	V
		Sinking 6 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.20V _{DD}	V
		Sinking 20 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.35V _{DD}	V



Symbol	Parameter	Condition	Min	Тур	Max	Unit
		Sinking 20 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.20V _{DD}	V
I _{IOLEAK}	Input leakage cur- rent	High Impedance IO connected to GROUND or V_{DD}		±0.1	±40	nA
R _{PU}	I/O pin pull-up resis- tor			40		kOhm
R _{PD}	I/O pin pull-down re- sistor			40		kOhm
R _{IOESD}	Internal ESD series resistor			200		Ohm
t _{IOGLITCH}	Pulse width of puls- es to be removed by the glitch sup- pression filter		10		50	ns
•	Output fall time	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capaci- tance C_L =12.5-25pF.	20+0.1C _L		250	ns
UOOF			20+0.1C _L		250	ns
V _{IOHYST}	I/O pin hysteresis (V _{IOTHR+} - V _{IOTHR-})	V _{DD} = 1.98 - 3.8 V	0.10V _{DD}			V



Symbol	Parameter	Condition	Min	Тур	Max	Unit
		200 kSamples/s, 12 bit, sin- gle ended, internal 1.25V refer- ence		62		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		200 kSamples/s, 12 bit, single ended, V _{DD} reference		67		dB
		200 kSamples/s, 12 bit, differ- ential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differ- ential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differ- ential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	63	66		dB
		200 kSamples/s, 12 bit, differ- ential, 2xV _{DD} reference		70		dB
		1 MSamples/s, 12 bit, single ended, internal 1.25V refer- ence		58		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		62		dB
		1 MSamples/s, 12 bit, single ended, V _{DD} reference		64		dB
		1 MSamples/s, 12 bit, differen- tial, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differen- tial, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differen- tial, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
SINAD _{ADC}	SIgnal-to-Noise And Distortion-ratio (SINAD)	1 MSamples/s, 12 bit, differen- tial, 2xV _{DD} reference		68		dB
		200 kSamples/s, 12 bit, sin- gle ended, internal 1.25V refer- ence		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V _{DD} reference		66		dB
		200 kSamples/s, 12 bit, differ- ential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differ- ential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differ- ential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	62	65		dB



Symbol	Parameter	Condition	Min	Тур	Max	Unit
		200 kSamples/s, 12 bit, differ- ential, 2xV _{DD} reference		69		dB
		1 MSamples/s, 12 bit, single ended, internal 1.25V refer- ence		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc
		1 MSamples/s, 12 bit, single ended, V _{DD} reference		73		dBc
		1 MSamples/s, 12 bit, differen- tial, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differen- tial, internal 2.5V reference		77		dBc
		1 MSamples/s, 12 bit, differen- tial, V _{DD} reference		76		dBc
		1 MSamples/s, 12 bit, differen- tial, 2xV _{DD} reference		75		dBc
SEDRADO	Spurious-Free Dy-	1 MSamples/s, 12 bit, differen- tial, 5V reference		69		dBc
SI DINADC	DR)	200 kSamples/s, 12 bit, sin- gle ended, internal 1.25V refer- ence		75		dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, V _{DD} reference		76		dBc
		200 kSamples/s, 12 bit, differ- ential, internal 1.25V reference		79		dBc
		200 kSamples/s, 12 bit, differ- ential, internal 2.5V reference		79		dBc
		200 kSamples/s, 12 bit, differ- ential, 5V reference		78		dBc
		200 kSamples/s, 12 bit, differ- ential, V _{DD} reference	68	79		dBc
		200 kSamples/s, 12 bit, differ- ential, 2xV _{DD} reference		79		dBc
	Offset voltage	After calibration, single ended		0.3		mV
ADCOFFSET	Cliser voltage	After calibration, differential	-3	0.3	3	mV
				-1.92		mV/°C
TGRAD _{ADCTH}	Thermometer out- put gradient			-6.3		ADC Codes/ °C
DNL _{ADC}	Differential non-lin- earity (DNL)	V _{DD} = 3.0 V, external 2.5V reference	-1	±0.7	4	LSB
INL _{ADC}	Integral non-linear- ity (INL), End point method			±1.2	±3.0	LSB
MC _{ADC}	No missing codes		11.999 ¹	12		bits

3.10.1 Typical performance

Figure 3.19. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°C



Symbol	Parameter	Condition	Min	Тур	Max	Unit
		500 kSamples/s, 12 bit, differ- ential, internal 2.5V reference		58		dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference		59		dB
		500 kSamples/s, 12 bit, sin- gle ended, internal 1.25V refer- ence		57		dB
	Signal to Noise-	500 kSamples/s, 12 bit, single ended, internal 2.5V reference		54		dB
SNDR _{DAC}	pulse Distortion Ra- tio (SNDR)	500 kSamples/s, 12 bit, differ- ential, internal 1.25V reference		56		dB
		500 kSamples/s, 12 bit, differ- ential, internal 2.5V reference		53		dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference		55		dB
		500 kSamples/s, 12 bit, sin- gle ended, internal 1.25V refer- ence		62		dBc
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		56		dBc
SFDR _{DAC}	Dynamic Range(SFDR)	500 kSamples/s, 12 bit, differ- ential, internal 1.25V reference		61		dBc
		500 kSamples/s, 12 bit, differ- ential, internal 2.5V reference		55		dBc
		500 kSamples/s, 12 bit, differential, V_{DD} reference		60		dBc
V	Offset voltage	After calibration, single ended		2	12	mV
V DACOFFSET	Oliset voltage	After calibration, differential		2		mV
DNL _{DAC}	Differential non-lin- earity			±1		LSB
INL _{DAC}	Integral non-lineari- ty			±5		LSB
MC _{DAC}	No missing codes			12		bits

¹Measured with a static input code and no loading on the output.

3.12 Operational Amplifier (OPAMP)

The electrical characteristics for the Operational Amplifiers are based on simulations.

Table 3.16. OPAMP

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
I _{OPAMP}	A stine Querrant	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, Unity Gain		350	405	μA
	Active Current	(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, Unity Gain		95	115	μA

3.14 Voltage Comparator (VCMP)

Table 3.18. VCMP

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
V _{VCMPIN}	Input voltage range			V _{DD}		V
V _{VCMPCM}	VCMP Common Mode voltage range			V _{DD}		V
	Active current	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register		0.3	0.6	μA
VCMP		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0.		22	30	μA
t _{VCMPREF}	Startup time refer- ence generator	NORMAL		10		μs
	Offset voltage	Single ended	-230	-40	190	mV
▼ VCMPOFFSET	Unset voltage	Differential		10		mV
V _{VCMPHYST}	VCMP hysteresis			40		mV
t _{VCMPSTART}	Startup time				10	μs

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

VCMP Trigger Level as a Function of Level Setting

V_{DD Trigger Level}=1.667V+0.034 ×TRIGLEVEL

3.15 I2C

Table 3.19. I2C Standard-mode (Sm)

Symbol	Parameter	Min	Тур	Max	Unit
f _{SCL}	SCL clock frequency	0		100 ¹	kHz
t _{LOW}	SCL clock low time	4.7			μs
t _{HIGH}	SCL clock high time	4.0			μs
t _{SU,DAT}	SDA set-up time	250			ns
t _{HD,DAT}	SDA hold time	8		3450 ^{2,3}	ns
t _{SU,STA}	Repeated START condition set-up time	4.7			μs
t _{HD,STA}	(Repeated) START condition hold time	4.0			μs
t _{SU,STO}	STOP condition set-up time	4.0			μs
t _{BUF}	Bus free time between a STOP and START condition	4.7			μs

¹For the minimum HFPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32GG Reference Manual. ²The maximum SDA hold time (t_{HD,DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

³When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((3450*10⁻⁹ [s] * f_{HFPERCLK} [Hz]) - 4).

(3.2)

Table 3.20. I2C Fast-mode (Fm)

Symbol	Parameter	Min	Тур	Max	Unit
f _{SCL}	SCL clock frequency	0		400 ¹	kHz
t _{LOW}	SCL clock low time	1.3			μs
t _{HIGH}	SCL clock high time	0.6			μs
t _{SU,DAT}	SDA set-up time	100			ns
t _{HD,DAT}	SDA hold time	8		900 ^{2,3}	ns
t _{SU,STA}	Repeated START condition set-up time	0.6			μs
t _{HD,STA}	(Repeated) START condition hold time	0.6			μs
t _{SU,STO}	STOP condition set-up time	0.6			μs
t _{BUF}	Bus free time between a STOP and START condition	1.3			μs

¹For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32GG Reference Manual. ²The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}). ³When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((900*10⁻⁹ [s] * f_{HFPERCLK} [Hz]) - 4).

Table 3.21. I2C Fast-mode Plus (Fm+)

Symbol	Parameter	Min	Тур	Max	Unit
f _{SCL}	SCL clock frequency	0		1000 ¹	kHz
t _{LOW}	SCL clock low time	0.5			μs
t _{ніGH}	SCL clock high time	0.26			μs
t _{SU,DAT}	SDA set-up time	50			ns
t _{HD,DAT}	SDA hold time	8			ns
t _{SU,STA}	Repeated START condition set-up time	0.26			μs
t _{HD,STA}	(Repeated) START condition hold time	0.26			μs
t _{SU,STO}	STOP condition set-up time	0.26			μs
t _{BUF}	Bus free time between a STOP and START condition	0.5			μs

¹For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32GG Reference Manual.

3.16 USART SPI

Figure 3.31. SPI Master Timing

	QFN64 Pin# and Name		Pin Alternate Functionality / Description				
Pin#	Pin Name	Analog	Timers	Communication	Other		
53	PF4		TIM0_CDTI1 #2/5		PRS_CH1 #1		
54	PF5		TIM0_CDTI2 #2/5		PRS_CH2 #1		
55	IOVDD_5	Digital IO power supply 5.					
56	PE8		PCNT2_S0IN #1		PRS_CH3 #1		
57	PE9		PCNT2_S1IN #1				
58	PE10		TIM1_CC0 #1	US0_TX #0	BOOT_TX		
59	PE11		TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX		
60	PE12		TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0		
61	PE13			US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5		
62	PE14		TIM3_CC0 #0	LEU0_TX #2			
63	PE15		TIM3_CC1 #0	LEU0_RX #2			
64	PA15		TIM3_CC2 #0				

4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 51). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCA-TION bitfield. In these cases, the pinout is shown in the column corresponding to LOCA-TION 0.

Table 4.2. Alternate functionality overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2							Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3							Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5							Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6							Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7							Analog comparator ACMP0, channel 7.
ACMP0_O	PE13		PD6					Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8							Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9							Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10							Analog comparator ACMP1, channel 2.

5 PCB Layout and Soldering

5.1 Recommended PCB Layout

Figure 5.1. QFN64 PCB Land Pattern

Table 5.1. QFN64 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin number	Symbol	Pin number
а	0.85	P1	1	P8	64
b	0.30	P2	16	P9	65
с	0.50	P3	17	-	-
d	8.90	P4	32	-	-
e	8.90	P5	33	-	-
f	7.20	P6	48	-	-
g	7.20	P7	49	-	-

Figure 5.2. QFN64 PCB Solder Mask

Table 5.2. QFN64 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Dim. (mm)
а	0.97	е	8.90
b	0.42	f	7.32
С	0.50	g	7.32
d	8.90	-	-

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

7.6 Revision 1.00

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

Other minor corrections.

7.7 Revision 0.98

May 25th, 2012

Corrected EM3 current consumption in the Electrical Characteristics section.

7.8 Revision 0.96

February 28th, 2012

Added reference to errata document.

Corrected QFN64 package drawing.

Updated PCB land pattern, solder mask and stencil design.

7.9 Revision 0.95

September 28th, 2011

Flash configuration for Giant Gecko is now 1024KB or 512KB. For flash sizes below 512KB, see the Leopard Gecko Family.

Corrected operating voltage from 1.8 V to 1.85 V.

Added rising POR level to Electrical Characteristics section.

Updated Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup.

Added Gain error drift and Offset error drift to ADC table.

Added Opamp pinout overview.

Added reference to errata document.

Corrected QFN64 package drawing.

Updated PCB land pattern, solder mask and stencil design.

7.10 Revision 0.91

March 21th, 2011

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