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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	600
Number of Logic Elements/Cells	2700
Total RAM Bits	40960
Number of I/O	176
Number of Gates	108904
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv100-5fg256c

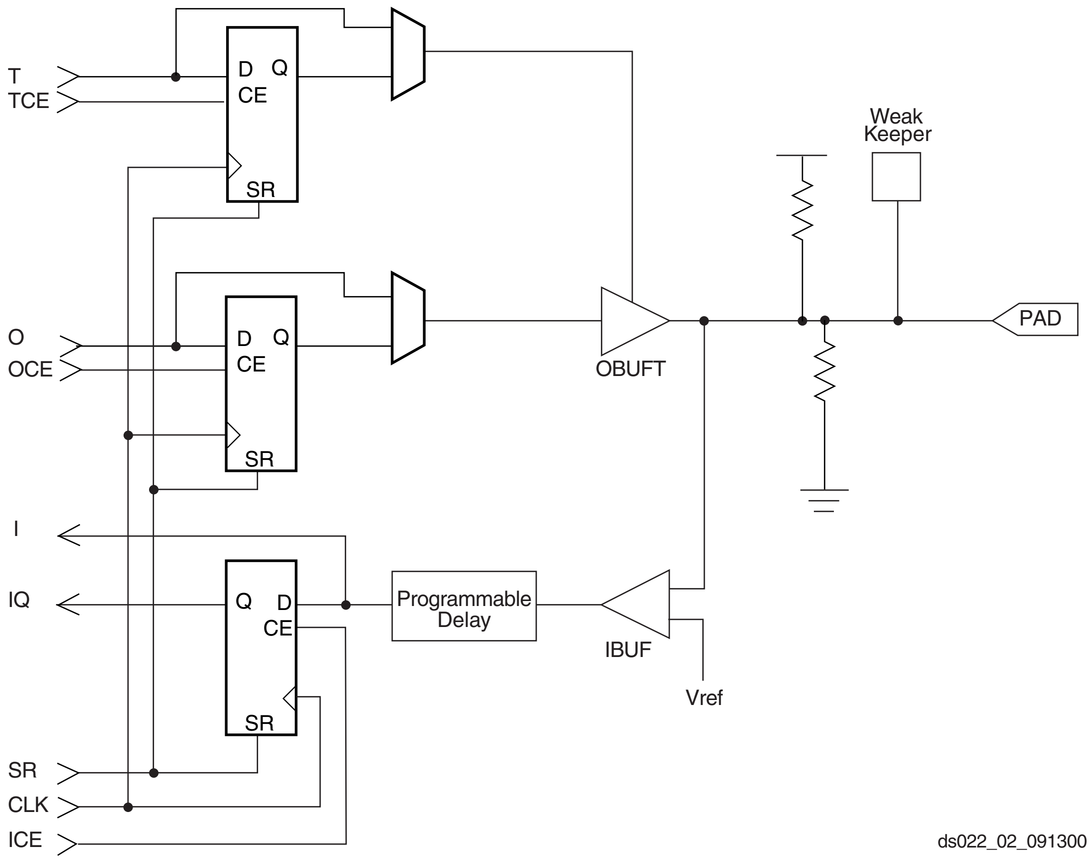


Figure 2: **Virtex Input/Output Block (IOB)**

Table 1: **Supported Select I/O Standards**

I/O Standard	Input Reference Voltage (V_{REF})	Output Source Voltage (V_{CCO})	Board Termination Voltage (V_{TT})	5 V Tolerant
LVTTL 2 – 24 mA	N/A	3.3	N/A	Yes
LVCMOS2	N/A	2.5	N/A	Yes
PCI, 5 V	N/A	3.3	N/A	Yes
PCI, 3.3 V	N/A	3.3	N/A	No
GTL	0.8	N/A	1.2	No
GTL+	1.0	N/A	1.5	No
HSTL Class I	0.75	1.5	0.75	No
HSTL Class III	0.9	1.5	1.5	No
HSTL Class IV	0.9	1.5	1.5	No
SSTL3 Class I &II	1.5	3.3	1.5	No
SSTL2 Class I & II	1.25	2.5	1.25	No
CTT	1.5	3.3	1.5	No
AGP	1.32	3.3	N/A	No

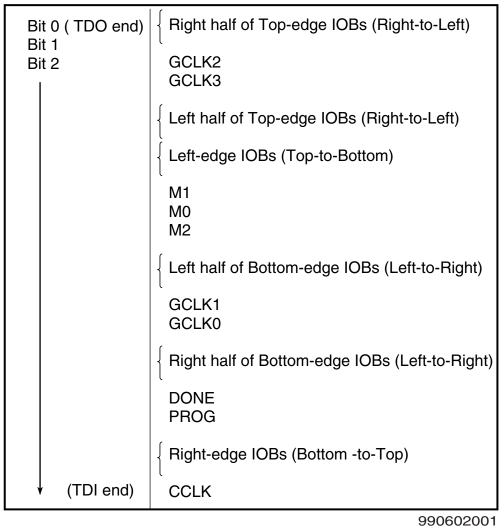


Figure 11: **Boundary Scan Bit Sequence**

Table 5: **Boundary Scan Instructions**

Boundary-Scan Command	Binary Code(4:0)	Description
EXTEST	00000	Enables boundary-scan EXTEST operation
SAMPLE/PRELOAD	00001	Enables boundary-scan SAMPLE/PRELOAD operation
USER 1	00010	Access user-defined register 1
USER 2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for read operations.
CFG_IN	00101	Access the configuration bus for write operations.
INTEST	00111	Enables boundary-scan INTEST operation
USERCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIGHZ	01010	3-states output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

Identification Registers

The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined.

The IDCODE register has the following binary format:

vvvv:ffff:fffa:aaaa:aaaa:cccc:cccc:ccc1

where

v = the die version number

f = the family code (03h for Virtex family)

a = the number of CLB rows (ranges from 010h for XCV50 to 040h for XCV1000)

c = the company code (49h for Xilinx)

The USERCODE register is supported. By using the USER-CODE, a user-programmable identification code can be loaded and shifted out for examination. The identification code is embedded in the bitstream during bitstream generation and is valid only after configuration.

Table 6: **IDCODEs Assigned to Virtex FPGAs**

FPGA	IDCODE
XCV50	v0610093h
XCV100	v0614093h
XCV150	v0618093h
XCV200	v061C093h
XCV300	v0620093h
XCV400	v0628093h
XCV600	v0630093h
XCV800	v0638093h
XCV1000	v0640093h

Including Boundary Scan in a Design

Since the boundary scan pins are dedicated, no special element needs to be added to the design unless an internal data register (USER1 or USER2) is desired.

If an internal data register is used, insert the boundary scan symbol and connect the necessary pins as appropriate.

Development System

Virtex FPGAs are supported by the Xilinx Foundation and Alliance CAE tools. The basic methodology for Virtex design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation (for example, Synopsys FPGA Express), while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under the Xilinx Design Manager (XDM™) software, providing designers with a common user interface regardless of their choice of entry and verification tools. The XDM software simplifies the selection of implementation options with pull-down menus and on-line help.

Application programs ranging from schematic capture to Placement and Routing (PAR) can be accessed through the XDM software. The program command sequence is generated prior to execution, and stored for documentation.

Several advanced software features facilitate Virtex design. RPMs, for example, are schematic-based macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the Xilinx FPGA Foundation development system provides interfaces to the following synthesis design environments.

- Synopsys (FPGA Compiler, FPGA Express)
- Exemplar (Spectrum)
- Synplicity (Synplify)

For schematic design entry, the Xilinx FPGA Foundation and alliance development system provides interfaces to the following schematic-capture design environments.

- Mentor Graphics V8 (Design Architect, QuickSim II)
- Viewlogic Systems (Viewdraw)

Third-party vendors support many other environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Virtex FPGAs supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The “soft macro” portion of the library contains detailed descriptions of common logic functions, but does not contain any partitioning or placement information. The performance of these macros depends, therefore, on the partitioning and placement obtained during implementation.

RPMs, on the other hand, do contain predetermined partitioning and placement information that permits optimal implementation of these functions. Users can create their own library of soft macros or RPMs based on the macros and primitives in the standard library.

The design environment supports hierarchical design entry, with high-level schematics that comprise major functional blocks, while lower-level schematics define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF net list for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floor planning.

The implementation software incorporates Timing Wizard® timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered on a schematic in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

Design Verification

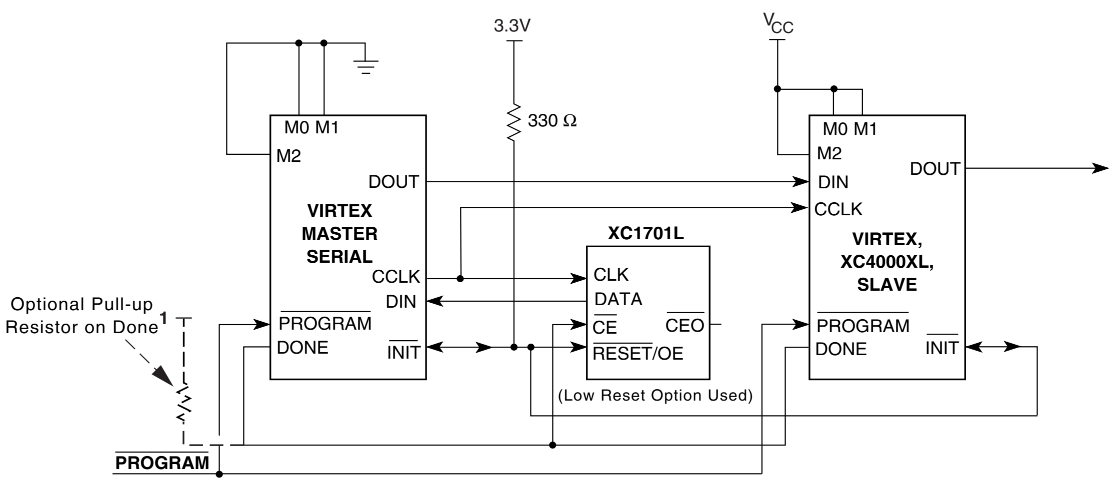
In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the net list for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the TRACE® static timing analyzer.

For in-circuit debugging, the development system includes a download and readback cable. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

Table 8: **Master/Slave Serial Mode Programming Switching**

	Description	Figure References	Symbol	Values	Units
CCLK	DIN setup/hold, slave mode	1/2	T_{DCC}/T_{CCD}	5.0 / 0	ns, min
	DIN setup/hold, master mode	1/2	T_{DSCK}/T_{CKDS}	5.0 / 0	ns, min
	DOUT	3	T_{CCO}	12.0	ns, max
	High time	4	T_{CCH}	5.0	ns, min
	Low time	5	T_{CCL}	5.0	ns, min
	Maximum Frequency		F_{CC}	66	MHz, max
	Frequency Tolerance, master mode with respect to nominal			+45% –30%	



Note 1: If none of the Virtex FPGAs have been selected to drive DONE, an external pull-up resistor of 330 Ω should be added to the common DONE line. (For Spartan-XL devices, add a 4.7K Ω pull-up resistor.) This pull-up is not needed if the DriveDONE attribute is set. If used, DriveDONE should be selected only for the last device in the configuration chain.

xcv_12_050103

Figure 12: **Master/Slave Serial Mode Circuit Diagram**

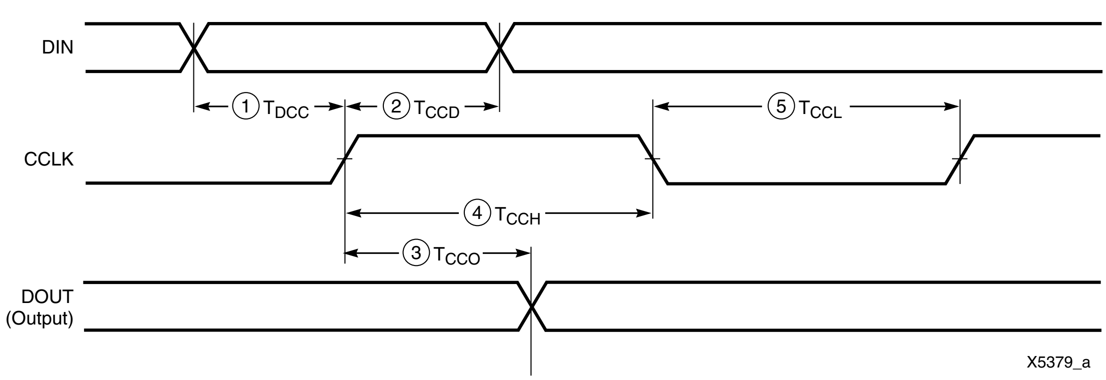


Figure 13: **Slave-Serial Mode Programming Switching Characteristics**

3. At the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this has happened.
4. Repeat steps 2 and 3 until all the data has been sent.
5. De-assert $\overline{CS}$ and $\overline{WRITE}$.

A flowchart for the write operation appears in Figure 17. Note that if CCLK is slower than f_{CCNH}, the FPGA never asserts BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

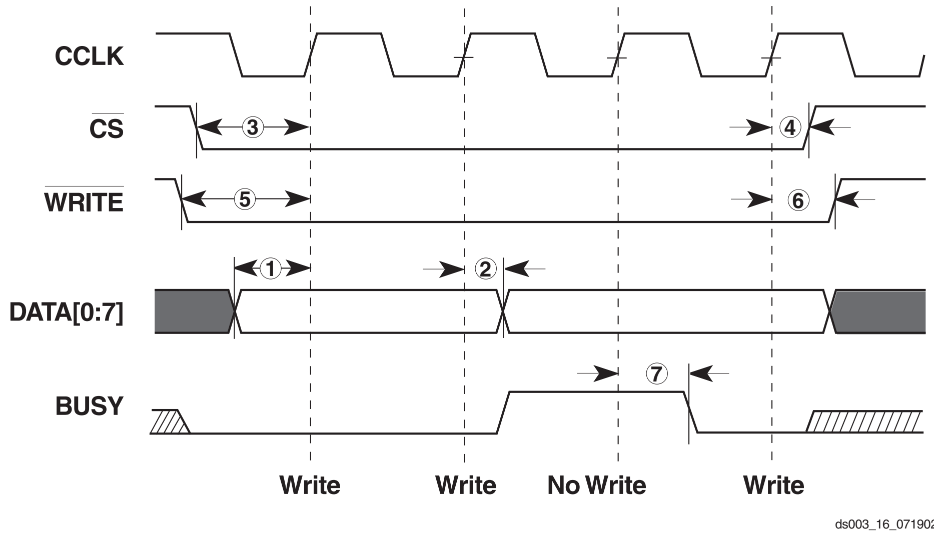


Figure 16: **Write Operations**

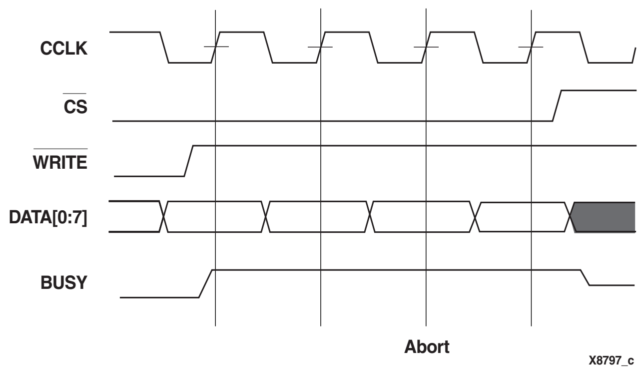


Figure 18: **SelectMAP Write Abort Waveforms**

Boundary-Scan Mode

In the boundary-scan mode, configuration is done through the IEEE 1149.1 Test Access Port. Note that the PROGRAM pin must be pulled High prior to reconfiguration. A Low on the PROGRAM pin resets the TAP controller and no JTAG operations can be performed.

Configuration through the TAP uses the CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port (when using TCK as a start-up clock).

1. Load the CFG_IN instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the JSTART instruction into IR
6. Enter the SDR state
7. Clock TCK through the startup sequence
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode is selected by a <101> or 001> on the mode pins (M2, M1, M0). For details on TAP characteristics, refer to XAPP139.

Configuration Sequence

The configuration of Virtex devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user, as described below. The configuration process can also be initiated by asserting PROGRAM. The end of the memory-clearing phase is signalled by INIT going High, and the completion of the entire process is signalled by DONE going High.

The power-up timing of configuration signals is shown in Figure 19. The corresponding timing characteristics are listed in Table 10.

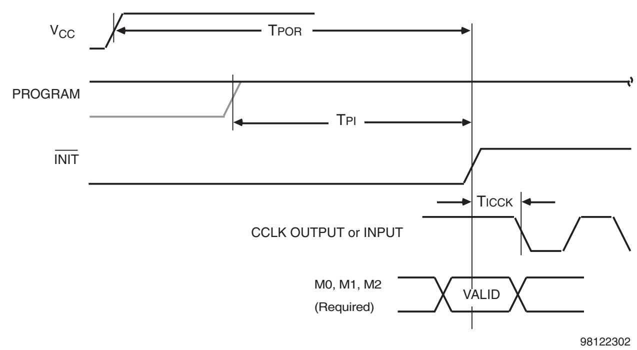


Figure 19: **Power-Up Timing Configuration Signals**

Table 10: **Power-up Timing Characteristics**

Description	Symbol	Value	Units
Power-on Reset	T_{POR}	2.0	ms, max
Program Latency	T_{PL}	100.0	µs, max
CCLK (output) Delay	T_{ICCK}	0.5	µs, min
		4.0	µs, max
Program Pulse Width	$T_{PROGRAM}$	300	ns, min

Delaying Configuration

INIT can be held Low using an open-drain driver. An open-drain is required since INIT is a bidirectional open-drain pin that is held Low by the FPGA while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

Start-Up Sequence

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed. In addition, the GTS, GSR, and GWE events can be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start in synchronism. The sequence can also be paused at any stage until lock has been achieved on any or all DLLs.

Date	Version	Revision
01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
03/00	2.0	New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration.
05/00	2.1	Modified “Pins not listed...” statement. Speed grade update to Final status.
05/00	2.2	Modified Table 18.
09/00	2.3	• Added XCV400 values to table under **Minimum Clock-to-Out for Virtex Devices**. • Corrected Units column in table under **IOB Input Switching Characteristics**. • Added values to table under **CLB SelectRAM Switching Characteristics**.
10/00	2.4	• Corrected Pinout information for devices in the BG256, BG432, and BG560 packages in Table 18. • Corrected **BG256 Pin Function Diagram**.
04/01	2.5	• Revised minimums for **Global Clock Set-Up and Hold for LVTTL Standard, with DLL**. • Updated SelectMAP Write Timing Characteristics values in Table 9. • Converted file to modularized format. See the **Virtex Data Sheet** section.
07/19/01	2.6	• Made minor edits to text under **Configuration**.
07/19/02	2.7	• Made minor edit to Figure 16 and Figure 18.
09/10/02	2.8	• Added clarifications in the **Configuration**, **Boundary-Scan Mode**, and **Block SelectRAM** sections. Revised Figure 17.
12/09/02	2.8.1	• Added clarification in the **Boundary Scan** section. • Corrected number of buffered Hex lines listed in **General Purpose Routing** section.
03/01/13	4.0	The products listed in this data sheet are obsolete. See **XCN10016** for further information.

Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

- DS003-1, Virtex 2.5V FPGAs:
  Introduction and Ordering Information (Module 1)
- DS003-2, Virtex 2.5V FPGAs:
  Functional Description (Module 2)
- DS003-3, Virtex 2.5V FPGAs:
  DC and Switching Characteristics (Module 3)
- DS003-4, Virtex 2.5V FPGAs:
  Pinout Tables (Module 4)

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Description	Symbol	Standard (1)	Speed Grade				Units
			Min	-6	-5	-4	
Output Delay Adjustments							
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T_{OLVTTL_S2}	LVTTL, Slow, 2 mA	4.2	14.7	15.8	17.0	ns
	T_{OLVTTL_S4}	4 mA	2.5	7.5	8.0	8.6	ns
	T_{OLVTTL_S6}	6 mA	1.8	4.8	5.1	5.6	ns
	T_{OLVTTL_S8}	8 mA	1.2	3.0	3.3	3.5	ns
	T_{OLVTTL_S12}	12 mA	1.0	1.9	2.1	2.2	ns
	T_{OLVTTL_S16}	16 mA	0.9	1.7	1.9	2.0	ns
	T_{OLVTTL_S24}	24 mA	0.8	1.3	1.4	1.6	ns
	T_{OLVTTL_F2}	LVTTL, Fast, 2mA	1.9	13.1	14.0	15.1	ns
	T_{OLVTTL_F4}	4 mA	0.7	5.3	5.7	6.1	ns
	T_{OLVTTL_F6}	6 mA	0.2	3.1	3.3	3.6	ns
	T_{OLVTTL_F8}	8 mA	0.1	1.0	1.1	1.2	ns
	T_{OLVTTL_F12}	12 mA	0	0	0	0	ns
	T_{OLVTTL_F16}	16 mA	–0.10	–0.05	–0.05	–0.05	ns
	T_{OLVTTL_F24}	24 mA	–0.10	–0.20	–0.21	–0.23	ns
	$T_{OLVCMOS2}$	LVCMOS2	0.10	0.10	0.11	0.12	ns
	T_{OPCI33_3}	PCI, 33 MHz, 3.3 V	0.50	2.3	2.5	2.7	ns
	T_{OPCI33_5}	PCI, 33 MHz, 5.0 V	0.40	2.8	3.0	3.3	ns
	T_{OPCI66_3}	PCI, 66 MHz, 3.3 V	0.10	–0.40	–0.42	–0.46	ns
	T_{OGTL}	GTL	0.6	0.50	0.54	0.6	ns
	T_{OGTLP}	GTL+	0.7	0.8	0.9	1.0	ns
	T_{OHSTL_I}	HSTL I	0.10	–0.50	–0.53	–0.5	ns
	T_{OHSTL_III}	HSTL III	–0.10	–0.9	–0.9	–1.0	ns
	T_{OHSTL_IV}	HSTL IV	–0.20	–1.0	–1.0	–1.1	ns
	T_{OSSTL2_I}	SSTL2 I	–0.10	–0.50	–0.53	–0.5	ns
	T_{OSSLT2_II}	SSTL2 II	–0.20	–0.9	–0.9	–1.0	ns
	T_{OSSTL3_I}	SSTL3 I	–0.20	–0.50	–0.53	–0.5	ns
	T_{OSSTL3_II}	SSTL3 II	–0.30	–1.0	–1.0	–1.1	ns
	T_{OCTT}	CTT	0	–0.6	–0.6	–0.6	ns
	T_{OAGP}	AGP	0	–0.9	–0.9	–1.0	ns

Notes:
1. Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see Table 2 and Table 3.

Clock Distribution Guidelines

Description	Device	Symbol	Speed Grade			Units
			-6	-5	-4	
Global Clock Skew[1]						
Global Clock Skew between IOB Flip-flops	XCV50	$T_{GSKEWIOB}$	0.10	0.12	0.14	ns, max
	XCV100		0.12	0.13	0.15	ns, max
	XCV150		0.12	0.13	0.15	ns, max
	XCV200		0.13	0.14	0.16	ns, max
	XCV300		0.14	0.16	0.18	ns, max
	XCV400		0.13	0.13	0.14	ns, max
	XCV600		0.14	0.15	0.17	ns, max
	XCV800		0.16	0.17	0.20	ns, max
	XCV1000		0.20	0.23	0.25	ns, max

Notes:
1. These clock-skew delays are provided for guidance only. They reflect the delays encountered in a typical design under worst-case conditions. Precise values for a particular design are provided by the timing analyzer.

Clock Distribution Switching Characteristics

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
GCLK IOB and Buffer						
Global Clock PAD to output.	T_{GPIO}	0.33	0.7	0.8	0.9	ns, max
Global Clock Buffer I input to O output	T_{GIO}	0.34	0.7	0.8	0.9	ns, max

CLB SelectRAM Switching Characteristics

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Sequential Delays						
Clock CLK to X/Y outputs (WE active) 16 x 1 mode	$T_{SHCKO16}$	1.2	2.3	2.6	3.0	ns, max
Clock CLK to X/Y outputs (WE active) 32 x 1 mode	$T_{SHCKO32}$	1.2	2.7	3.1	3.5	ns, max
Shift-Register Mode						
Clock CLK to X/Y outputs	T_{REG}	1.2	3.7	4.1	4.7	ns, max
Setup and Hold Times before/after Clock CLK[1]	Setup Time / Hold Time					
F/G address inputs	T_{AS}/T_{AH}	0.25 / 0	0.5 / 0	0.6 / 0	0.7 / 0	ns, min
BX/BY data inputs (DIN)	T_{DS}/T_{DH}	0.34 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
CE input (WE)	T_{WS}/T_{WH}	0.38 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
Shift-Register Mode						
BX/BY data inputs (DIN)	T_{SHDICK}	0.34	0.7	0.8	0.9	ns, min
CE input (WS)	T_{SHCECK}	0.38	0.8	0.9	1.0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{WPH}	1.2	2.4	2.7	3.1	ns, min
Minimum Pulse Width, Low	T_{WPL}	1.2	2.4	2.7	3.1	ns, min
Minimum clock period to meet address write cycle time	T_{WC}	2.4	4.8	5.4	6.2	ns, min
Shift-Register Mode						
Minimum Pulse Width, High	T_{SRPH}	1.2	2.4	2.7	3.1	ns, min
Minimum Pulse Width, Low	T_{SRPL}	1.2	2.4	2.7	3.1	ns, min

Notes:
1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Description	Symbol	Speed Grade						Units
		-6		-5		-4		
		Min	Max	Min	Max	Min	Max	
Input Clock Frequency (CLKDLLHF)	FCLKINHF	60	200	60	180	60	180	MHz
Input Clock Frequency (CLKDLL)	FCLKINLF	25	100	25	90	25	90	MHz
Input Clock Pulse Width (CLKDLLHF)	$T_{DLLPWHF}$	2.0	-	2.4	-	2.4	-	ns
Input Clock Pulse Width (CLKDLL)	$T_{DLLPWLF}$	2.5	-	3.0		3.0	-	ns

Notes:
1. All specifications correspond to Commercial Operating Temperatures (0°C to + 85°C).

DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

Description	Symbol	F_{CLKIN}	CLKDLLHF		CLKDLL		Units
			Min	Max	Min	Max	
Input Clock Period Tolerance	T_{IPTOL}		-	1.0	-	1.0	ns
Input Clock Jitter Tolerance (Cycle to Cycle)	T_{IJITCC}		-	± 150	-	± 300	ps
Time Required for DLL to Acquire Lock	T_{LOCK}	> 60 MHz	-	20	-	20	µs
		50 - 60 MHz	-	-	-	25	µs
		40 - 50 MHz	-	-	-	50	µs
		30 - 40 MHz	-	-	-	90	µs
		25 - 30 MHz	-	-	-	120	µs
Output Jitter (cycle-to-cycle) for any DLL Clock Output(1)	T_{OJITCC}			± 60		± 60	ps
Phase Offset between CLKIN and CLKO(2)	T_{PHIO}			± 100		± 100	ps
Phase Offset between Clock Outputs on the DLL(3)	T_{PHOO}			± 140		± 140	ps
Maximum Phase Difference between CLKIN and CLKO(4)	T_{PHIOM}			± 160		± 160	ps
Maximum Phase Difference between Clock Outputs on the DLL(5)	T_{PHOOM}			± 200		± 200	ps

Notes:
1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* Output Jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN an CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase DIfference between Clock Outputs on the DLL** is the sum of Output JItter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges sue to DLL alone (*excluding* input clock jitter).
6. All specifications correspond to Commercial Operating Temperatures (0°C to +85°C).

Date	Version	Revision
01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
03/00	2.0	New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration.
05/00	2.1	Modified "Pins not listed..." statement. Speed grade update to Final status.
05/00	2.2	Modified Table 18.
09/00	2.3	• Added XCV400 values to table under **Minimum Clock-to-Out for Virtex Devices**. • Corrected Units column in table under **IOB Input Switching Characteristics**. • Added values to table under **CLB SelectRAM Switching Characteristics**.
10/00	2.4	• Corrected Pinout information for devices in the BG256, BG432, and BG560 packages in Table 18. • Corrected **BG256 Pin Function Diagram**.
04/02/01	2.5	• Revised minimums for **Global Clock Set-Up and Hold for LVTTL Standard, with DLL**. • Converted file to modularized format. See the **Virtex Data Sheet** section.
04/19/01	2.6	• Clarified TIOCKP and TIOCKON **IOB Output Switching Characteristics** descriptors.
07/19/01	2.7	• Under **Absolute Maximum Ratings**, changed (T_{SOL}) to 220 °C.
07/26/01	2.8	• Removed T_{SOL} parameter and added footnote to **Absolute Maximum Ratings** table.
10/29/01	2.9	• Updated the speed grade designations used in data sheets, and added Table 1, which shows the current speed grade designation for each device.
02/01/02	3.0	• Added footnote to **DC Input and Output Levels** table.
07/19/02	3.1	• Removed mention of MIL-M-38510/605 specification. • Added link to xapp158 from the **Power-On Power Supply Requirements** section.
09/10/02	3.2	• Added Clock CLK to **IOB Input Switching Characteristics** and **IOB Output Switching Characteristics**.
03/01/13	4.0	The products listed in this data sheet are obsolete. See XCN10016 for further information.

Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

- DS003-1, Virtex 2.5V FPGAs: Introduction and Ordering Information (Module 1)
- DS003-2, Virtex 2.5V FPGAs: Functional Description (Module 2)
- DS003-3, Virtex 2.5V FPGAs: DC and Switching Characteristics (Module 3)
- DS003-4, Virtex 2.5V FPGAs: Pinout Tables (Module 4)

Table 2: **Virtex Pinout Tables (Chip-Scale and QFP Packages) *(Continued)***

Pin Name	Device	CS144	TQ144	PQ/HQ240
V_{CCO}	All	Banks 0 and 1: A2, A13, D7 Banks 2 and 3: B12, G11, M13 Banks 4 and 5: N1, N7, N13 Banks 6 and 7: B2, G2, M2	No I/O Banks in this package: 1, 17, 37, 55, 73, 92, 109, 128	No I/O Banks in this package: 15, 30, 44, 61, 76, 90, 105, 121, 136, 150, 165, 180, 197, 212, 226, 240
V_{REF}, Bank 0 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	C4, D6	5, 13	218, 232
	XCV100/150	... + B4	... + 7	... + 229
	XCV200/300	N/A	N/A	... + 236
	XCV400	N/A	N/A	... + 215
	XCV600	N/A	N/A	... + 230
	XCV800	N/A	N/A	... + 222
V_{REF}, Bank 1 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	A10, B8	22, 30	191, 205
	XCV100/150	... + D9	... + 28	... + 194
	XCV200/300	N/A	N/A	... + 187
	XCV400	N/A	N/A	... + 208
	XCV600	N/A	N/A	... + 193
	XCV800	N/A	N/A	... + 201
V_{REF}, Bank 2 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	D11, F10	42, 50	157, 171
	XCV100/150	... + D13	... + 44	... + 168
	XCV200/300	N/A	N/A	... + 175
	XCV400	N/A	N/A	... + 154
	XCV600	N/A	N/A	... + 169
	XCV800	N/A	N/A	... + 161

Table 2: **Virtex Pinout Tables (Chip-Scale and QFP Packages) *(Continued)***

Pin Name	Device	CS144	TQ144	PQ/HQ240
V_{REF}, Bank 3 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	H11, K12	60, 68	130, 144
	XCV100/150	... + J10	... + 66	... + 133
	XCV200/300	N/A	N/A	... + 126
	XCV400	N/A	N/A	... + 147
	XCV600	N/A	N/A	... + 132
	XCV800	N/A	N/A	... + 140
V_{REF}, Bank 4 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	L8, L10	79, 87	97, 111
	XCV100/150	... + N10	... + 81	... + 108
	XCV200/300	N/A	N/A	... + 115
	XCV400	N/A	N/A	... + 94
	XCV600	N/A	N/A	... + 109
	XCV800	N/A	N/A	... + 101
V_{REF}, Bank 5 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	L4, L6	96, 104	70, 84
	XCV100/150	... + N4	... + 102	... + 73
	XCV200/300	N/A	N/A	... + 66
	XCV400	N/A	N/A	... + 87
	XCV600	N/A	N/A	... + 72
	XCV800	N/A	N/A	... + 80

Table 3: **Virtex Pinout Tables (BGA)** ***(Continued)***

Pin Name	Device	BG256	BG352	BG432	BG560
V_{CCINT} **Notes:** • Superset includes all pins, including the ones in **bold** type. Subset excludes pins in **bold** type. • In BG352, for XCV300 all the V_{CCINT} pins in the superset must be connected. For XCV150/200, V_{CCINT} pins in the subset must be connected, and pins in **bold** type can be left unconnected (these unconnected pins cannot be used as user I/O.) • In BG432, for XCV400/600/800 all V_{CCINT} pins in the superset must be connected. For XCV300, V_{CCINT} pins in the subset must be connected, and pins in **bold** type can be left unconnected (these unconnected pins cannot be used as user I/O.) • In BG560, for XCV800/1000 all V_{CCINT} pins in the superset must be connected. For XCV400/600, V_{CCINT} pins in the subset must be connected, and pins in **bold** type can be left unconnected (these unconnected pins cannot be used as user I/O.)	XCV50/100	C10, D6, D15, F4, F17, L3, L18, R4, R17, U6, U15, V10	N/A	N/A	N/A
	XCV150/200/300	Same as above	A20, C14, D10, J24, K4, P2, P25, V24, W2, AC10, AE14, AE19, **B16, D12, L1, L25, R23, T1, AF11, AF16**	A10, A17, B23, C14, C19, K3, K29, N2, N29, T1, T29, W2, W31, AB2, AB30, AJ10, AJ16, AK13, AK19, AK22, **B26, C7, F1, F30, AE29, AF1, AH8, AH24**	N/A
	XCV400/600/800/1000	N/A	N/A	Same as above	A21, B14, B18, B28, C24, E9, E12, F2, H30, J1, K32, N1, N33, U5, U30, Y2, Y31, AD2, AD32, AG3, AG31, AK8, AK11, AK17, AK20, AL14, AL27, AN25, **B12, C22, M3, N29, AB2, AB32, AJ13, AL22**
V_{CCO}, Bank 0	All	D7, D8	A17, B25, D19	A21, C29, D21	A22, A26, A30, B19, B32
V_{CCO}, Bank 1	All	D13, D14	A10, D7, D13	A1, A11, D11	A10, A16, B13, C3, E5
V_{CCO}, Bank 2	All	G17, H17	B2, H4, K1	C3, L1, L4	B2, D1, H1, M1, R2
V_{CCO}, Bank 3	All	N17, P17	P4, U1, Y4	AA1, AA4, AJ3	V1, AA2, AD1, AK1, AL2
V_{CCO}, Bank 4	All	U13, U14	AC8, AE2, AF10	AH11, AL1, AL11	AM2, AM15, AN4, AN8, AN12
V_{CCO}, Bank 5	All	U7, U8	AC14, AC20, AF17	AH21, AJ29, AL21	AL31, AM21, AN18, AN24, AN30
V_{CCO}, Bank 6	All	N4, P4	U26, W23, AE25	AA28, AA31, AL31	W32, AB33, AF33, AK33, AM32

Table 4: **Virtex Pinout Tables (Fine-Pitch BGA)**

Pin Name	Device	FG256	FG456	FG676	FG680
GCK0	All	N8	W12	AA14	AW19
GCK1	All	R8	Y11	AB13	AU22
GCK2	All	C9	A11	C13	D21
GCK3	All	B8	C11	E13	A20
M0	All	N3	AB2	AD4	AT37
M1	All	P2	U5	W7	AU38
M2	All	R3	Y4	AB6	AT35
CCLK	All	D15	B22	D24	E4
PROGRAM	All	P15	W20	AA22	AT5
DONE	All	R14	Y19	AB21	AU5
INIT	All	N15	V19	Y21	AU2
BUSY/DOUT	All	C15	C21	E23	E3
D0/DIN	All	D14	D20	F22	C2
D1	All	E16	H22	K24	P4
D2	All	F15	H20	K22	P3
D3	All	G16	K20	M22	R1
D4	All	J16	N22	R24	AD3
D5	All	M16	R21	U23	AG2
D6	All	N16	T22	V24	AH1
D7	All	N14	Y21	AB23	AR4
WRITE	All	C13	A20	C22	B4
CS	All	B13	C19	E21	D5
TDI	All	A15	B20	D22	B3
TDO	All	B14	A21	C23	C4
TMS	All	D3	D3	F5	E36
TCK	All	C4	C4	E6	C36
DXN	All	R4	Y5	AB7	AV37
DXP	All	P4	V6	Y8	AU35

Table 4: **Virtex Pinout Tables (Fine-Pitch BGA)** ***(Continued)***

<table>
<tr><th>Pin Name</th><th>Device</th><th>FG256</th><th>FG456</th><th>FG676</th><th>FG680</th></tr>
<tr><td rowspan="7">V_{REF}, Bank 1
(VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)
Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.</td><td>XCV50</td><td>B9, C11</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>XCV100/150</td><td>... + E11</td><td>A18, B13, E14</td><td>N/A</td><td>N/A</td></tr>
<tr><td>XCV200/300</td><td>... + A14</td><td>... + A19</td><td>N/A</td><td>N/A</td></tr>
<tr><td>XCV400</td><td>N/A</td><td>N/A</td><td>A14, C20, C21, D15, G16</td><td>N/A</td></tr>
<tr><td>XCV600</td><td>N/A</td><td>N/A</td><td>... + B19</td><td>B6, B8, B18, D11, D13, D17</td></tr>
<tr><td>XCV800</td><td>N/A</td><td>N/A</td><td>... + A17</td><td>... + B14</td></tr>
<tr><td>XCV1000</td><td>N/A</td><td>N/A</td><td>N/A</td><td>... + B5</td></tr>
<tr><td rowspan="7">V_{REF}, Bank 2
(V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)
Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.</td><td>XCV50</td><td>F13, H13</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>XCV100/150</td><td>... + F14</td><td>F21, H18, K21</td><td>N/A</td><td>N/A</td></tr>
<tr><td>XCV200/300</td><td>... + E13</td><td>... + D22</td><td>N/A</td><td>N/A</td></tr>
<tr><td>XCV400</td><td>N/A</td><td>N/A</td><td>F24, H23, K20, M23, M26</td><td>N/A</td></tr>
<tr><td>XCV600</td><td>N/A</td><td>N/A</td><td>... + G26</td><td>G1, H4, J1, L2, V5, W3</td></tr>
<tr><td>XCV800</td><td>N/A</td><td>N/A</td><td>... + K25</td><td>... + N1</td></tr>
<tr><td>XCV1000</td><td>N/A</td><td>N/A</td><td>N/A</td><td>... + D2</td></tr>
<tr><td rowspan="7">V_{REF}, Bank 3
(V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)
Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.</td><td>XCV50</td><td>K16, L14</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>XCV100/150</td><td>... + L13</td><td>N21, R19, U21</td><td>N/A</td><td>N/A</td></tr>
<tr><td>XCV200/300</td><td>... + M13</td><td>... + U20</td><td>N/A</td><td>N/A</td></tr>
<tr><td>XCV400</td><td>N/A</td><td>N/A</td><td>R23, R25, U21, W22, W23</td><td>N/A</td></tr>
<tr><td>XCV600</td><td>N/A</td><td>N/A</td><td>... + W26</td><td>AC1, AJ2, AK3, AL4, AR1, Y1</td></tr>
<tr><td>XCV800</td><td>N/A</td><td>N/A</td><td>... + U25</td><td>... + AF3</td></tr>
<tr><td>XCV1000</td><td>N/A</td><td>N/A</td><td>N/A</td><td>... + AP4</td></tr>
</table>

Table 4: **Virtex Pinout Tables (Fine-Pitch BGA)** ***(Continued)***

Pin Name	Device	FG256	FG456	FG676	FG680
V_{REF}, Bank 4 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	P9, T12	N/A	N/A	N/A
	XCV100/150	... + T11	AA13, AB16, AB19	N/A	N/A
	XCV200/300	... + R13	... + AB20	N/A	N/A
	XCV400	N/A	N/A	AC15, AD18, AD21, AD22, AF15	N/A
	XCV600	N/A	N/A	... + AF20	AT19, AU7, AU17, AV8, AV10, AW11
	XCV800	N/A	N/A	... + AF17	... + AV14
	XCV1000	N/A	N/A	N/A	... + AU6
V_{REF}, Bank 5 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	T4, P8	N/A	N/A	N/A
	XCV100/150	... + R5	W8, Y10, AA5	N/A	N/A
	XCV200/300	... + T2	... + Y6	N/A	N/A
	XCV400	N/A	N/A	AA10, AB8, AB12, AC7, AF12	N/A
	XCV600	N/A	N/A	... + AF8	AT27, AU29, AU31, AV35, AW21, AW23
	XCV800	N/A	N/A	... + AE10	... + AT25
	XCV1000	N/A	N/A	N/A	... + AV36
V_{REF}, Bank 6 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	J3, N1	N/A	N/A	N/A
	XCV100/150	... + M1	N2, R4, T3	N/A	N/A
	XCV200/300	... + N2	... + Y1	N/A	N/A
	XCV400	N/A	N/A	AB3, R1, R4, U6, V5	N/A
	XCV600	N/A	N/A	... + Y1	AB35, AD37, AH39, AK39, AM39, AN36
	XCV800	N/A	N/A	... + U2	... + AE39
	XCV1000	N/A	N/A	N/A	... + AT39

TQ144 Pin Function Diagram

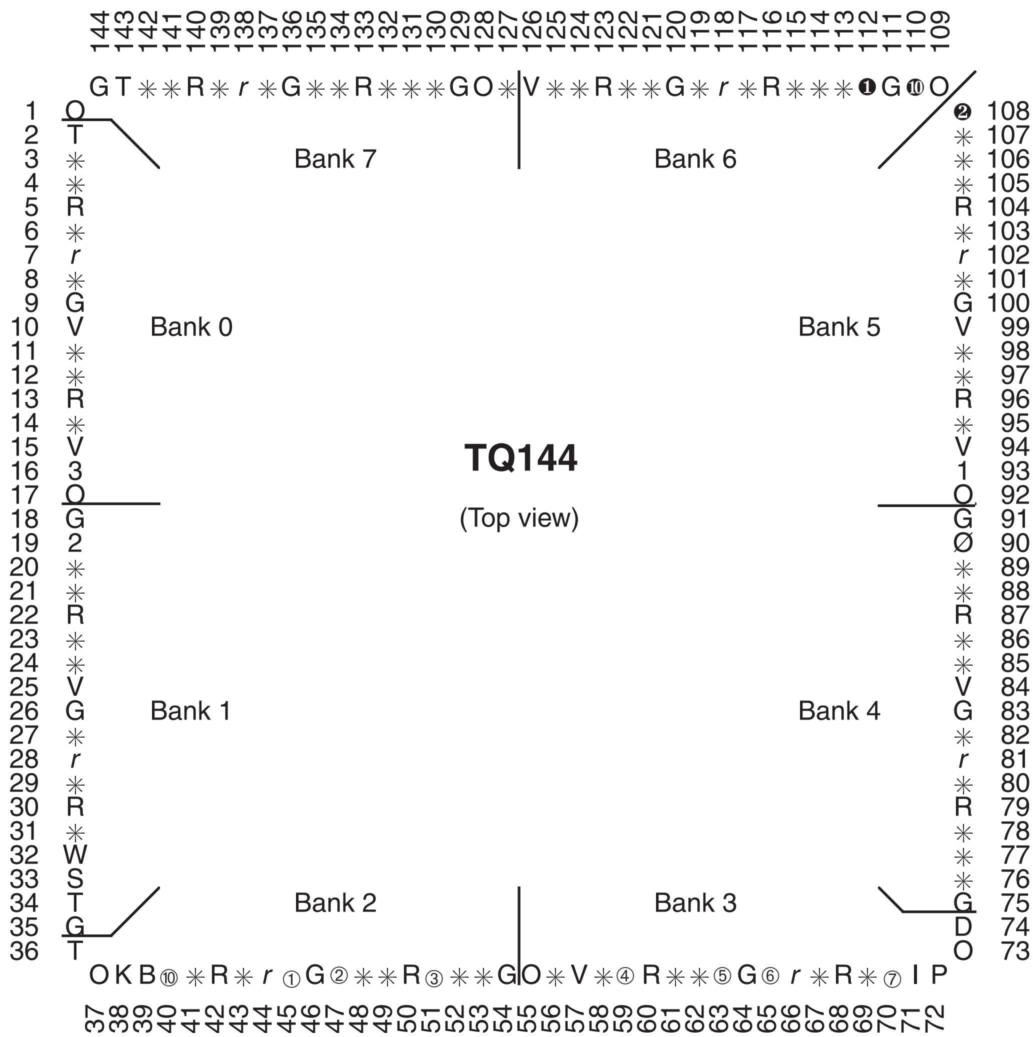


Figure 2: **TQ144 Pin Function Diagram**

BG256 Pin Function Diagram

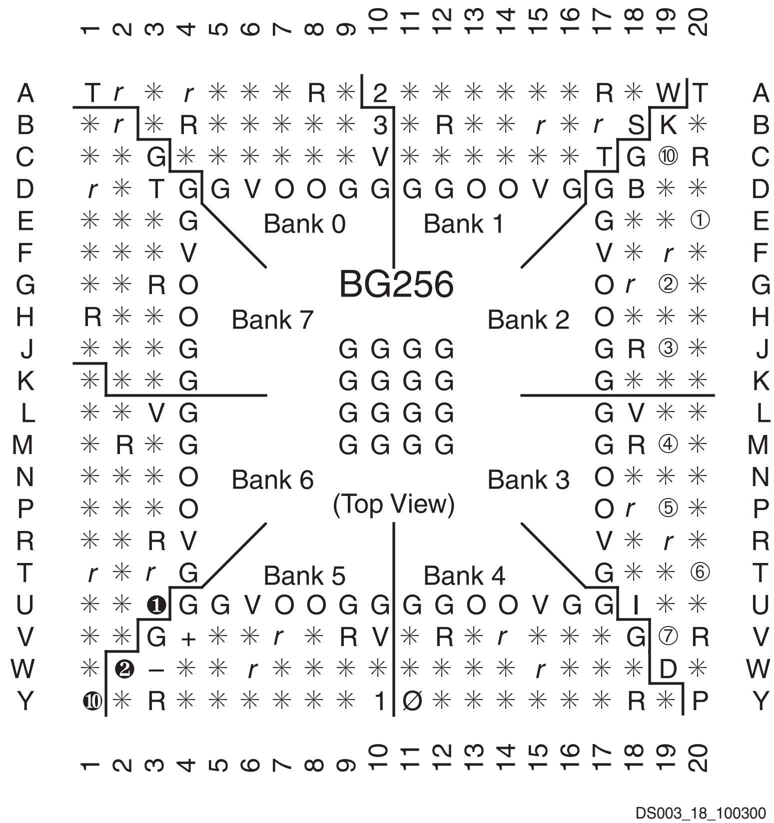


Figure 4: **BG256 Pin Function Diagram**