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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	600
Number of Logic Elements/Cells	2700
Total RAM Bits	40960
Number of I/O	166
Number of Gates	108904
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xcv100-5pq240c">https://www.e-xfl.com/product-detail/xilinx/xcv100-5pq240c</a>

### Input Path

A buffer in the Virtex IOB input path routes the input signal either directly to internal logic or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signalling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage,  $V_{REF}$ . The need to supply  $V_{REF}$  imposes constraints on which standards can be used in close proximity to each other. See [I/O Banking, page 3](#).

There are optional pull-up and pull-down resistors at each user I/O input for use after configuration. Their value is in the range 50 k $\Omega$  – 100 k $\Omega$ .

### Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flop that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signalling standards. Each output buffer can source up to 24 mA and sink up to 48mA. Drive strength and slew rate controls minimize bus transients.

In most signalling standards, the output High voltage depends on an externally supplied  $V_{CCO}$  voltage. The need to supply  $V_{CCO}$  imposes constraints on which standards can be used in close proximity to each other. See [I/O Banking, page 3](#).

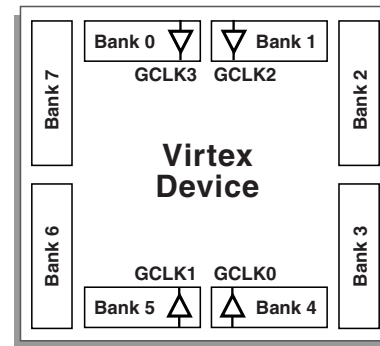
An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate  $V_{REF}$  voltage must be provided if the signalling standard requires one. The provision of this voltage must comply with the I/O banking rules.

### I/O Banking

Some of the I/O standards described above require  $V_{CCO}$  and/or  $V_{REF}$  voltages. These voltages externally and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks, as shown in [Figure 3](#). Each bank has multiple  $V_{CCO}$  pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.



X8778\_b

Figure 3: Virtex I/O Banks

Within a bank, output standards can be mixed only if they use the same  $V_{CCO}$ . Compatible standards are shown in [Table 2](#). GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on  $V_{CCO}$ .

Table 2: Compatible Output Standards

$V_{CCO}$	Compatible Standards
3.3 V	PCI, LVTTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+
2.5 V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+
1.5 V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage,  $V_{REF}$ . In this case, certain user-I/O pins are automatically configured as inputs for the  $V_{REF}$  voltage. Approximately one in six of the I/O pins in the bank assume this role.

The  $V_{REF}$  pins within a bank are interconnected internally and consequently only one  $V_{REF}$  voltage can be used within each bank. All  $V_{REF}$  pins in the bank, however, must be connected to the external voltage source for correct operation.

Within a bank, inputs that require  $V_{REF}$  can be mixed with those that do not. However, only one  $V_{REF}$  voltage can be used within a bank. Input buffers that use  $V_{REF}$  are not 5 V tolerant. LVTTTL, LVCMOS2, and PCI 33 MHz 5 V, are 5 V tolerant.

The  $V_{CCO}$  and  $V_{REF}$  pins for each bank appear in the device Pinout tables and diagrams. The diagrams also show the bank affiliation of each I/O.

Within a given package, the number of  $V_{REF}$  and  $V_{CCO}$  pins can vary depending on the size of device. In larger devices,

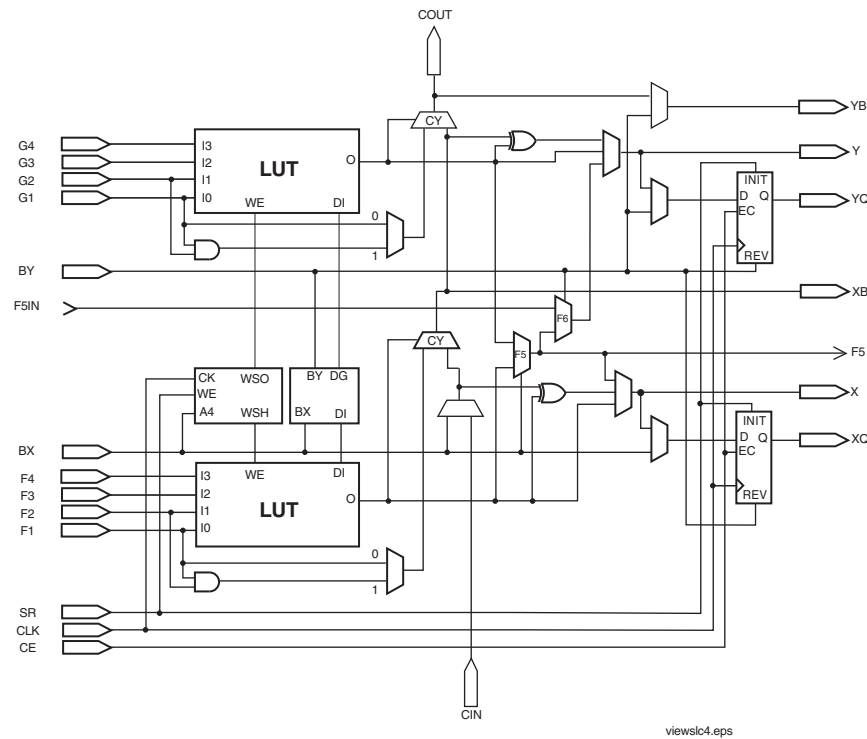


Figure 5: Detailed View of Virtex Slice

### Additional Logic

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Each CLB has four direct feedthrough paths, one per LC. These paths provide extra data input or additional local routing that does not consume logic resources.

### Arithmetic Logic

Dedicated carry logic provides fast arithmetic carry capability for high-speed arithmetic functions. The Virtex CLB supports two separate carry chains, one per Slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 1-bit full adder to be implemented within an LC. In addition, a dedicated AND gate improves the efficiency of multiplier implementation.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

### BUFTs

Each Virtex CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. See **Dedicated Routing**, page 7. Each Virtex BUFT has an independent 3-state control pin and an independent input pin.

### Block SelectRAM

Virtex FPGAs incorporate several large block SelectRAM memories. These complement the distributed LUT SelectRAMs that provide shallow RAM structures implemented in CLBs.

Block SelectRAM memory blocks are organized in columns. All Virtex devices contain two such columns, one along each vertical edge. These columns extend the full height of the chip. Each memory block is four CLBs high, and consequently, a Virtex device 64 CLBs high contains 16 memory blocks per column, and a total of 32 blocks.

**Table 3** shows the amount of block SelectRAM memory that is available in each Virtex device.

Table 3: Virtex Block SelectRAM Amounts

Device	# of Blocks	Total Block SelectRAM Bits
XCV50	8	32,768
XCV100	10	40,960
XCV150	12	49,152
XCV200	14	57,344
XCV300	16	65,536
XCV400	20	81,920
XCV600	24	98,304
XCV800	28	114,688
XCV1000	32	131,072

Each block SelectRAM cell, as illustrated in Figure 6, is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

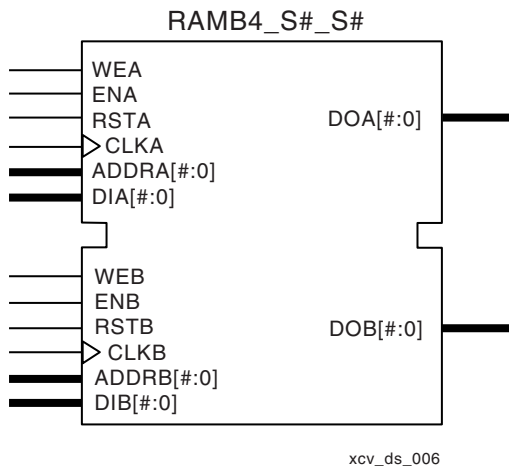


Figure 6: Dual-Port Block SelectRAM

Table 4 shows the depth and width aspect ratios for the block SelectRAM.

Table 4: Block SelectRAM Port Aspect Ratios

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

The Virtex block SelectRAM also includes dedicated routing to provide an efficient interface with both CLBs and other block SelectRAMs. Refer to XAPP130 for block SelectRAM timing waveforms.

## Programmable Routing Matrix

It is the longest delay path that limits the speed of any worst-case design. Consequently, the Virtex routing architecture and its place-and-route software were defined in a single optimization process. This joint optimization minimizes long-path delays, and consequently, yields the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

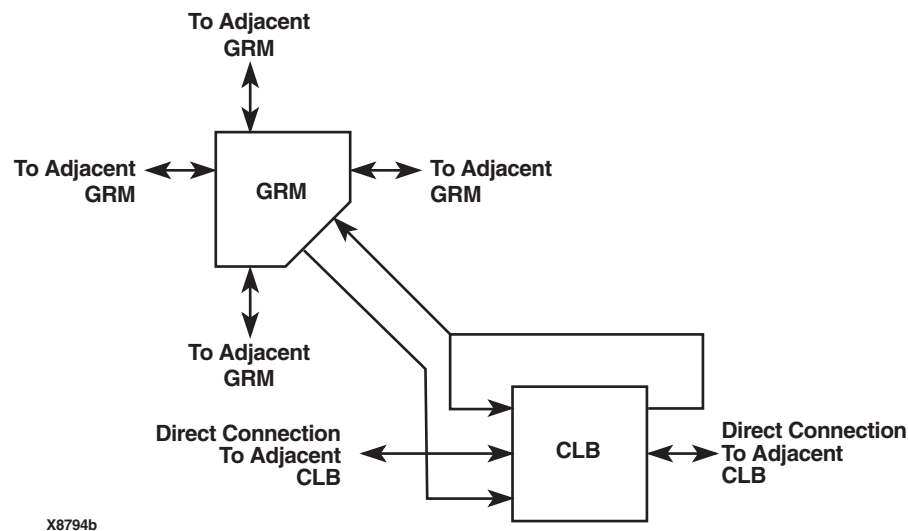


Figure 7: Virtex Local Routing

## Local Routing

The VersaBlock provides local routing resources, as shown in Figure 7, providing the following three types of connections.

- Interconnections among the LUTs, flip-flops, and GRM

- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is

selected either from these pads or from signals in the general purpose routing.



Figure 9: Global Clock Distribution Network

### Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Clock edges reach internal flip-flops one to four clock periods after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to de-skew a board level clock among multiple Virtex devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

See **DLL Timing Parameters**, page 21 of Module 3, for frequency range information.

### Boundary Scan

Virtex devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, and HIGHZ instructions. The TAP also supports two internal scan chains and configuration/readback of the device. The TAP uses dedicated package pins that always operate using LVTTTL. For TDO to operate using LVTTTL, the  $V_{CCO}$  for Bank 2 should be 3.3 V. Otherwise, TDO switches rail-to-rail between ground and  $V_{CCO}$ .

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including un-bonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections, provided the user design or application is turned off.

**Table 5** lists the boundary-scan instructions supported in Virtex FPGAs. Internal signals can be captured during EXTEST by connecting them to un-bonded or unused IOBs. They can also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Before the device is configured, all instructions except USER1 and USER2 are available. After configuration, all instructions are available. During configuration, it is recommended that those operations using the boundary-scan register (SAMPLE/PRELOAD, INTEST, EXTEST) not be performed.

## Configuration

Virtex devices are configured by loading configuration data into the internal configuration memory. Some of the pins used for this are dedicated configuration pins, while others can be re-used as general purpose inputs and outputs once configuration is complete.

The following are dedicated pins:

- Mode pins (M2, M1, M0)
- Configuration clock pin (CCLK)
- $\overline{\text{PROGRAM}}$  pin
- DONE pin
- Boundary-scan pins (TDI, TDO, TMS, TCK)

Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or it can be generated externally and provided to the FPGA as an input. The  $\overline{\text{PROGRAM}}$  pin must be pulled High prior to reconfiguration.

Note that some configuration pins can act as outputs. For correct operation, these pins can require a  $V_{\text{CCO}}$  of 3.3 V to permit LVTTTL operation. All the pins affected are in banks 2 or 3. The configuration pins needed for SelectMap (CS, Write) are located in bank 1.

Table 7: Configuration Codes

Configuration Mode	M2	M1	M0	CCLK Direction	Data Width	Serial D <sub>out</sub>	Configuration Pull-ups
Master-serial mode	0	0	0	Out	1	Yes	No
Boundary-scan mode	1	0	1	N/A	1	No	No
SelectMAP mode	1	1	0	In	8	No	No
Slave-serial mode	1	1	1	In	1	Yes	No
Master-serial mode	1	0	0	Out	1	Yes	Yes
Boundary-scan mode	0	0	1	N/A	1	No	Yes
SelectMAP mode	0	1	0	In	8	No	Yes
Slave-serial mode	0	1	1	In	1	Yes	Yes

### Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other source of serial configuration data. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

For more information on serial PROMs, see the PROM data sheet at:

<http://www.xilinx.com/bvdocs/publications/ds026.pdf>.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin. The data on the DOUT pin changes on the rising edge of CCLK.

The change of DOUT on the rising edge of CCLK differs from previous families, but does not cause a problem for

After Virtex devices are configured, unused IOBs function as 3-state OBUFTs with weak pull downs. For a more detailed description than that given below, see the XAPP138, Virtex Configuration and Readback.

## Configuration Modes

Virtex supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- SelectMAP mode
- Boundary-scan mode

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in Table 7.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected. However, it is recommended to drive the configuration mode pins externally.

mixed configuration chains. This change was made to improve serial configuration rates for Virtex-only chains.

Figure 12 shows a full master/slave system. A Virtex device in slave-serial mode should be connected as shown in the third device from the left.

Slave-serial mode is selected by applying <111> or <011> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave-serial the default mode if the pins are left unconnected. However, it is recommended to drive the configuration mode pins externally. Figure 13 shows slave-serial mode programming switching characteristics.

Table 8 provides more detail about the characteristics shown in Figure 13. Configuration must be delayed until the  $\overline{\text{INIT}}$  pins of all daisy-chained FPGAs are High.



## Master-Serial Mode

In master-serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM that feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge.

The interface is identical to slave-serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration. Switching to a lower frequency is prohibited.

The CCLK frequency is set using the ConfigRate option in the bitstream generation software. The maximum CCLK frequency that can be selected is 60 MHz. When selecting a CCLK frequency, ensure that the serial PROM and any

daisy-chained FPGAs are fast enough to support the clock rate.

On power-up, the CCLK frequency is 2.5 MHz. This frequency is used until the ConfigRate bits have been loaded when the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz.

Figure 12 shows a full master/slave system. In this system, the left-most device operates in master-serial mode. The remaining devices operate in slave-serial mode. The SPROM RESET pin is driven by INIT, and the CE input is driven by DONE. There is the potential for contention on the DONE pin, depending on the start-up sequence options chosen.

Figure 14 shows the timing of master-serial configuration. Master-serial mode is selected by a <000> or <100> on the mode pins (M2, M1, M0). Table 8 shows the timing information for Figure 14.

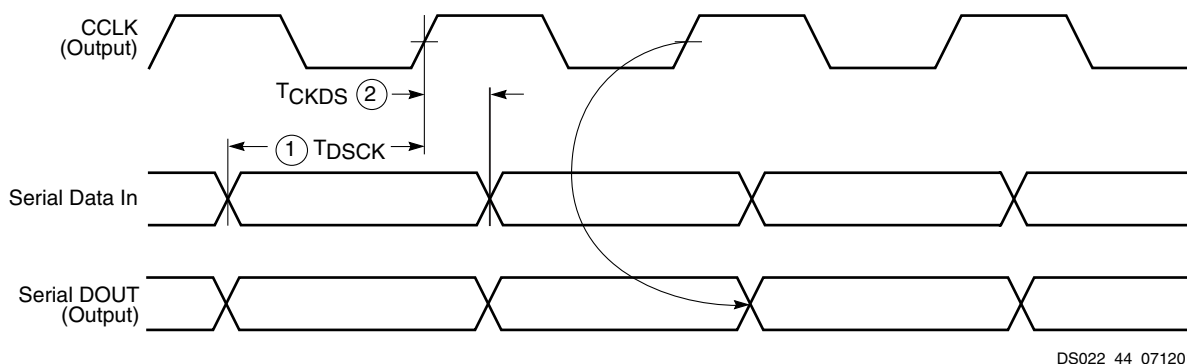


Figure 14: Master-Serial Mode Programming Switching Characteristics

At power-up,  $V_{CC}$  must rise from 1.0 V to  $V_{CC}$  min in less than 50 ms, otherwise delay configuration by pulling PROGRAM Low until  $V_{CC}$  is valid.

The sequence of operations necessary to configure a Virtex FPGA serially appears in Figure 15.

## SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the FPGA with a BUSY flag controlling the flow of data.

An external data source provides a byte stream, CCLK, a Chip Select ( $\overline{CS}$ ) signal and a Write signal ( $\overline{WRITE}$ ). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

Data can also be read using the SelectMAP mode. If  $\overline{WRITE}$  is not asserted, configuration data is read out of the FPGA as part of a readback operation.

In the SelectMAP mode, multiple Virtex devices can be chained in parallel. DATA pins (D7:D0), CCLK,  $\overline{WRITE}$ ,  $\overline{BUSY}$ ,  $\overline{PROGRAM}$ ,  $\overline{DONE}$ , and  $\overline{INIT}$  can be connected in parallel between all the FPGAs. Note that the data is organized with the MSB of each byte on pin D0 and the LSB of each byte on D7. The  $\overline{CS}$  pins are kept separate, insuring that each FPGA can be selected individually.  $\overline{WRITE}$  should be Low before loading the first bitstream and returned High after the last device has been programmed. Use  $\overline{CS}$  to select the appropriate FPGA for loading the bitstream and sending the configuration data. At the end of the bitstream, deselect the loaded device and select the next target FPGA by setting its  $\overline{CS}$  pin High. A free-running oscillator or other externally generated signal can be used for CCLK. The  $\overline{BUSY}$  signal can be ignored for frequencies below 50 MHz. For details about frequencies above 50 MHz, see XAPP138, Virtex Configuration and Readback. Once all the devices have been programmed, the  $\overline{DONE}$  pin goes High.

## Data Stream Format

Virtex devices are configured by sequentially loading frames of data. Table 11 lists the total number of bits required to configure each device. For more detailed information, see application note XAPP151 “Virtex Configuration Architecture Advanced Users Guide”.

Table 11: Virtex Bit-Stream Lengths

Device	# of Configuration Bits
XCV50	559,200
XCV100	781,216
XCV150	1,040,096
XCV200	1,335,840
XCV300	1,751,808
XCV400	2,546,048
XCV600	3,607,968
XCV800	4,715,616
XCV1000	6,127,744

## Readback

The configuration data stored in the Virtex configuration memory can be readback for verification. Along with the configuration data it is possible to readback the contents all flip-flops/latches, LUTRAMs, and block RAMs. This capability is used for real-time debugging.

For more detailed information, see Application Note XAPP138: *Virtex FPGA Series Configuration and Readback*, available online at [www.xilinx.com](http://www.xilinx.com).

## Revision History

Date	Version	Revision
11/98	1.0	Initial Xilinx release.
01/99	1.2	Updated package drawings and specs.
02/99	1.3	Update of package drawings, updated specifications.
05/99	1.4	Addition of package drawings and specifications.
05/99	1.5	Replaced FG 676 & FG680 package drawings.
07/99	1.6	Changed Boundary Scan Information and changed Figure 11, Boundary Scan Bit Sequence. Updated IOB Input & Output delays. Added Capacitance info for different I/O Standards. Added 5 V tolerant information. Added DLL Parameters and waveforms and new Pin-to-pin Input and Output Parameter tables for Global Clock Input to Output and Setup and Hold. Changed Configuration Information including Figures 12, 14, 17 & 19. Added device-dependent listings for quiescent currents ICCINTQ and ICCOQ. Updated IOB Input and Output Delays based on default standard of LVTTTL, 12 mA, Fast Slew Rate. Added IOB Input Switching Characteristics Standard Adjustments.
09/99	1.7	Speed grade update to preliminary status, Power-on specification and Clock-to-Out Minimums additions, “0” hold time listing explanation, quiescent current listing update, and Figure 6 ADDRA input label correction. Added T <sub>IJITCC</sub> parameter, changed T <sub>OJIT</sub> to T <sub>OPHASE</sub> .
01/00	1.8	Update to speed.txt file 1.96. Corrections for CRs 111036, 111137, 112697, 115479, 117153, 117154, and 117612. Modified notes for Recommended Operating Conditions (voltage and temperature). Changed Bank information for V <sub>CCO</sub> in CS144 package on p.43.



## Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device<sup>(1)</sup> from 0 V. The current is highest at the fastest suggested ramp rate (0 V to nominal voltage in 2 ms) and is lowest at the slowest allowed ramp rate (0 V to nominal voltage in 50 ms). For more details on power supply requirements, see Application Note XAPP158 on [www.xilinx.com](http://www.xilinx.com).

Product	Description <sup>(2)</sup>	Current Requirement <sup>(1,3)</sup>
Virtex Family, Commercial Grade	Minimum required current supply	500 mA
Virtex Family, Industrial Grade	Minimum required current supply	2 A

### Notes:

1. Ramp rate used for this specification is from 0 - 2.7 VDC. Peak current occurs on or near the internal power-on reset threshold of 1.0V and lasts for less than 3 ms.
2. Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
3. Larger currents can result if ramp rates are forced to be faster.

## DC Input and Output Levels

Values for  $V_{IL}$  and  $V_{IH}$  are recommended input voltages. Values for  $I_{OL}$  and  $I_{OH}$  are guaranteed output currents over the recommended operating conditions at the  $V_{OL}$  and  $V_{OH}$  test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum  $V_{CCO}$  for each standard with the respective  $V_{OL}$  and  $V_{OH}$  voltage levels shown. Other standards are sample tested.

Input/Output Standard	$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$	$I_{OH}$
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTL <sup>(1)</sup>	-0.5	0.8	2.0	5.5	0.4	2.4	24	-24
LVC MOS2	-0.5	.7	1.7	5.5	0.4	1.9	12	-12
PCI, 3.3 V	-0.5	44% $V_{CCINT}$	60% $V_{CCINT}$	$V_{CCO} + 0.5$	10% $V_{CCO}$	90% $V_{CCO}$	Note 2	Note 2
PCI, 5.0 V	-0.5	0.8	2.0	5.5	0.55	2.4	Note 2	Note 2
GTL	-0.5	$V_{REF} - 0.05$	$V_{REF} + 0.05$	3.6	0.4	n/a	40	n/a
GTL+	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.6	n/a	36	n/a
HSTL I <sup>(3)</sup>	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	8	-8
HSTL III	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	24	-8
HSTL IV	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	48	-8
SSTL3 I	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.6$	$V_{REF} + 0.6$	8	-8
SSTL3 II	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.8$	$V_{REF} + 0.8$	16	-16
SSTL2 I	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.61$	$V_{REF} + 0.61$	7.6	-7.6
SSTL2 II	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.80$	$V_{REF} + 0.80$	15.2	-15.2
CTT	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
AGP	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	10% $V_{CCO}$	90% $V_{CCO}$	Note 2	Note 2

### Notes:

1.  $V_{OL}$  and  $V_{OH}$  for lower drive currents are sample tested.
2. Tested according to the relevant specifications.
3. DC input and output levels for HSTL18 (HSTL I/O standard with  $V_{CCO}$  of 1.8 V) are provided in an HSTL white paper on [www.xilinx.com](http://www.xilinx.com).

### Virtex Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation net list. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Virtex devices unless otherwise noted.

### IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTTL levels. For other standards, adjust the delays with the values shown in , page 6.

Description	Device	Symbol	Speed Grade				Units
			Min	-6	-5	-4	
Propagation Delays							
Pad to I output, no delay	All	T <sub>IOPI</sub>	0.39	0.8	0.9	1.0	ns, max
Pad to I output, with delay	XCV50	T <sub>IOPID</sub>	0.8	1.5	1.7	1.9	ns, max
	XCV100		0.8	1.5	1.7	1.9	ns, max
	XCV150		0.8	1.5	1.7	1.9	ns, max
	XCV200		0.8	1.5	1.7	1.9	ns, max
	XCV300		0.8	1.5	1.7	1.9	ns, max
	XCV400		0.9	1.8	2.0	2.3	ns, max
	XCV600		0.9	1.8	2.0	2.3	ns, max
	XCV800		1.1	2.1	2.4	2.7	ns, max
	XCV1000		1.1	2.1	2.4	2.7	ns, max
Pad to output IQ via transparent latch, no delay	All	T <sub>IOPLI</sub>	0.8	1.6	1.8	2.0	ns, max
Pad to output IQ via transparent latch, with delay	XCV50	T <sub>IOPLID</sub>	1.9	3.7	4.2	4.8	ns, max
	XCV100		1.9	3.7	4.2	4.8	ns, max
	XCV150		2.0	3.9	4.3	4.9	ns, max
	XCV200		2.0	4.0	4.4	5.1	ns, max
	XCV300		2.0	4.0	4.4	5.1	ns, max
	XCV400		2.1	4.1	4.6	5.3	ns, max
	XCV600		2.1	4.2	4.7	5.4	ns, max
	XCV800		2.2	4.4	4.9	5.6	ns, max
	XCV1000		2.3	4.5	5.1	5.8	ns, max
Sequential Delays							
Clock CLK	All						
Minimum Pulse Width, High		T <sub>CH</sub>	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low		T <sub>CL</sub>	0.8	1.5	1.7	2.0	ns, min
Clock CLK to output IQ		T <sub>IOCKIQ</sub>	0.2	0.7	0.7	0.8	ns, max

### IOB Input Switching Characteristics Standard Adjustments

Description	Symbol	Standard <sup>(1)</sup>	Speed Grade				Units
			Min	-6	-5	-4	
Data Input Delay Adjustments							
Standard-specific data input delay adjustments	T <sub>ILVTTL</sub>	LVTTL	0	0	0	0	ns
	T <sub>ILVCMOS2</sub>	LVC MOS2	−0.02	−0.04	−0.04	−0.05	ns
	T <sub>I PCI33_3</sub>	PCI, 33 MHz, 3.3 V	−0.05	−0.11	−0.12	−0.14	ns
	T <sub>I PCI33_5</sub>	PCI, 33 MHz, 5.0 V	0.13	0.25	0.28	0.33	ns
	T <sub>I PCI66_3</sub>	PCI, 66 MHz, 3.3 V	−0.05	−0.11	−0.12	−0.14	ns
	T <sub>IGTL</sub>	GTL	0.10	0.20	0.23	0.26	ns
	T <sub>IGTLP</sub>	GTL+	0.06	0.11	0.12	0.14	ns
	T <sub>IHSTL</sub>	HSTL	0.02	0.03	0.03	0.04	ns
	T <sub>ISSTL2</sub>	SSTL2	−0.04	−0.08	−0.09	−0.10	ns
	T <sub>ISSTL3</sub>	SSTL3	−0.02	−0.04	−0.05	−0.06	ns
	T <sub>ICTT</sub>	CTT	0.01	0.02	0.02	0.02	ns
	T <sub>IAGP</sub>	AGP	−0.03	−0.06	−0.07	−0.08	ns

#### Notes:

- Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see [Table 3](#).

### IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in [IOB Output Switching Characteristics Standard Adjustments, page 9](#).

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Propagation Delays						
O input to Pad	T <sub>IOOP</sub>	1.2	2.9	3.2	3.5	ns, max
O input to Pad via transparent latch	T <sub>IOOLP</sub>	1.4	3.4	3.7	4.0	ns, max
3-State Delays						
T input to Pad high-impedance <sup>(1)</sup>	T <sub>IOTHZ</sub>	1.0	2.0	2.2	2.4	ns, max
T input to valid data on Pad	T <sub>IOTON</sub>	1.4	3.1	3.3	3.7	ns, max
T input to Pad high-impedance via transparent latch <sup>(1)</sup>	T <sub>IOTLPHZ</sub>	1.2	2.4	2.6	3.0	ns, max
T input to valid data on Pad via transparent latch	T <sub>IOTLPON</sub>	1.6	3.5	3.8	4.2	ns, max
GTS to Pad high impedance <sup>(1)</sup>	T <sub>GTS</sub>	2.5	4.9	5.5	6.3	ns, max
Sequential Delays						
Clock CLK						
Minimum Pulse Width, High	T <sub>CH</sub>	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low	T <sub>CL</sub>	0.8	1.5	1.7	2.0	ns, min

## Calculation of $T_{i\text{oop}}$ as a Function of Capacitance

$T_{i\text{oop}}$  is the propagation delay from the O Input of the IOB to the pad. The values for  $T_{i\text{oop}}$  were based on the standard capacitive load ( $C_{sl}$ ) for each I/O standard as listed in [Table 2](#).

Table 2: Constants for Calculating  $T_{i\text{oop}}$

Standard	Csl (pF)	fl (ns/pF)
LVTTL Fast Slew Rate, 2mA drive	35	0.41
LVTTL Fast Slew Rate, 4mA drive	35	0.20
LVTTL Fast Slew Rate, 6mA drive	35	0.13
LVTTL Fast Slew Rate, 8mA drive	35	0.079
LVTTL Fast Slew Rate, 12mA drive	35	0.044
LVTTL Fast Slew Rate, 16mA drive	35	0.043
LVTTL Fast Slew Rate, 24mA drive	35	0.033
LVTTL Slow Slew Rate, 2mA drive	35	0.41
LVTTL Slow Slew Rate, 4mA drive	35	0.20
LVTTL Slow Slew Rate, 6mA drive	35	0.100
LVTTL Slow Slew Rate, 8mA drive	35	0.086
LVTTL Slow Slew Rate, 12mA drive	35	0.058
LVTTL Slow Slew Rate, 16mA drive	35	0.050
LVTTL Slow Slew Rate, 24mA drive	35	0.048
LVCMS2	35	0.041
PCI 33MHz 5V	50	0.050
PCI 33MHZ 3.3 V	10	0.050
PCI 66 MHz 3.3 V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

### Notes:

1. I/O parameter measurements are made with the capacitance values shown above. See Application Note XAPP133 on [www.xilinx.com](http://www.xilinx.com) for appropriate terminations.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

For other capacitive loads, use the formulas below to calculate the corresponding  $T_{i\text{oop}}$ .

$$T_{i\text{oop}} = T_{i\text{oop}} + T_{\text{opadjust}} + (C_{\text{load}} - C_{sl}) * fl$$

Where:

$T_{\text{opadjust}}$  is reported above in the Output Delay Adjustment section.

$C_{\text{load}}$  is the capacitive load for the design.

Table 3: Delay Measurement Methodology

Standard	$V_L$ (1)	$V_H$ (1)	Meas. Point	$V_{REF}$ Typ (2)
LVTTL	0	3	1.4	-
LVCMS2	0	2.5	1.125	-
PCI33_5	Per PCI Spec			-
PCI33_3	Per PCI Spec			-
PCI66_3	Per PCI Spec			-
GTL	$V_{REF} - 0.2$	$V_{REF} + 0.2$	$V_{REF}$	0.80
GTL+	$V_{REF} - 0.2$	$V_{REF} + 0.2$	$V_{REF}$	1.0
HSTL Class I	$V_{REF} - 0.5$	$V_{REF} + 0.5$	$V_{REF}$	0.75
HSTL Class III	$V_{REF} - 0.5$	$V_{REF} + 0.5$	$V_{REF}$	0.90
HSTL Class IV	$V_{REF} - 0.5$	$V_{REF} + 0.5$	$V_{REF}$	0.90
SSTL3 I & II	$V_{REF} - 1.0$	$V_{REF} + 1.0$	$V_{REF}$	1.5
SSTL2 I & II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	$V_{REF}$	1.25
CTT	$V_{REF} - 0.2$	$V_{REF} + 0.2$	$V_{REF}$	1.5
AGP	$V_{REF} - (0.2 \times V_{CCO})$	$V_{REF} + (0.2 \times V_{CCO})$	$V_{REF}$	Per AGP Spec

### Notes:

1. Input waveform switches between  $V_L$  and  $V_H$ .
2. Measurements are made at  $V_{REF}$  (Typ), Maximum, and Minimum. Worst-case values are reported.
3. I/O parameter measurements are made with the capacitance values shown in [Table 2](#). See Application Note XAPP133 on [www.xilinx.com](http://www.xilinx.com) for appropriate terminations.
4. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

## CLB SelectRAM Switching Characteristics

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Sequential Delays						
Clock CLK to X/Y outputs (WE active) 16 x 1 mode	T <sub>SHCKO16</sub>	1.2	2.3	2.6	3.0	ns, max
Clock CLK to X/Y outputs (WE active) 32 x 1 mode	T <sub>SHCKO32</sub>	1.2	2.7	3.1	3.5	ns, max
Shift-Register Mode						
Clock CLK to X/Y outputs	T <sub>REG</sub>	1.2	3.7	4.1	4.7	ns, max
Setup and Hold Times before/after Clock CLK <sup>(1)</sup>	Setup Time / Hold Time					
F/G address inputs	T <sub>AS</sub> /T <sub>AH</sub>	0.25 / 0	0.5 / 0	0.6 / 0	0.7 / 0	ns, min
BX/BY data inputs (DIN)	T <sub>DS</sub> /T <sub>DH</sub>	0.34 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
CE input (WE)	T <sub>WS</sub> /T <sub>WH</sub>	0.38 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
Shift-Register Mode						
BX/BY data inputs (DIN)	T <sub>SHDICK</sub>	0.34	0.7	0.8	0.9	ns, min
CE input (WS)	T <sub>SHCECK</sub>	0.38	0.8	0.9	1.0	ns, min
Clock CLK						
Minimum Pulse Width, High	T <sub>WPH</sub>	1.2	2.4	2.7	3.1	ns, min
Minimum Pulse Width, Low	T <sub>WPL</sub>	1.2	2.4	2.7	3.1	ns, min
Minimum clock period to meet address write cycle time	T <sub>WC</sub>	2.4	4.8	5.4	6.2	ns, min
Shift-Register Mode						
Minimum Pulse Width, High	T <sub>SRPH</sub>	1.2	2.4	2.7	3.1	ns, min
Minimum Pulse Width, Low	T <sub>SRPL</sub>	1.2	2.4	2.7	3.1	ns, min

**Notes:**

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

### DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Description	Symbol	Speed Grade						Units
		-6		-5		-4		
		Min	Max	Min	Max	Min	Max	
Input Clock Frequency (CLKDLLHF)	FCLKINHF	60	200	60	180	60	180	MHz
Input Clock Frequency (CLKDLL)	FCLKINLF	25	100	25	90	25	90	MHz
Input Clock Pulse Width (CLKDLLHF)	T <sub>DLLPWHF</sub>	2.0	-	2.4	-	2.4	-	ns
Input Clock Pulse Width (CLKDLL)	T <sub>DLLPWLF</sub>	2.5	-	3.0		3.0	-	ns

#### Notes:

1. All specifications correspond to Commercial Operating Temperatures (0°C to +85°C).

### DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

Description	Symbol	F <sub>CLKIN</sub>	CLKDLLHF		CLKDLL		Units
			Min	Max	Min	Max	
Input Clock Period Tolerance	T <sub>IP</sub> TOL		-	1.0	-	1.0	ns
Input Clock Jitter Tolerance (Cycle to Cycle)	T <sub>IJ</sub> TCC		-	± 150	-	± 300	ps
Time Required for DLL to Acquire Lock	T <sub>LOCK</sub>	> 60 MHz	-	20	-	20	μs
		50 - 60 MHz	-	-	-	25	μs
		40 - 50 MHz	-	-	-	50	μs
		30 - 40 MHz	-	-	-	90	μs
		25 - 30 MHz	-	-	-	120	μs
Output Jitter (cycle-to-cycle) for any DLL Clock Output <sup>(1)</sup>	T <sub>OJ</sub> TCC			± 60		± 60	ps
Phase Offset between CLKIN and CLKO <sup>(2)</sup>	T <sub>PHIO</sub>			± 100		± 100	ps
Phase Offset between Clock Outputs on the DLL <sup>(3)</sup>	T <sub>PHOO</sub>			± 140		± 140	ps
Maximum Phase Difference between CLKIN and CLKO <sup>(4)</sup>	T <sub>PHIOM</sub>			± 160		± 160	ps
Maximum Phase Difference between Clock Outputs on the DLL <sup>(5)</sup>	T <sub>PHOOM</sub>			± 200		± 200	ps

#### Notes:

1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* Output Jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN and CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of Output Jitter and Phase Offset between any two DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).
6. All specifications correspond to Commercial Operating Temperatures (0°C to +85°C).





## Virtex Pinout Information

### Pinout Tables

See [www.xilinx.com](http://www.xilinx.com) for updates or additional pinout information. For convenience, [Table 2](#), [Table 3](#) and [Table 4](#) list the locations of special-purpose and power-supply pins. Pins not listed are either user I/Os or not connected, depending on the device/package combination. See the Pinout Diagrams starting on [page 17](#) for any pins not listed for a particular part/package combination.

*Table 2: Virtex Pinout Tables (Chip-Scale and QFP Packages)*

Pin Name	Device	CS144	TQ144	PQ/HQ240
GCK0	All	K7	90	92
GCK1	All	M7	93	89
GCK2	All	A7	19	210
GCK3	All	A6	16	213
M0	All	M1	110	60
M1	All	L2	112	58
M2	All	N2	108	62
CCLK	All	B13	38	179
PROGRAM	All	L12	72	122
DONE	All	M12	74	120
INIT	All	L13	71	123
BUSY/DOUT	All	C11	39	178
D0/DIN	All	C12	40	177
D1	All	E10	45	167
D2	All	E12	47	163
D3	All	F11	51	156
D4	All	H12	59	145
D5	All	J13	63	138
D6	All	J11	65	134
D7	All	K10	70	124
WRITE	All	C10	32	185
CS	All	D10	33	184
TDI	All	A11	34	183
TDO	All	A12	36	181
TMS	All	B1	143	2
TCK	All	C3	2	239
V <sub>CCINT</sub>	All	A9, B6, C5, G3, G12, M5, M9, N6	10, 15, 25, 57, 84, 94, 99, 126	16, 32, 43, 77, 88, 104, 137, 148, 164, 198, 214, 225

Table 3: Virtex Pinout Tables (BGA)

Pin Name	Device	BG256	BG352	BG432	BG560
GCK0	All	Y11	AE13	AL16	AL17
GCK1	All	Y10	AF14	AK16	AJ17
GCK2	All	A10	B14	A16	D17
GCK3	All	B10	D14	D17	A17
M0	All	Y1	AD24	AH28	AJ29
M1	All	U3	AB23	AH29	AK30
M2	All	W2	AC23	AJ28	AN32
CCLK	All	B19	C3	D4	C4
PROGRAM	All	Y20	AC4	AH3	AM1
DONE	All	W19	AD3	AH4	AJ5
INIT	All	U18	AD2	AJ2	AH5
BUSY/DOUT	All	D18	E4	D3	D4
D0/DIN	All	C19	D3	C2	E4
D1	All	E20	G1	K4	K3
D2	All	G19	J3	K2	L4
D3	All	J19	M3	P4	P3
D4	All	M19	R3	V4	W4
D5	All	P19	U4	AB1	AB5
D6	All	T20	V3	AB3	AC4
D7	All	V19	AC3	AG4	AJ4
WRITE	All	A19	D5	B4	D6
CS	All	B18	C4	D5	A2
TDI	All	C17	B3	B3	D5
TDO	All	A20	D4	C4	E6
TMS	All	D3	D23	D29	B33
TCK	All	A1	C24	D28	E29
DXN	All	W3	AD23	AH27	AK29
DXP	All	V4	AE24	AK29	AJ28

Table 3: Virtex Pinout Tables (BGA) (Continued)

Pin Name	Device	BG256	BG352	BG432	BG560
<b>V<sub>REF</sub> Bank 3</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	M18, V20	N/A	N/A	N/A
	XCV100/150	... + R19	R4, V4, Y3	N/A	N/A
	XCV200/300	... + P18	... + AC2	V2, AB4, AD4, AF3	N/A
	XCV400	N/A	N/A	... + U2	V4, W5, AD3, AE5, AK2
	XCV600	N/A	N/A	... + AC3	... + AF1
	XCV800	N/A	N/A	... + Y3	... + AA4
	XCV1000	N/A	N/A	N/A	... + AH4
<b>V<sub>REF</sub> Bank 4</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	V12, Y18	N/A	N/A	N/A
	XCV100/150	... + W15	AC12, AE5, AE8,	N/A	N/A
	XCV200/300	... + V14	... + AE4	AJ7, AL4, AL8, AL13	N/A
	XCV400	N/A	N/A	... + AK15	AL7, AL10, AL16, AM4, AM14
	XCV600	N/A	N/A	... + AK8	... + AL9
	XCV800	N/A	N/A	... + AJ12	... + AK13
	XCV1000	N/A	N/A	N/A	... + AN3
<b>V<sub>REF</sub> Bank 5</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	V9, Y3	N/A	N/A	N/A
	XCV100/150	... + W6	AC15, AC18, AD20	N/A	N/A
	XCV200/300	... + V7	... + AE23	AJ18, AJ25, AK23, AK27	N/A
	XCV400	N/A	N/A	... + AJ17	AJ18, AJ25, AL20, AL24, AL29
	XCV600	N/A	N/A	... + AL24	... + AM26
	XCV800	N/A	N/A	... + AH19	... + AN23
	XCV1000	N/A	N/A	N/A	... + AK28
<b>V<sub>REF</sub> Bank 6</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	M2, R3	N/A	N/A	N/A
	XCV100/150	... + T1	R24, Y26, AA25,	N/A	N/A
	XCV200/300	... + T3	... + AD26	V28, AB28, AE30, AF28	N/A
	XCV400	N/A	N/A	... + U28	V29, Y32, AD31, AE29, AK32
	XCV600	N/A	N/A	... + AC28	... + AE31
	XCV800	N/A	N/A	... + Y30	... + AA30
	XCV1000	N/A	N/A	N/A	... + AH30

Table 4: Virtex Pinout Tables (Fine-Pitch BGA) (Continued)

Pin Name	Device	FG256	FG456	FG676	FG680
V <sub>CCINT</sub>	All	C3, C14, D4, D13, E5, E12, M5, M12, N4, N13, P3, P14	E5, E18, F6, F17, G7, G8, G9, G14, G15, G16, H7, H16, J7, J16, P7, P16, R7, R16, T7, T8, T9, T14, T15, T16, U6, U17, V5, V18	G7, G20, H8, H19, J9, J10, J11, J16, J17, J18, K9, K18, L9, L18, T9, T18, U9, U18, V9, V10, V11, V16, V17, V18, W8, W19, Y7, Y20	AD5, AD35, AE5, AE35, AL5, AL35, AM5, AM35, AR8, AR9, AR15, AR16, AR24, AR25, AR31, AR32, E8, E9, E15, E16, E24, E25, E31, E32, H5, H35, J5, J35, R5, R35, T5, T35
V <sub>CCO</sub> , Bank 0	All	E8, F8	F7, F8, F9, F10, G10, G11	H9, H10, H11, H12, J12, J13	E26, E27, E29, E30, E33, E34
V <sub>CCO</sub> , Bank 1	All	E9, F9	F13, F14, F15, F16, G12, G13	H15, H16, H17, H18, J14, J15	E6, E7, E10, E11, E13, E14
V <sub>CCO</sub> , Bank 2	All	H11, H12	G17, H17, J17, K16, K17, L16	J19, K19, L19, M18, M19, N18	F5, G5, K5, L5, N5, P5
V <sub>CCO</sub> , Bank 3	All	J11, J12	M16, N16, N17, P17, R17, T17	P18, R18, R19, T19, U19, V19	AF5, AG5, AN5, AK5, AJ5, AP5
V <sub>CCO</sub> , Bank 4	All	L9, M9	T12, T13, U13, U14, U15, U16,	V14, V15, W15, W16, W17, W18	AR6, AR7, AR10, AR11, AR13, AR14
V <sub>CCO</sub> , Bank 5	All	L8, M8	T10, T11, U7, U8, U9, U10	V12, V13, W9, W10, W11, W12	AR26, AR27, AR29, AR30, AR33, AR34
V <sub>CCO</sub> , Bank 6	All	J5, J6	M7, N6, N7, P6, R6, T6	P9, R8, R9, T8, U8, V8	AF35, AG35, AJ35, AK35, AN35, AP35
V <sub>CCO</sub> , Bank 7	All	H5, H6	G6, H6, J6, K6, K7, L7	J8, K8, L8, M8, M9, N9	F35, G35, K35, L35, N35, P35
V <sub>REF</sub> , Bank 0 (VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	B4, B7	N/A	N/A	N/A
	XCV100/150	... + C6	A9, C6, E8	N/A	N/A
	XCV200/300	... + A3	... + B4	N/A	N/A
	XCV400	N/A	N/A	A12, C11, D6, E8, G10	
	XCV600	N/A	N/A	... + B7	A33, B28, B30, C23, C24, D33
	XCV800	N/A	N/A	... + B10	... + A26
	XCV1000	N/A	N/A	N/A	... + D34

## TQ144 Pin Function Diagram

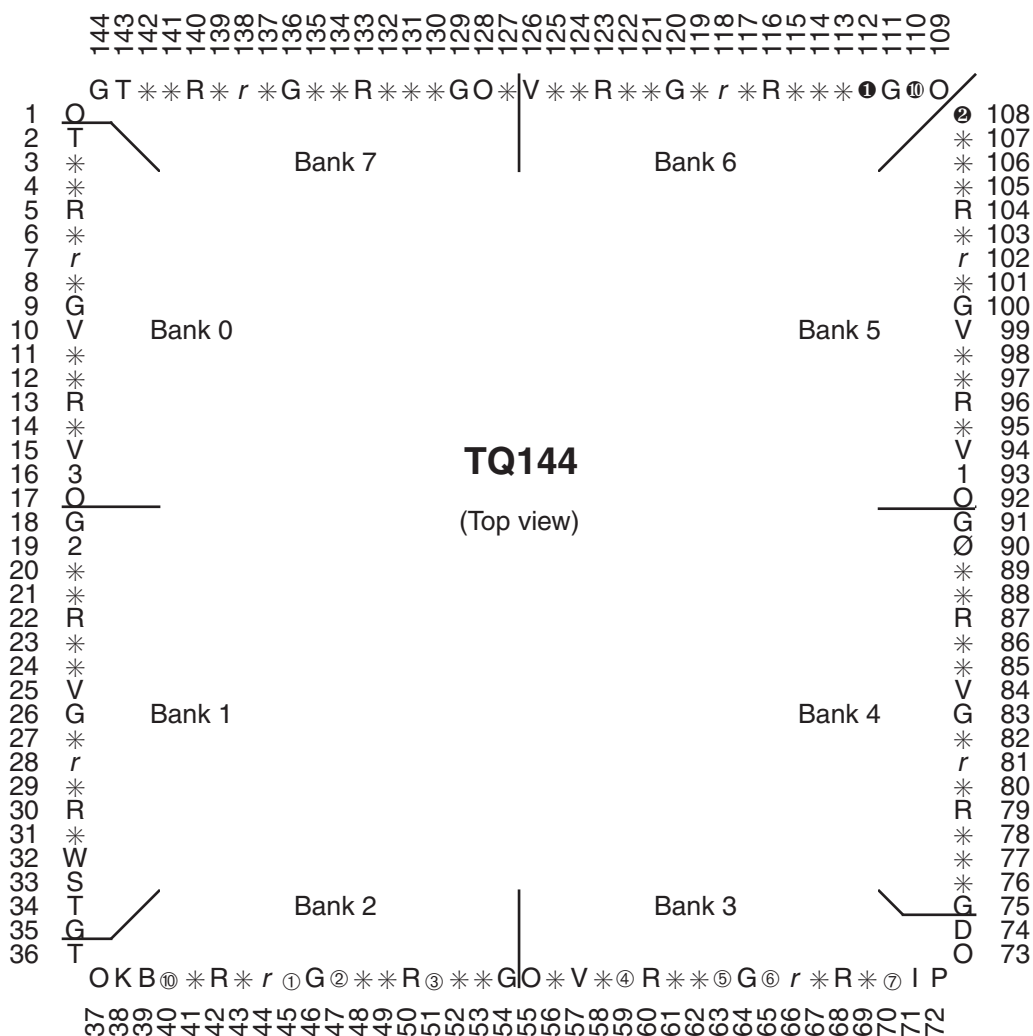
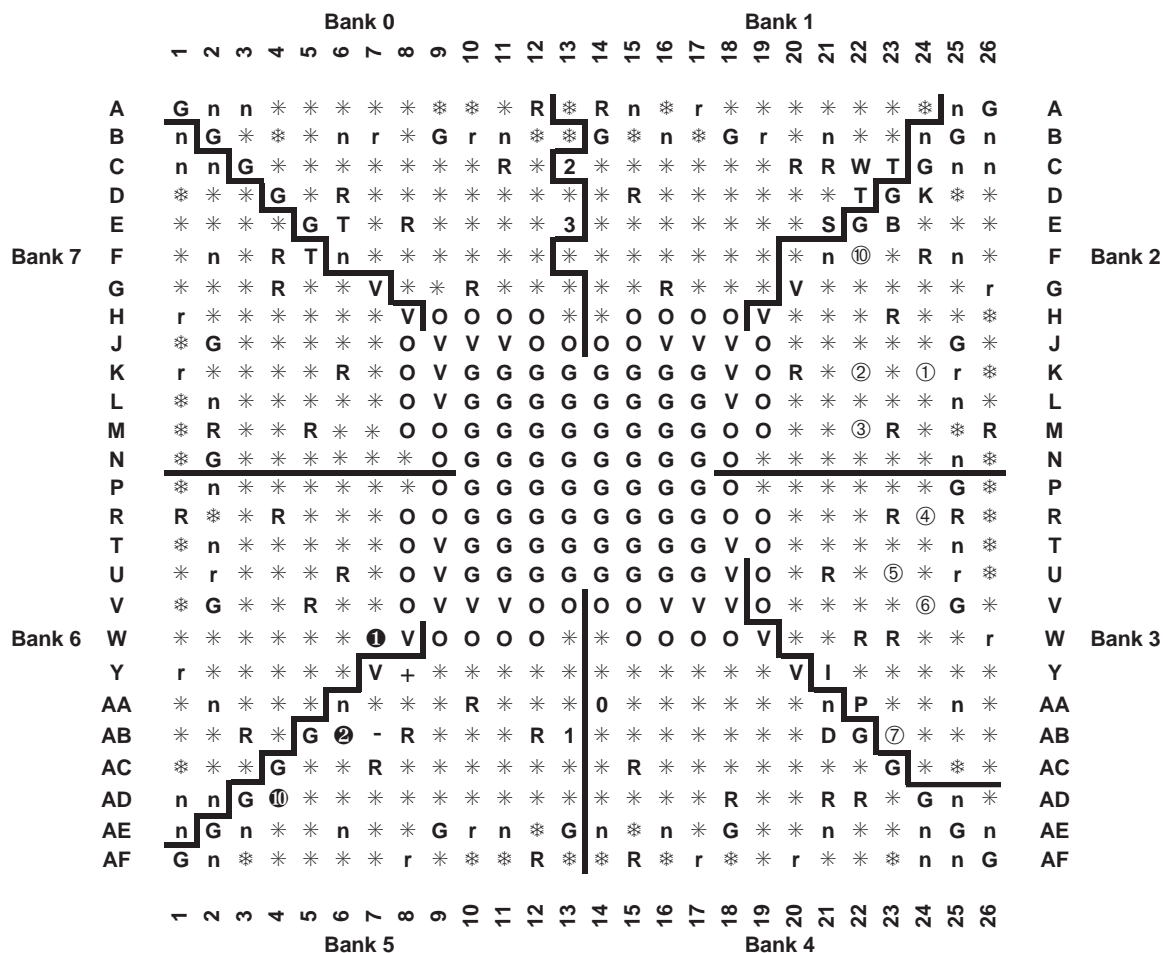


Figure 2: TQ144 Pin Function Diagram



## FG676 Pin Function Diagram

FG676  
(Top view)

fg676a

Figure 10: FG676 Pin Function Diagram

## Notes:

Packages FG456 and FG676 are layout compatible.