Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	600
Number of Logic Elements/Cells	2700
Total RAM Bits	40960
Number of I/O	176
Number of Gates	108904
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv100-6fg256c

Virtex Architecture

Virtex devices feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing resources. The abundance of routing resources permits the Virtex family to accommodate even the largest and most complex designs.

Virtex FPGAs are SRAM-based, and are customized by loading configuration data into internal memory cells. In some modes, the FPGA reads its own configuration data from an external PROM (master serial mode). Otherwise, the configuration data is written into the FPGA (Select-MAP™, slave serial, and JTAG modes).

The standard Xilinx Foundation™ and Alliance Series™ Development systems deliver complete design support for Virtex, covering every aspect from behavioral and schematic entry, through simulation, automatic design translation and implementation, to the creation, downloading, and readback of a configuration bit stream.

Higher Performance

Virtex devices provide better performance than previous generations of FPGA. Designs can achieve synchronous system clock rates up to 200 MHz including I/O. Virtex inputs and outputs comply fully with PCI specifications, and interfaces can be implemented that operate at 33 MHz or 66 MHz. Additionally, Virtex supports the hot-swapping requirements of Compact PCI.

Xilinx thoroughly benchmarked the Virtex family. While performance is design-dependent, many designs operated internally at speeds in excess of 100 MHz and can achieve 200 MHz. Table 2 shows performance data for representative circuits, using worst-case timing parameters.

Table 2: **Performance for Common Circuit Functions**

Function	Bits	Virtex -6
Register-to-Register		
Adder	16	5.0 ns
	64	7.2 ns
Pipelined Multiplier	8 x 8	5.1 ns
	16 x 16	6.0 ns
Address Decoder	16	4.4 ns
	64	6.4 ns
16:1 Multiplexer		5.4 ns
Parity Tree	9	4.1 ns
	18	5.0 ns
	36	6.9 ns
Chip-to-Chip		
HSTL Class IV		200 MHz
LVTTL,16mA, fast slew		180 MHz

Input Path

A buffer In the Virtex IOB input path routes the input signal either directly to internal logic or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signalling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can used in close proximity to each other. See **I/O Banking**, page 3.

There are optional pull-up and pull-down resistors at each user I/O input for use after configuration. Their value is in the range 50 kΩ – 100 kΩ.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signalling standards. Each output buffer can source up to 24 mA and sink up to 48mA. Drive strength and slew rate controls minimize bus transients.

In most signalling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See **I/O Banking**, page 3.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signalling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages externally and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks, as shown in Figure 3. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.
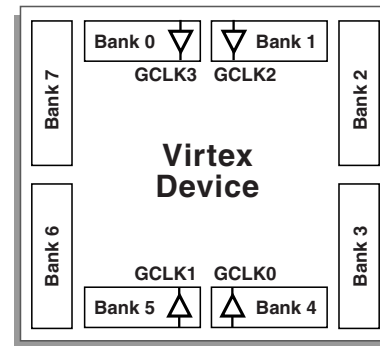
X8778_b

Figure 3: **Virtex I/O Banks**

Within a bank, output standards can be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 2. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}.

Table 2: **Compatible Output Standards**

V_{CCO}	Compatible Standards
3.3 V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+
2.5 V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+
1.5 V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, V_{REF}. In this case, certain user-I/O pins are automatically configured as inputs for the V_{REF} voltage. Approximately one in six of the I/O pins in the bank assume this role.

The V_{REF} pins within a bank are interconnected internally and consequently only one V_{REF} voltage can be used within each bank. All V_{REF} pins in the bank, however, must be connected to the external voltage source for correct operation.

Within a bank, inputs that require V_{REF} can be mixed with those that do not. However, only one V_{REF} voltage can be used within a bank. Input buffers that use V_{REF} are not 5 V tolerant. LVTTL, LVCMOS2, and PCI 33 MHz 5 V, are 5 V tolerant.

The V_{CCO} and V_{REF} pins for each bank appear in the device Pinout tables and diagrams. The diagrams also show the bank affiliation of each I/O.

Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices,

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is

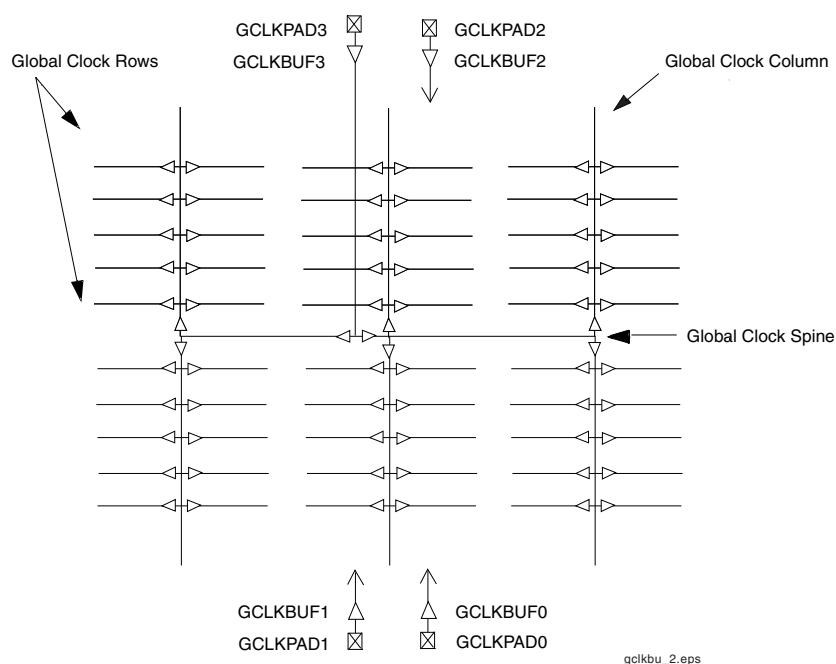selected either from these pads or from signals in the general purpose routing.

Figure 9: **Global Clock Distribution Network**

Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks.The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Clock edges reach internal flip-flops one to four clock periods after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to de-skew a board level clock among multiple Virtex devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

See **DLL Timing Parameters**, page 21 of Module 3, for frequency range information.

Boundary Scan

Virtex devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, and HIGHZ instructions. The TAP also supports two internal scan chains and configuration/readback of the device.The TAP uses dedicated package pins that always operate using LVTTL. For TDO to operate using LVTTL, the V_{CCO} for Bank 2 should be 3.3 V. Otherwise, TDO switches rail-to-rail between ground and V_{CCO}.

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including un-bonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections, provided the user design or application is turned off.

Table 5 lists the boundary-scan instructions supported in Virtex FPGAs. Internal signals can be captured during EXTEST by connecting them to un-bonded or unused IOBs. They can also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Before the device is configured, all instructions except USER1 and USER2 are available. After configuration, all instructions are available. During configuration, it is recommended that those operations using the boundary-scan register (SAMPLE/PRELOAD, INTEST, EXTEST) not be performed.

Configuration

Virtex devices are configured by loading configuration data into the internal configuration memory. Some of the pins used for this are dedicated configuration pins, while others can be re-used as general purpose inputs and outputs once configuration is complete.

The following are dedicated pins:

- Mode pins (M2, M1, M0)
- Configuration clock pin (CCLK)
- PROGRAM pin
- DONE pin
- Boundary-scan pins (TDI, TDO, TMS, TCK)

Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or it can be generated externally and provided to the FPGA as an input. The PROGRAM pin must be pulled High prior to reconfiguration.

Note that some configuration pins can act as outputs. For correct operation, these pins can require a V_{CCO} of 3.3 V to permit LVTTL operation. All the pins affected are in banks 2 or 3. The configuration pins needed for SelectMap (CS, Write) are located in bank 1.

After Virtex devices are configured, unused IOBs function as 3-state OBUFTs with weak pull downs. For a more detailed description than that given below, see the XAPP138, Virtex Configuration and Readback.

Configuration Modes

Virtex supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- SelectMAP mode
- Boundary-scan mode

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in Table 7.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected. However, it is recommended to drive the configuration mode pins externally.

Table 7: **Configuration Codes**

Configuration Mode	M2	M1	M0	CCLK Direction	Data Width	Serial D_{out}	Configuration Pull-ups
Master-serial mode	0	0	0	Out	1	Yes	No
Boundary-scan mode	1	0	1	N/A	1	No	No
SelectMAP mode	1	1	0	In	8	No	No
Slave-serial mode	1	1	1	In	1	Yes	No
Master-serial mode	1	0	0	Out	1	Yes	Yes
Boundary-scan mode	0	0	1	N/A	1	No	Yes
SelectMAP mode	0	1	0	In	8	No	Yes
Slave-serial mode	0	1	1	In	1	Yes	Yes

Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other source of serial configuration data. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

For more information on serial PROMs, see the PROM data sheet at:
http://www.xilinx.com/bvdocs/publications/ds026.pdf.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin. The data on the DOUT pin changes on the rising edge of CCLK.

The change of DOUT on the rising edge of CCLK differs from previous families, but does not cause a problem for mixed configuration chains. This change was made to improve serial configuration rates for Virtex-only chains.

Figure 12 shows a full master/slave system. A Virtex device in slave-serial mode should be connected as shown in the third device from the left.

Slave-serial mode is selected by applying <111> or <011> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave-serial the default mode if the pins are left unconnected. However, it is recommended to drive the configuration mode pins externally. Figure 13 shows slave-serial mode programming switching characteristics.

Table 8 provides more detail about the characteristics shown in Figure 13. Configuration must be delayed until the INIT pins of all daisy-chained FPGAs are High.

3. At the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this has happened.

4. Repeat steps 2 and 3 until all the data has been sent.

5. De-assert $\overline{CS}$ and $\overline{WRITE}$.

A flowchart for the write operation appears in Figure 17. Note that if CCLK is slower than f_{CCNH}, the FPGA never asserts BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.
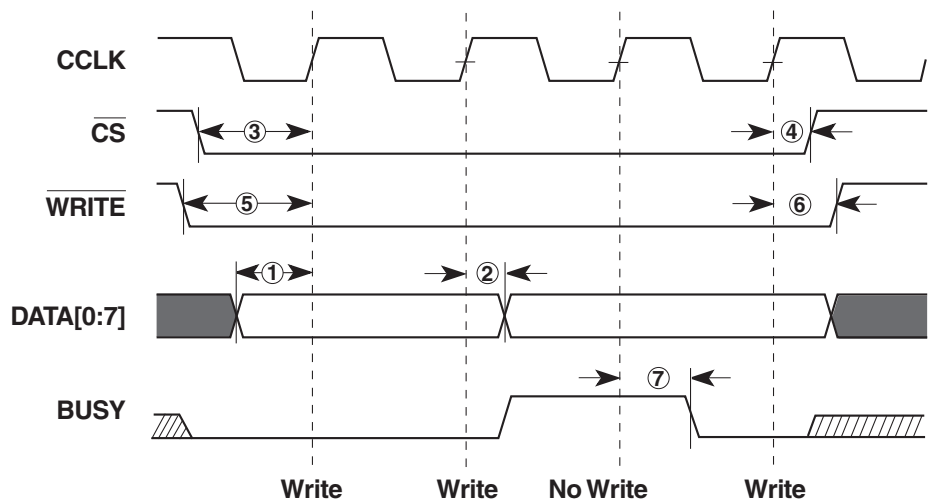
ds003_16_071902

Figure 16: **Write Operations**

$$\Sigma\text{XILINX}^{®}$$
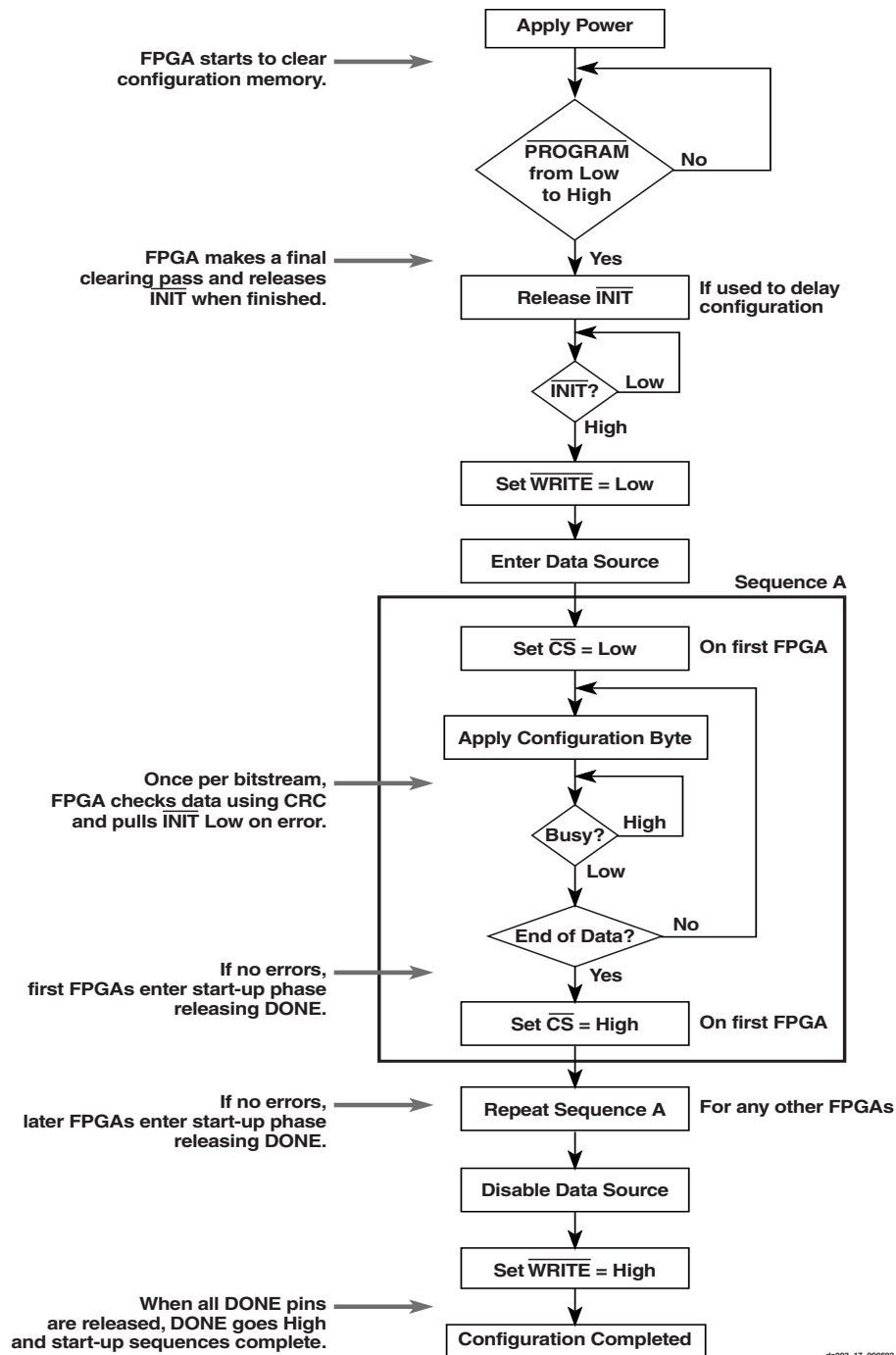
Figure 17: **SelectMAP Flowchart for Write Operation**

Abort

During a given assertion of $\overline{CS}$, the user cannot switch from a write to a read, or vice-versa. This action causes the current packet command to be aborted. The device will remain BUSY until the aborted operation has completed. Following an abort, data is assumed to be unaligned to word boundar-

ies, and the FPGA requires a new synchronization word prior to accepting any new packets.

To initiate an abort during a write operation, de-assert $\overline{WRITE}$. At the rising edge of CCLK, an abort is initiated, as shown in Figure 18.

Data Stream Format

Virtex devices are configured by sequentially loading frames of data. Table 11 lists the total number of bits required to configure each device. For more detailed information, see application note XAPP151 "Virtex Configuration Architecture Advanced Users Guide".

Table 11: **Virtex Bit-Stream Lengths**

Device	# of Configuration Bits
XCV50	559,200
XCV100	781,216
XCV150	1,040,096
XCV200	1,335,840
XCV300	1,751,808
XCV400	2,546,048
XCV600	3,607,968
XCV800	4,715,616
XCV1000	6,127,744

Readback

The configuration data stored in the Virtex configuration memory can be readback for verification. Along with the configuration data it is possible to readback the contents all flip-flops/latches, LUTRAMs, and block RAMs. This capability is used for real-time debugging.

For more detailed information, see Application Note XAPP138: *Virtex FPGA Series Configuration and Readback*, available online at www.xilinx.com.

Revision History

Date	Version	Revision
11/98	1.0	Initial Xilinx release.
01/99	1.2	Updated package drawings and specs.
02/99	1.3	Update of package drawings, updated specifications.
05/99	1.4	Addition of package drawings and specifications.
05/99	1.5	Replaced FG 676 & FG680 package drawings.
07/99	1.6	Changed Boundary Scan Information and changed Figure 11, Boundary Scan Bit Sequence. Updated IOB Input & Output delays. Added Capacitance info for different I/O Standards. Added 5 V tolerant information. Added DLL Parameters and waveforms and new Pin-to-pin Input and Output Parameter tables for Global Clock Input to Output and Setup and Hold. Changed Configuration Information including Figures 12, 14, 17 & 19. Added device-dependent listings for quiescent currents ICCINTQ and ICCOQ. Updated IOB Input and Output Delays based on default standard of LVTTL, 12 mA, Fast Slew Rate. Added IOB Input Switching Characteristics Standard Adjustments.
09/99	1.7	Speed grade update to preliminary status, Power-on specification and Clock-to-Out Minimums additions, "0" hold time listing explanation, quiescent current listing update, and Figure 6 ADDRA input label correction. Added T_{IJITCC} parameter, changed T_{OJIT} to T_{OPHASE}.
01/00	1.8	Update to speed.txt file 1.96. Corrections for CRs 111036,111137, 112697, 115479, 117153, 117154, and 117612. Modified notes for Recommended Operating Conditions (voltage and temperature). Changed Bank information for V_{CCO} in CS144 package on p.43.

I/O Standard Global Clock Input Adjustments

Description	Symbol	Standard[1]	Speed Grade				Units
			Min	-6	-5	-4	
Data Input Delay Adjustments							
Standard-specific global clock input delay adjustments	$T_{GPLVTTL}$	LVTTL	0	0	0	0	ns, max
	$T_{GPLVCMOS2}$	LVCMOS2	–0.02	–0.04	–0.04	–0.05	ns, max
	$T_{GPPCI33\_3}$	PCI, 33 MHz, 3.3 V	–0.05	–0.11	–0.12	–0.14	ns, max
	$T_{GPPCI33\_5}$	PCI, 33 MHz, 5.0 V	0.13	0.25	0.28	0.33	ns, max
	$T_{GPPCI66\_3}$	PCI, 66 MHz, 3.3 V	–0.05	–0.11	–0.12	–0.14	ns, max
	T_{GPGTL}	GTL	0.7	0.8	0.9	0.9	ns, max
	T_{GPGTLP}	GTL+	0.7	0.8	0.8	0.8	ns, max
	T_{GPHSTL}	HSTL	0.7	0.7	0.7	0.7	ns, max
	$T_{GPSSTL2}$	SSTL2	0.6	0.52	0.51	0.50	ns, max
	$T_{GPSSTL3}$	SSTL3	0.6	0.6	0.55	0.54	ns, max
	T_{GPCTT}	CTT	0.7	0.7	0.7	0.7	ns, max
	T_{GPAGP}	AGP	0.6	0.54	0.53	0.52	ns, max

Notes:
1. Input timing for GPLVTTL is measured at 1.4 V. For other I/O standards, see Table 3.

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Combinatorial Delays						
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.29	0.6	0.7	0.8	ns, max
5-input function: F/G inputs to F5 output	T_{IF5}	0.32	0.7	0.8	0.9	ns, max
5-input function: F/G inputs to X output	T_{IF5X}	0.36	0.8	0.8	1.0	ns, max
6-input function: F/G inputs to Y output via F6 MUX	T_{IF6Y}	0.44	0.9	1.0	1.2	ns, max
6-input function: F5IN input to Y output	T_{F5INY}	0.17	0.32	0.36	0.42	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.31	0.7	0.7	0.8	ns, max
BY input to YB output	T_{BYYB}	0.27	0.53	0.6	0.7	ns, max
Sequential Delays						
FF Clock CLK to XQ/YQ outputs	T_{CKO}	0.54	1.1	1.2	1.4	ns, max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.6	1.2	1.4	1.6	ns, max
Setup and Hold Times before/after Clock CLK[1]		Setup Time / Hold Time				
4-input function: F/G Inputs	T_{ICK}/T_{CKI}	0.6 / 0	1.2 / 0	1.4 / 0	1.5 / 0	ns, min
5-input function: F/G inputs	T_{IF5CK}/T_{CKIF5}	0.7 / 0	1.3 / 0	1.5 / 0	1.7 / 0	ns, min
6-input function: F5IN input	T_{F5INCK}/T_{CKF5IN}	0.46 / 0	1.0 / 0	1.1 / 0	1.2 / 0	ns, min
6-input function: F/G inputs via F6 MUX	T_{IF6CK}/T_{CKIF6}	0.8 / 0	1.5 / 0	1.7 / 0	1.9 / 0	ns, min
BX/BY inputs	T_{DICK}/T_{CKDI}	0.30 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
CE input	T_{CECK}/T_{CKCE}	0.37 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
SR/BY inputs (synchronous)	$T_{RCK}T_{CKR}$	0.33 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{CH}	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low	T_{CL}	0.8	1.5	1.7	2.0	ns, min
Set/Reset						
Minimum Pulse Width, SR/BY inputs	T_{RPW}	1.3	2.5	2.8	3.3	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}	0.54	1.1	1.3	1.4	ns, max
Delay from GSR to XQ/YQ outputs	T_{IOGSRQ}	4.9	9.7	10.9	12.5	ns, max
Toggle Frequency (MHz) (for export control)	F_{TOG} (MHz)	625	333	294	250	MHz

Notes:
1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Minimum Clock-to-Out for Virtex Devices

I/O Standard	With DLL	Without DLL									Units
	All Devices	V50	V100	V150	V200	V300	V400	V600	V800	V1000	
*LVTTL_S2	5.2	6.0	6.0	6.0	6.0	6.1	6.1	6.1	6.1	6.1	ns
*LVTTL_S4	3.5	4.3	4.3	4.3	4.3	4.4	4.4	4.4	4.4	4.4	ns
*LVTTL_S6	2.8	3.6	3.6	3.6	3.6	3.7	3.7	3.7	3.7	3.7	ns
*LVTTL_S8	2.2	3.1	3.1	3.1	3.1	3.1	3.1	3.2	3.2	3.2	ns
*LVTTL_S12	2.0	2.9	2.9	2.9	2.9	2.9	2.9	3.0	3.0	3.0	ns
*LVTTL_S16	1.9	2.8	2.8	2.8	2.8	2.8	2.8	2.9	2.9	2.9	ns
*LVTTL_S24	1.8	2.6	2.6	2.7	2.7	2.7	2.7	2.7	2.7	2.8	ns
*LVTTL_F2	2.9	3.8	3.8	3.8	3.8	3.8	3.8	3.9	3.9	3.9	ns
*LVTTL_F4	1.7	2.6	2.6	2.6	2.6	2.6	2.6	2.7	2.7	2.7	ns
*LVTTL_F6	1.2	2.0	2.0	2.0	2.1	2.1	2.1	2.1	2.1	2.2	ns
*LVTTL_F8	1.1	1.9	1.9	1.9	1.9	2.0	2.0	2.0	2.0	2.0	ns
*LVTTL_F12	1.0	1.8	1.8	1.8	1.8	1.9	1.9	1.9	1.9	1.9	ns
*LVTTL_F16	0.9	1.7	1.8	1.8	1.8	1.8	1.8	1.8	1.9	1.9	ns
*LVTTL_F24	0.9	1.7	1.7	1.7	1.8	1.8	1.8	1.8	1.8	1.9	ns
LVCMOS2	1.1	1.9	1.9	1.9	2.0	2.0	2.0	2.0	2.0	2.1	ns
PCI33_3	1.5	2.4	2.4	2.4	2.4	2.4	2.4	2.5	2.5	2.5	ns
PCI33_5	1.4	2.2	2.2	2.3	2.3	2.3	2.3	2.3	2.3	2.4	ns
PCI66_3	1.1	1.9	1.9	2.0	2.0	2.0	2.0	2.0	2.1	2.1	ns
GTL	1.6	2.5	2.5	2.5	2.5	2.5	2.5	2.6	2.6	2.6	ns
GTL+	1.7	2.5	2.5	2.6	2.6	2.6	2.6	2.6	2.6	2.7	ns
HSTL I	1.1	1.9	1.9	1.9	1.9	2.0	2.0	2.0	2.0	2.0	ns
HSTL III	0.9	1.7	1.7	1.8	1.8	1.8	1.8	1.8	1.8	1.9	ns
HSTL IV	0.8	1.6	1.6	1.6	1.7	1.7	1.7	1.7	1.7	1.8	ns
SSTL2 I	0.9	1.7	1.7	1.7	1.7	1.8	1.8	1.8	1.8	1.8	ns
SSTL2 II	0.8	1.6	1.6	1.6	1.6	1.7	1.7	1.7	1.7	1.7	ns
SSTL3 I	0.8	1.6	1.7	1.7	1.7	1.7	1.7	1.7	1.8	1.8	ns
SSTL3 II	0.7	1.5	1.5	1.6	1.6	1.6	1.6	1.6	1.6	1.7	ns
CTT	1.0	1.8	1.8	1.8	1.9	1.9	1.9	1.9	1.9	2.0	ns
AGP	1.0	1.8	1.8	1.9	1.9	1.9	1.9	1.9	1.9	2.0	ns

*S = Slow Slew Rate, F = Fast Slew Rate

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Input and output timing is measured at 1.4 V for LVTTL. For other I/O standards, see Table 3. In all cases, an 8 pF external capacitive load is used.

Period Tolerance: the allowed input clock period change in nanoseconds.

T_{CLKIN}

$|T_{CLKIN} \pm T_{IPTOL}|$
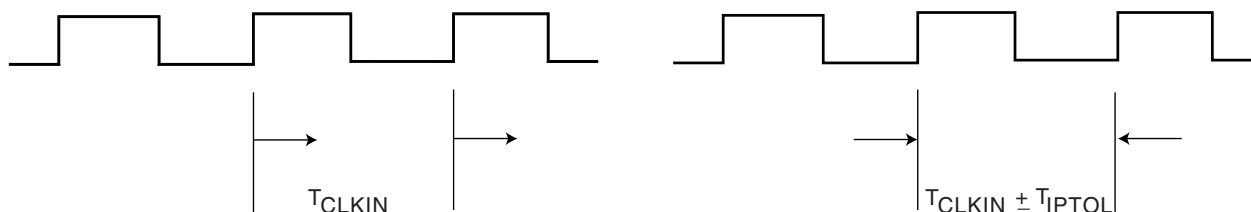
Output Jitter: the difference between an ideal reference clock edge and the actual design.

Ideal Period

Actual Period

+ Jitter

Phase Offset and Maximum Phase Difference

+/- Jitter

+ Maximum Phase Difference

+ Phase Offset
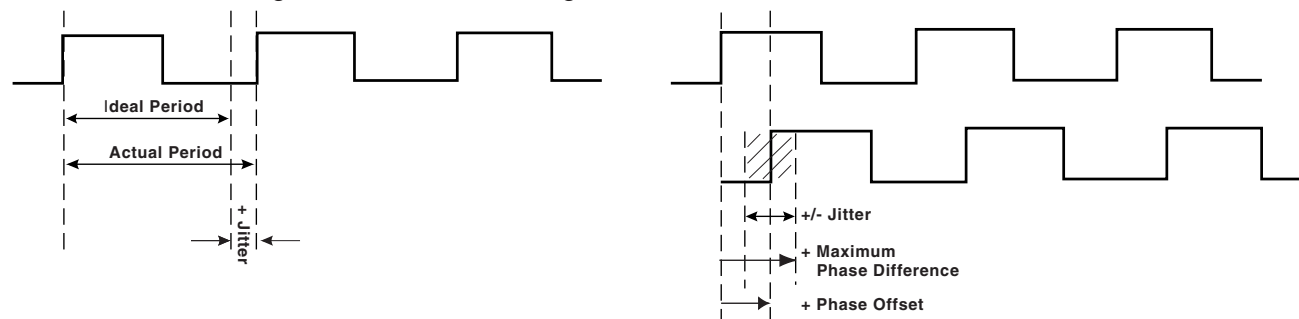
ds003_20c_110399

Figure 1: **Frequency Tolerance and Clock Jitter**

Revision History

Date	Version	Revision
11/98	1.0	Initial Xilinx release.
01/99	1.2	Updated package drawings and specs.
02/99	1.3	Update of package drawings, updated specifications.
05/99	1.4	Addition of package drawings and specifications.
05/99	1.5	Replaced FG 676 & FG680 package drawings.
07/99	1.6	Changed Boundary Scan Information and changed Figure 11, Boundary Scan Bit Sequence. Updated IOB Input & Output delays. Added Capacitance info for different I/O Standards. Added 5 V tolerant information. Added DLL Parameters and waveforms and new Pin-to-pin Input and Output Parameter tables for Global Clock Input to Output and Setup and Hold. Changed Configuration Information including Figures 12, 14, 17 & 19. Added device-dependent listings for quiescent currents ICCINTQ and ICCOQ. Updated IOB Input and Output Delays based on default standard of LVTTL, 12 mA, Fast Slew Rate. Added IOB Input Switching Characteristics Standard Adjustments.
09/99	1.7	Speed grade update to preliminary status, Power-on specification and Clock-to-Out Minimums additions, "0" hold time listing explanation, quiescent current listing update, and Figure 6 ADDRA input label correction. Added T_{IJITCC} parameter, changed T_{OJIT} to T_{OPHASE}.
01/00	1.8	Update to speed.txt file 1.96. Corrections for CRs 111036,111137, 112697, 115479, 117153, 117154, and 117612. Modified notes for Recommended Operating Conditions (voltage and temperature). Changed Bank information for V_{CCO} in CS144 package on p.43.

Date	Version	Revision
01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
03/00	2.0	New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration.
05/00	2.1	Modified "Pins not listed..." statement. Speed grade update to Final status.
05/00	2.2	Modified Table 18.
09/00	2.3	• Added XCV400 values to table under **Minimum Clock-to-Out for Virtex Devices**. • Corrected Units column in table under **IOB Input Switching Characteristics**. • Added values to table under **CLB SelectRAM Switching Characteristics**.
10/00	2.4	• Corrected Pinout information for devices in the BG256, BG432, and BG560 packages in Table 18. • Corrected **BG256 Pin Function Diagram**.
04/02/01	2.5	• Revised minimums for **Global Clock Set-Up and Hold for LVTTL Standard, with DLL**. • Converted file to modularized format. See the **Virtex Data Sheet** section.
04/19/01	2.6	• Clarified TIOCKP and TIOCKON **IOB Output Switching Characteristics** descriptors.
07/19/01	2.7	• Under **Absolute Maximum Ratings**, changed (T_{SOL}) to 220 °C.
07/26/01	2.8	• Removed T_{SOL} parameter and added footnote to **Absolute Maximum Ratings** table.
10/29/01	2.9	• Updated the speed grade designations used in data sheets, and added Table 1, which shows the current speed grade designation for each device.
02/01/02	3.0	• Added footnote to **DC Input and Output Levels** table.
07/19/02	3.1	• Removed mention of MIL-M-38510/605 specification. • Added link to xapp158 from the **Power-On Power Supply Requirements** section.
09/10/02	3.2	• Added Clock CLK to **IOB Input Switching Characteristics** and **IOB Output Switching Characteristics**.
03/01/13	4.0	The products listed in this data sheet are obsolete. See **XCN10016** for further information.

Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

- DS003-1, Virtex 2.5V FPGAs:
  Introduction and Ordering Information (Module 1)

- DS003-2, Virtex 2.5V FPGAs:
  Functional Description (Module 2)

- DS003-3, Virtex 2.5V FPGAs:
  DC and Switching Characteristics (Module 3)

- DS003-4, Virtex 2.5V FPGAs:
  Pinout Tables (Module 4)

Virtex™ 2.5 V
Field Programmable Gate Arrays

DS003-4 (v4.0) March 1, 2013   **Production Product Specification**

Virtex Pin Definitions

Table 1: **Special Purpose Pins**

Pin Name	Dedicated Pin	Direction	Description
GCK0, GCK1, GCK2, GCK3	Yes	Input	Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin: it is an input for SelectMAP and slave-serial modes, and output in master-serial mode. After configuration, it is input only, logic level = Don't Care.
PROGRAM	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output can be open drain.
INIT	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. The pin becomes a user I/O after configuration.
BUSY/ DOUT	No	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration unless the SelectMAP port is retained. In bit-serial modes, DOUT provides header information to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In SelectMAP mode, D0 - D7 are configuration data pins. These pins become user I/Os after configuration unless the SelectMAP port is retained. In bit-serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
WRITE	No	Input	In SelectMAP mode, the active-low Write Enable signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
CS	No	Input	In SelectMAP mode, the active-low Chip Select signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary-scan Test-Access-Port pins, as defined in IEEE 1149.1.
DXN, DXP	Yes	N/A	Temperature-sensing diode pins. (Anode: DXP, cathode: DXN)
V_{CCINT}	Yes	Input	Power-supply pins for the internal core logic.
V_{CCO}	Yes	Input	Power-supply pins for the output drivers (subject to banking rules)
V_{REF}	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground

Table 3: **Virtex Pinout Tables (BGA)** *(Continued)*

Pin Name	Device	BG256	BG352	BG432	BG560
V_{CCO}, Bank 7	All	G4, H4	G23, K26, N23	A31, L28, L31	C32, D33, K33, N32, T33
V_{REF}, Bank 0 (VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	A8, B4	N/A	N/A	N/A
	XCV100/150	... + A4	A16,C19, C21	N/A	N/A
	XCV200/300	... + A2	... + D21	B19, D22, D24, D26	N/A
	XCV400	N/A	N/A	... + C18	A19, D20, D26, E23, E27
	XCV600	N/A	N/A	... + C24	... + E24
	XCV800	N/A	N/A	... + B21	... + E21
	XCV1000	N/A	N/A	N/A	... + D29
V_{REF}, Bank 1 (VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	A17, B12	N/A	N/A	N/A
	XCV100/150	... + B15	B6, C9, C12	N/A	N/A
	XCV200/300	... + B17	... + D6	A13, B7, C6, C10	N/A
	XCV400	N/A	N/A	... + B15	A6, D7, D11, D16, E15
	XCV600	N/A	N/A	... + D10	... + D10
	XCV800	N/A	N/A	... + B12	... + D13
	XCV1000	N/A	N/A	N/A	... + E7
V_{REF}, Bank 2 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	C20, J18	N/A	N/A	N/A
	XCV100/150	... + F19	E2, H2, M4	N/A	N/A
	XCV200/300	... + G18	... + D2	E2, G3, J2, N1	N/A
	XCV400	N/A	N/A	... + R3	G5, H4, L5, P4, R1
	XCV600	N/A	N/A	... + H1	... + K5
	XCV800	N/A	N/A	... + M3	... + N5
	XCV1000	N/A	N/A	N/A	... + B3

XILINX®

Table 4: **Virtex Pinout Tables (Fine-Pitch BGA)**

Pin Name	Device	FG256	FG456	FG676	FG680
GCK0	All	N8	W12	AA14	AW19
GCK1	All	R8	Y11	AB13	AU22
GCK2	All	C9	A11	C13	D21
GCK3	All	B8	C11	E13	A20
M0	All	N3	AB2	AD4	AT37
M1	All	P2	U5	W7	AU38
M2	All	R3	Y4	AB6	AT35
CCLK	All	D15	B22	D24	E4
PROGRAM	All	P15	W20	AA22	AT5
DONE	All	R14	Y19	AB21	AU5
INIT	All	N15	V19	Y21	AU2
BUSY/DOUT	All	C15	C21	E23	E3
D0/DIN	All	D14	D20	F22	C2
D1	All	E16	H22	K24	P4
D2	All	F15	H20	K22	P3
D3	All	G16	K20	M22	R1
D4	All	J16	N22	R24	AD3
D5	All	M16	R21	U23	AG2
D6	All	N16	T22	V24	AH1
D7	All	N14	Y21	AB23	AR4
WRITE	All	C13	A20	C22	B4
CS	All	B13	C19	E21	D5
TDI	All	A15	B20	D22	B3
TDO	All	B14	A21	C23	C4
TMS	All	D3	D3	F5	E36
TCK	All	C4	C4	E6	C36
DXN	All	R4	Y5	AB7	AV37
DXP	All	P4	V6	Y8	AU35

Table 4: **Virtex Pinout Tables (Fine-Pitch BGA)** *(Continued)*

Pin Name	Device	FG256	FG456	FG676	FG680
V_{CCINT}	All	C3, C14, D4, D13, E5, E12, M5, M12, N4, N13, P3, P14	E5, E18, F6, F17, G7, G8, G9, G14, G15, G16, H7, H16, J7, J16, P7, P16, R7, R16, T7, T8, T9, T14, T15, T16, U6, U17, V5, V18	G7, G20, H8, H19, J9, J10, J11, J16, J17, J18, K9, K18, L9, L18, T9, T18, U9, U18, V9, V10, V11, V16, V17, V18, W8, W19, Y7, Y20	AD5, AD35, AE5, AE35, AL5, AL35, AM5, AM35, AR8, AR9, AR15, AR16, AR24, AR25, AR31, AR32, E8, E9, E15, E16, E24, E25, E31, E32, H5, H35, J5, J35, R5, R35, T5, T35
V_{CCO}, Bank 0	All	E8, F8	F7, F8, F9, F10 G10, G11	H9, H10, H11, H12, J12, J13	E26, E27, E29, E30, E33, E34
V_{CCO}, Bank 1	All	E9, F9	F13, F14, F15, F16, G12, G13	H15, H16, H17, H18, J14, J15	E6, E7, E10, E11, E13, E14
V_{CCO}, Bank 2	All	H11, H12	G17, H17, J17, K16, K17, L16	J19, K19, L19, M18, M19, N18	F5, G5, K5, L5, N5, P5
V_{CCO}, Bank 3	All	J11, J12	M16, N16, N17, P17, R17, T17	P18, R18, R19, T19, U19, V19	AF5, AG5, AN5, AK5, AJ5, AP5
V_{CCO}, Bank 4	All	L9. M9	T12, T13, U13, U14, U15, U16,	V14, V15, W15, W16, W17, W18	AR6, AR7, AR10, AR11, AR13, AR14
V_{CCO}, Bank 5	All	L8, M8	T10, T11, U7, U8, U9, U10	V12, V13, W9, W10, W11, W12	AR26, AR27, AR29, AR30, AR33, AR34
V_{CCO}, Bank 6	All	J5, J6	M7, N6, N7, P6, R6, T6	P9, R8, R9, T8, U8, V8	AF35, AG35, AJ35, AK35, AN35, AP35
V_{CCO}, Bank 7	All	H5, H6	G6, H6, J6, K6, K7, L7	J8, K8, L8, M8, M9, N9	F35, G35, K35, L35, N35, P35
V_{REF}, Bank 0 (VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	B4, B7	N/A	N/A	N/A
	XCV100/150	... + C6	A9, C6, E8	N/A	N/A
	XCV200/300	... + A3	... + B4	N/A	N/A
	XCV400	N/A	N/A	A12, C11, D6, E8, G10	
	XCV600	N/A	N/A	... + B7	A33, B28, B30, C23, C24, D33
	XCV800	N/A	N/A	... + B10	... + A26
	XCV1000	N/A	N/A	N/A	... + D34

Table 4: **Virtex Pinout Tables (Fine-Pitch BGA)** *(Continued)*

Pin Name	Device	FG256	FG456	FG676	FG680
V_{REF}, Bank 1 (VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	B9, C11	N/A	N/A	N/A
	XCV100/150	... + E11	A18, B13, E14	N/A	N/A
	XCV200/300	... + A14	... + A19	N/A	N/A
	XCV400	N/A	N/A	A14, C20, C21, D15, G16	N/A
	XCV600	N/A	N/A	... + B19	B6, B8, B18, D11, D13, D17
	XCV800	N/A	N/A	... + A17	... + B14
	XCV1000	N/A	N/A	N/A	... + B5
V_{REF}, Bank 2 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	F13, H13	N/A	N/A	N/A
	XCV100/150	... + F14	F21, H18, K21	N/A	N/A
	XCV200/300	... + E13	... + D22	N/A	N/A
	XCV400	N/A	N/A	F24, H23, K20, M23, M26	N/A
	XCV600	N/A	N/A	... + G26	G1, H4, J1, L2, V5, W3
	XCV800	N/A	N/A	... + K25	... + N1
	XCV1000	N/A	N/A	N/A	... + D2
V_{REF}, Bank 3 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	K16, L14	N/A	N/A	N/A
	XCV100/150	... + L13	N21, R19, U21	N/A	N/A
	XCV200/300	... + M13	... + U20	N/A	N/A
	XCV400	N/A	N/A	R23, R25, U21, W22, W23	N/A
	XCV600	N/A	N/A	... + W26	AC1, AJ2, AK3, AL4, AR1, Y1
	XCV800	N/A	N/A	... + U25	... + AF3
	XCV1000	N/A	N/A	N/A	... + AP4

Table 4: **Virtex Pinout Tables (Fine-Pitch BGA)** *(Continued)*

| Pin Name	Device	FG256	FG456	FG676	FG680
V$_{REF}$, Bank 4 (V$_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V$_{REF}$ pins are general I/O.	XCV50	P9, T12	N/A	N/A	N/A
	XCV100/150	... + T11	AA13, AB16, AB19	N/A	N/A
	XCV200/300	... + R13	... + AB20	N/A	N/A
	XCV400	N/A	N/A	AC15, AD18, AD21, AD22, AF15	N/A
	XCV600	N/A	N/A	... + AF20	AT19, AU7, AU17, AV8, AV10, AW11
	XCV800	N/A	N/A	... + AF17	... + AV14
	XCV1000	N/A	N/A	N/A	... + AU6
V$_{REF}$, Bank 5 (V$_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V$_{REF}$ pins are general I/O.	XCV50	T4, P8	N/A	N/A	N/A
	XCV100/150	... + R5	W8, Y10, AA5	N/A	N/A
	XCV200/300	... + T2	... + Y6	N/A	N/A
	XCV400	N/A	N/A	AA10, AB8, AB12, AC7, AF12	N/A
	XCV600	N/A	N/A	... + AF8	AT27, AU29, AU31, AV35, AW21, AW23
	XCV800	N/A	N/A	... + AE10	... + AT25
	XCV1000	N/A	N/A	N/A	... + AV36
V$_{REF}$, Bank 6 (V$_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V$_{REF}$ pins are general I/O.	XCV50	J3, N1	N/A	N/A	N/A
	XCV100/150	... + M1	N2, R4, T3	N/A	N/A
	XCV200/300	... + N2	... + Y1	N/A	N/A
	XCV400	N/A	N/A	AB3, R1, R4, U6, V5	N/A
	XCV600	N/A	N/A	... + Y1	AB35, AD37, AH39, AK39, AM39, AN36
	XCV800	N/A	N/A	... + U2	... + AE39
	XCV1000	N/A	N/A	N/A	... + AT39

BG256 Pin Function Diagram
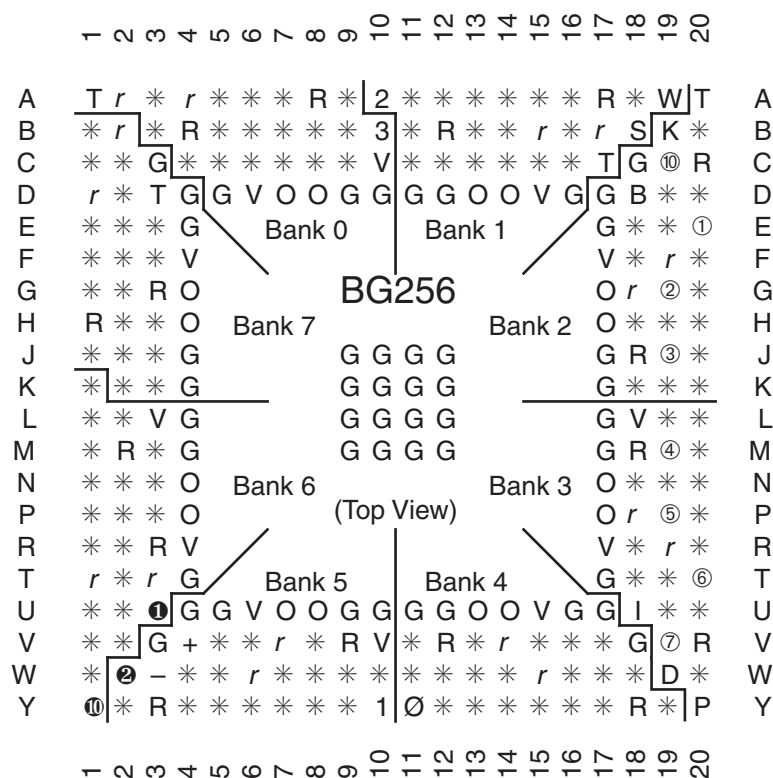
Figure 4: **BG256 Pin Function Diagram**

BG352 Pin Function Diagram
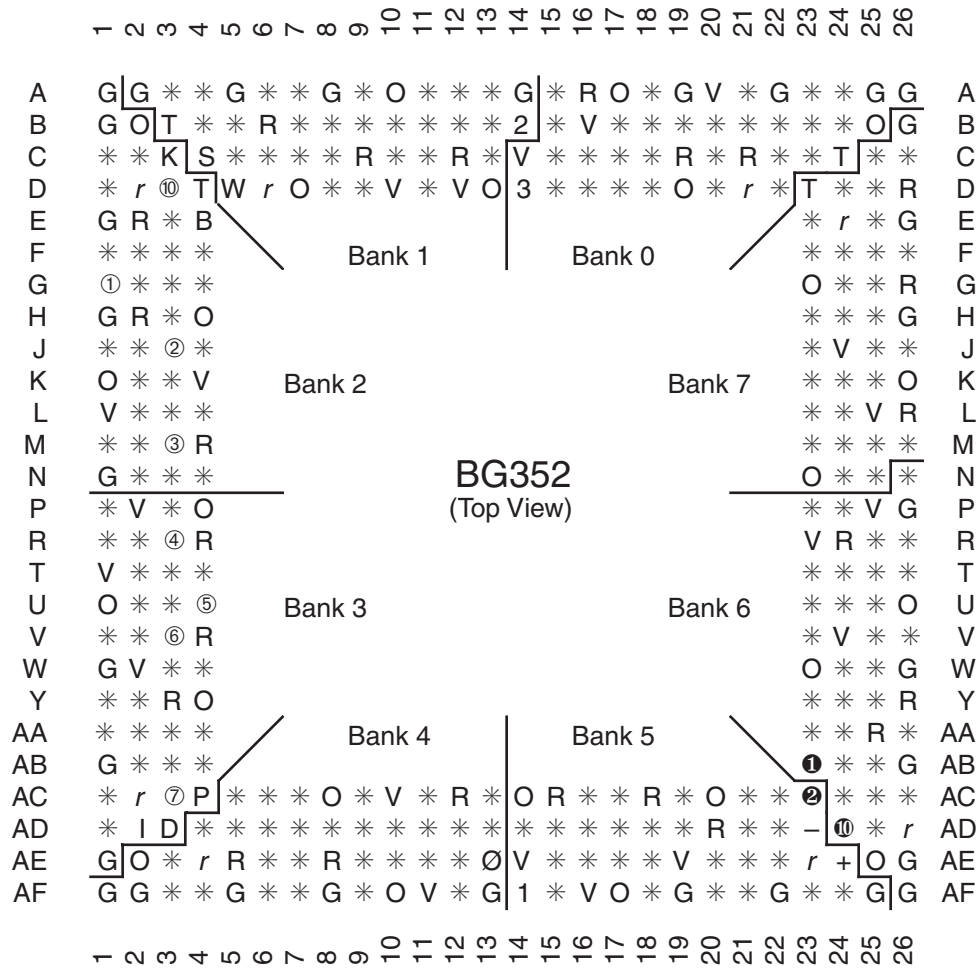
DS003_19_100600

Figure 5: **BG352 Pin Function Diagram**