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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	6144
Number of Logic Elements/Cells	27648
Total RAM Bits	131072
Number of I/O	512
Number of Gates	1124022
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	680-LBGA Exposed Pad
Supplier Device Package	680-FTEBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv1000-4fg680c

Virtex Architecture

Virtex devices feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing resources. The abundance of routing resources permits the Virtex family to accommodate even the largest and most complex designs.

Virtex FPGAs are SRAM-based, and are customized by loading configuration data into internal memory cells. In some modes, the FPGA reads its own configuration data from an external PROM (master serial mode). Otherwise, the configuration data is written into the FPGA (SelectMAP™, slave serial, and JTAG modes).

The standard Xilinx Foundation™ and Alliance Series™ Development systems deliver complete design support for Virtex, covering every aspect from behavioral and schematic entry, through simulation, automatic design translation and implementation, to the creation, downloading, and readback of a configuration bit stream.

Higher Performance

Virtex devices provide better performance than previous generations of FPGA. Designs can achieve synchronous system clock rates up to 200 MHz including I/O. Virtex inputs and outputs comply fully with PCI specifications, and interfaces can be implemented that operate at 33 MHz or 66 MHz. Additionally, Virtex supports the hot-swapping requirements of Compact PCI.

Xilinx thoroughly benchmarked the Virtex family. While performance is design-dependent, many designs operated internally at speeds in excess of 100 MHz and can achieve 200 MHz. Table 2 shows performance data for representative circuits, using worst-case timing parameters.

Table 2: **Performance for Common Circuit Functions**

Function	Bits	Virtex -6
Register-to-Register		
Adder	16	5.0 ns
	64	7.2 ns
Pipelined Multiplier	8 x 8	5.1 ns
	16 x 16	6.0 ns
Address Decoder	16	4.4 ns
	64	6.4 ns
16:1 Multiplexer		5.4 ns
Parity Tree	9	4.1 ns
	18	5.0 ns
	36	6.9 ns
Chip-to-Chip		
HSTL Class IV		200 MHz
LVTTL,16mA, fast slew		180 MHz

Virtex Device/Package Combinations and Maximum I/O

Table 3: **Virtex Family Maximum User I/O by Device/Package (Excluding Dedicated Clock Pins)**

Package	XCV50	XCV100	XCV150	XCV200	XCV300	XCV400	XCV600	XCV800	XCV1000
CS144	94	94							
TQ144	98	98							
PQ240	166	166	166	166	166				
HQ240						166	166	166	
BG256	180	180	180	180					
BG352			260	260	260				
BG432					316	316	316	316	
BG560						404	404	404	404
FG256	176	176	176	176					
FG456			260	284	312				
FG676						404	444	444	
FG680							512	512	512

Virtex Ordering Information

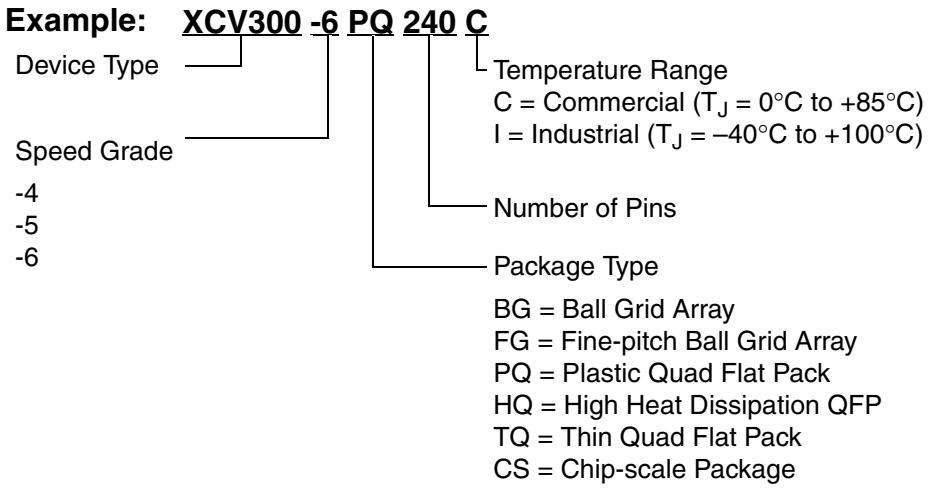

Figure 1: **Virtex Ordering Information**

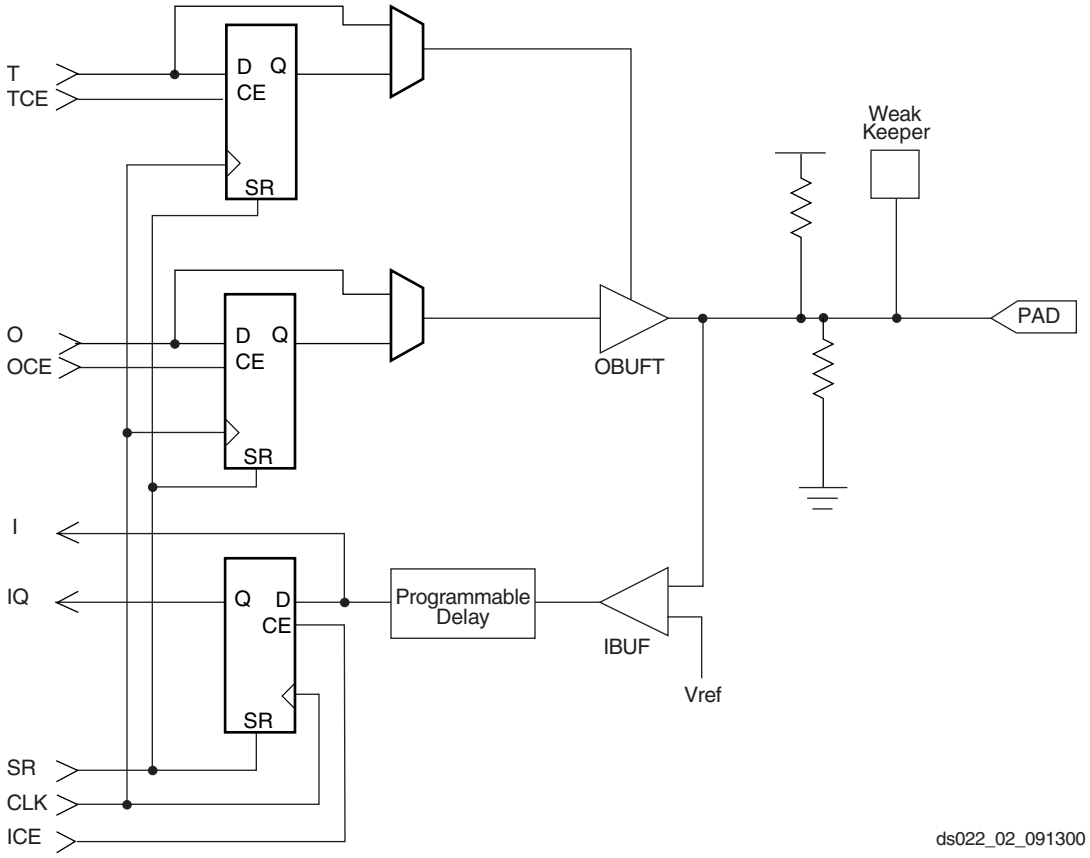

Figure 2: **Virtex Input/Output Block (IOB)**

Table 1: **Supported Select I/O Standards**

I/O Standard	Input Reference Voltage (V_{REF})	Output Source Voltage (V_{CCO})	Board Termination Voltage (V_{TT})	5 V Tolerant
LVTTL 2 – 24 mA	N/A	3.3	N/A	Yes
LVCMOS2	N/A	2.5	N/A	Yes
PCI, 5 V	N/A	3.3	N/A	Yes
PCI, 3.3 V	N/A	3.3	N/A	No
GTL	0.8	N/A	1.2	No
GTL+	1.0	N/A	1.5	No
HSTL Class I	0.75	1.5	0.75	No
HSTL Class III	0.9	1.5	1.5	No
HSTL Class IV	0.9	1.5	1.5	No
SSTL3 Class I &II	1.5	3.3	1.5	No
SSTL2 Class I & II	1.25	2.5	1.25	No
CTT	1.5	3.3	1.5	No
AGP	1.32	3.3	N/A	No

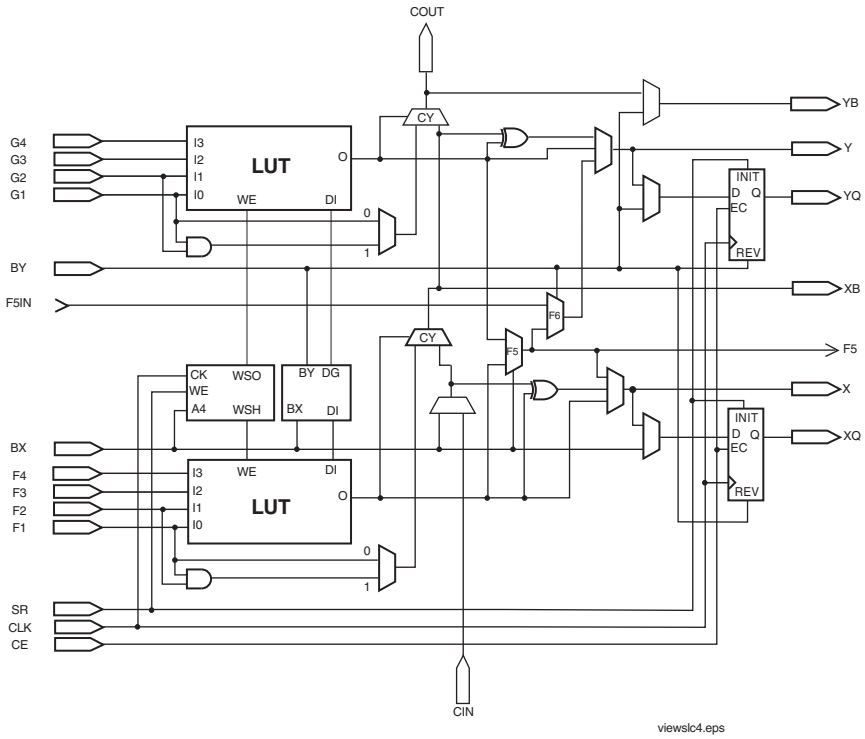

Figure 5: **Detailed View of Virtex Slice**

Additional Logic

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Each CLB has four direct feedthrough paths, one per LC. These paths provide extra data input lines or additional local routing that does not consume logic resources.

Arithmetic Logic

Dedicated carry logic provides fast arithmetic carry capability for high-speed arithmetic functions. The Virtex CLB supports two separate carry chains, one per Slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 1-bit full adder to be implemented within an LC. In addition, a dedicated AND gate improves the efficiency of multiplier implementation.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

BUFTs

Each Virtex CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. See **Dedicated Routing**, page 7. Each Virtex BUFT has an independent 3-state control pin and an independent input pin.

Block SelectRAM

Virtex FPGAs incorporate several large block SelectRAM memories. These complement the distributed LUT SelectRAMs that provide shallow RAM structures implemented in CLBs.

Block SelectRAM memory blocks are organized in columns. All Virtex devices contain two such columns, one along each vertical edge. These columns extend the full height of the chip. Each memory block is four CLBs high, and consequently, a Virtex device 64 CLBs high contains 16 memory blocks per column, and a total of 32 blocks.

Table 3 shows the amount of block SelectRAM memory that is available in each Virtex device.

Table 3: **Virtex Block SelectRAM Amounts**

Device	# of Blocks	Total Block SelectRAM Bits
XCV50	8	32,768
XCV100	10	40,960
XCV150	12	49,152
XCV200	14	57,344
XCV300	16	65,536
XCV400	20	81,920
XCV600	24	98,304
XCV800	28	114,688
XCV1000	32	131,072

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

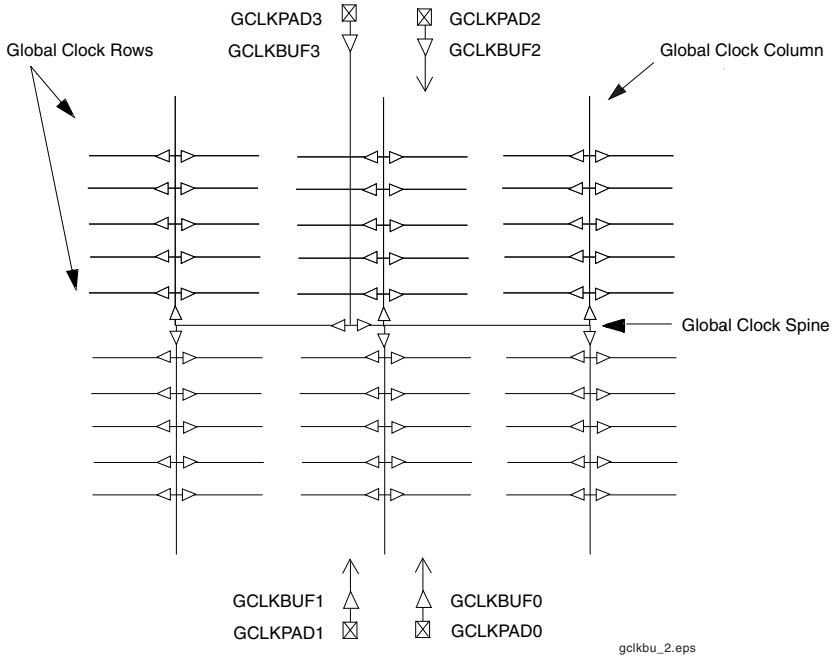

Figure 9: **Global Clock Distribution Network**

Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks.The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Clock edges reach internal flip-flops one to four clock periods after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to de-skew a board level clock among multiple Virtex devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

See **DLL Timing Parameters**, page 21 of Module 3, for frequency range information.

Boundary Scan

Virtex devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, and HIGHZ instructions. The TAP also supports two internal scan chains and configuration/readback of the device.The TAP uses dedicated package pins that always operate using LVTTL. For TDO to operate using LVTTL, the V_{CCO} for Bank 2 should be 3.3 V. Otherwise, TDO switches rail-to-rail between ground and V_{CCO}.

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including un-bonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections, provided the user design or application is turned off.

Table 5 lists the boundary-scan instructions supported in Virtex FPGAs. Internal signals can be captured during EXTEST by connecting them to un-bonded or unused IOBs. They can also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Before the device is configured, all instructions except USER1 and USER2 are available. After configuration, all instructions are available. During configuration, it is recommended that those operations using the boundary-scan register (SAMPLE/PRELOAD, INTEST, EXTEST) not be performed.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device(1) from 0 V. The current is highest at the fastest suggested ramp rate (0 V to nominal voltage in 2 ms) and is lowest at the slowest allowed ramp rate (0 V to nominal voltage in 50 ms). For more details on power supply requirements, see Application Note XAPP158 on www.xilinx.com.

Product	Description(2)	Current Requirement(1,3)
Virtex Family, Commercial Grade	Minimum required current supply	500 mA
Virtex Family, Industrial Grade	Minimum required current supply	2 A

Notes:
1. Ramp rate used for this specification is from 0 - 2.7 VDC. Peak current occurs on or near the internal power-on reset threshold of 1.0V and lasts for less than 3 ms.
2. Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
3. Larger currents can result if ramp rates are forced to be faster.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed output currents over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} for each standard with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTL(1)	– 0.5	0.8	2.0	5.5	0.4	2.4	24	–24
LVCMOS2	– 0.5	.7	1.7	5.5	0.4	1.9	12	–12
PCI, 3.3 V	– 0.5	44% V_{CCINT}	60% V_{CCINT}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI, 5.0 V	– 0.5	0.8	2.0	5.5	0.55	2.4	Note 2	Note 2
GTL	– 0.5	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	n/a	40	n/a
GTL+	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	n/a	36	n/a
HSTL I(3)	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	8	–8
HSTL III	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	24	–8
HSTL IV	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	48	–8
SSTL3 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.61	V_{REF} + 0.61	7.6	–7.6
SSTL2 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.80	V_{REF} + 0.80	15.2	–15.2
CTT	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.4	V_{REF} + 0.4	8	–8
AGP	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested.
2. Tested according to the relevant specifications.
3. DC input and output levels for HSTL18 (HSTL I/O standard with V_{CCO} of 1.8 V) are provided in an HSTL white paper on www.xilinx.com.

IOB Input Switching Characteristics Standard Adjustments

Description	Symbol	Standard(1)	Speed Grade				Units
			Min	-6	-5	-4	
Data Input Delay Adjustments							
Standard-specific data input delay adjustments	T_{ILVTTL}	LVTTL	0	0	0	0	ns
	$T_{ILVCMOS2}$	LVCMOS2	–0.02	–0.04	–0.04	–0.05	ns
	T_{IPCI33_3}	PCI, 33 MHz, 3.3 V	–0.05	–0.11	–0.12	–0.14	ns
	T_{IPCI33_5}	PCI, 33 MHz, 5.0 V	0.13	0.25	0.28	0.33	ns
	T_{IPCI66_3}	PCI, 66 MHz, 3.3 V	–0.05	–0.11	–0.12	–0.14	ns
	T_{IGTL}	GTL	0.10	0.20	0.23	0.26	ns
	T_{IGTLP}	GTL+	0.06	0.11	0.12	0.14	ns
	T_{IHSTL}	HSTL	0.02	0.03	0.03	0.04	ns
	T_{ISSTL2}	SSTL2	–0.04	–0.08	–0.09	–0.10	ns
	T_{ISSTL3}	SSTL3	–0.02	–0.04	–0.05	–0.06	ns
	T_{ICTT}	CTT	0.01	0.02	0.02	0.02	ns
	T_{IAGP}	AGP	–0.03	–0.06	–0.07	–0.08	ns

Notes:
1. Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see Table 3.

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 9.

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Propagation Delays						
O input to Pad	T_{IOOP}	1.2	2.9	3.2	3.5	ns, max
O input to Pad via transparent latch	T_{IOOLP}	1.4	3.4	3.7	4.0	ns, max
3-State Delays						
T input to Pad high-impedance(1)	T_{IOTHZ}	1.0	2.0	2.2	2.4	ns, max
T input to valid data on Pad	T_{IOTON}	1.4	3.1	3.3	3.7	ns, max
T input to Pad high-impedance via transparent latch(1)	$T_{IOTLPHZ}$	1.2	2.4	2.6	3.0	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$	1.6	3.5	3.8	4.2	ns, max
GTS to Pad high impedance(1)	T_{GTS}	2.5	4.9	5.5	6.3	ns, max
Sequential Delays						
Clock CLK						
Minimum Pulse Width, High	T_{CH}	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low	T_{CL}	0.8	1.5	1.7	2.0	ns, min

I/O Standard Global Clock Input Adjustments

Description	Symbol	Standard(1)	Speed Grade				Units
			Min	-6	-5	-4	
Data Input Delay Adjustments							
Standard-specific global clock input delay adjustments	$T_{GPLVTTL}$	LVTTL	0	0	0	0	ns, max
	$T_{GPLVCMOS2}$	LVCMOS2	–0.02	–0.04	–0.04	–0.05	ns, max
	$T_{GPPCI33\_3}$	PCI, 33 MHz, 3.3 V	–0.05	–0.11	–0.12	–0.14	ns, max
	$T_{GPPCI33\_5}$	PCI, 33 MHz, 5.0 V	0.13	0.25	0.28	0.33	ns, max
	$T_{GPPCI66\_3}$	PCI, 66 MHz, 3.3 V	–0.05	–0.11	–0.12	–0.14	ns, max
	T_{GPGTL}	GTL	0.7	0.8	0.9	0.9	ns, max
	T_{GPGTLP}	GTL+	0.7	0.8	0.8	0.8	ns, max
	T_{GPHSTL}	HSTL	0.7	0.7	0.7	0.7	ns, max
	$T_{GPSSTL2}$	SSTL2	0.6	0.52	0.51	0.50	ns, max
	$T_{GPSSTL3}$	SSTL3	0.6	0.6	0.55	0.54	ns, max
	T_{GPCTT}	CTT	0.7	0.7	0.7	0.7	ns, max
	T_{GPAGP}	AGP	0.6	0.54	0.53	0.52	ns, max

Notes:
1. Input timing for GPLVTTL is measured at 1.4 V. For other I/O standards, see Table 3.

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Combinatorial Delays						
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.29	0.6	0.7	0.8	ns, max
5-input function: F/G inputs to F5 output	T_{IF5}	0.32	0.7	0.8	0.9	ns, max
5-input function: F/G inputs to X output	T_{IF5X}	0.36	0.8	0.8	1.0	ns, max
6-input function: F/G inputs to Y output via F6 MUX	T_{IF6Y}	0.44	0.9	1.0	1.2	ns, max
6-input function: F5IN input to Y output	T_{F5INY}	0.17	0.32	0.36	0.42	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.31	0.7	0.7	0.8	ns, max
BY input to YB output	T_{BYYB}	0.27	0.53	0.6	0.7	ns, max
Sequential Delays						
FF Clock CLK to XQ/YQ outputs	T_{CKO}	0.54	1.1	1.2	1.4	ns, max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.6	1.2	1.4	1.6	ns, max
Setup and Hold Times before/after Clock CLK(1)	Setup Time / Hold Time					
4-input function: F/G Inputs	T_{ICK}/T_{CKI}	0.6 / 0	1.2 / 0	1.4 / 0	1.5 / 0	ns, min
5-input function: F/G inputs	T_{IF5CK}/T_{CKIF5}	0.7 / 0	1.3 / 0	1.5 / 0	1.7 / 0	ns, min
6-input function: F5IN input	T_{F5INCK}/T_{CKF5IN}	0.46 / 0	1.0 / 0	1.1 / 0	1.2 / 0	ns, min
6-input function: F/G inputs via F6 MUX	T_{IF6CK}/T_{CKIF6}	0.8 / 0	1.5 / 0	1.7 / 0	1.9 / 0	ns, min
BX/BY inputs	T_{DICK}/T_{CKDI}	0.30 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
CE input	T_{CECK}/T_{CKCE}	0.37 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
SR/BY inputs (synchronous)	$T_{RCK}T_{CKR}$	0.33 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{CH}	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low	T_{CL}	0.8	1.5	1.7	2.0	ns, min
Set/Reset						
Minimum Pulse Width, SR/BY inputs	T_{RPW}	1.3	2.5	2.8	3.3	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}	0.54	1.1	1.3	1.4	ns, max
Delay from GSR to XQ/YQ outputs	T_{IOGSRQ}	4.9	9.7	10.9	12.5	ns, max
Toggle Frequency (MHz) (for export control)	F_{TOG} (MHz)	625	333	294	250	MHz

Notes:
1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Combinatorial Delays						
F operand inputs to X via XOR	T_{OPX}	0.37	0.8	0.9	1.0	ns, max
F operand input to XB output	T_{OPXB}	0.54	1.1	1.3	1.4	ns, max
F operand input to Y via XOR	T_{OPY}	0.8	1.5	1.7	2.0	ns, max
F operand input to YB output	T_{OPYB}	0.8	1.5	1.7	2.0	ns, max
F operand input to COUT output	T_{OPCYF}	0.6	1.2	1.3	1.5	ns, max
G operand inputs to Y via XOR	T_{OPGY}	0.46	1.0	1.1	1.2	ns, max
G operand input to YB output	T_{OPGYB}	0.8	1.6	1.8	2.1	ns, max
G operand input to COUT output	T_{OPCYG}	0.7	1.3	1.4	1.6	ns, max
BX initialization input to COUT	T_{BXCY}	0.41	0.9	1.0	1.1	ns, max
CIN input to X output via XOR	T_{CINX}	0.21	0.41	0.46	0.53	ns, max
CIN input to XB	T_{CINXB}	0.02	0.04	0.05	0.06	ns, max
CIN input to Y via XOR	T_{CINY}	0.23	0.46	0.52	0.6	ns, max
CIN input to YB	T_{CINYB}	0.23	0.45	0.51	0.6	ns, max
CIN input to COUT output	T_{BYP}	0.05	0.09	0.10	0.11	ns, max
Multiplier Operation						
F1/2 operand inputs to XB output via AND	T_{FANDXB}	0.18	0.36	0.40	0.46	ns, max
F1/2 operand inputs to YB output via AND	T_{FANDYB}	0.40	0.8	0.9	1.1	ns, max
F1/2 operand inputs to COUT output via AND	T_{FANDCY}	0.22	0.43	0.48	0.6	ns, max
G1/2 operand inputs to YB output via AND	T_{GANDYB}	0.25	0.50	0.6	0.7	ns, max
G1/2 operand inputs to COUT output via AND	T_{GANDCY}	0.07	0.13	0.15	0.17	ns, max
Setup and Hold Times before/after Clock CLK(1)	Setup Time / Hold Time					
CIN input to FFX	T_{CCKX}/T_{CKCX}	0.50 / 0	1.0 / 0	1.2 / 0	1.3 / 0	ns, min
CIN input to FFY	T_{CCKY}/T_{CKCY}	0.53 / 0	1.1 / 0	1.2 / 0	1.4 / 0	ns, min

Notes:
1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Minimum Clock-to-Out for Virtex Devices

I/O Standard	With DLL	Without DLL									
	All Devices	V50	V100	V150	V200	V300	V400	V600	V800	V1000	Units
*LVTTL_S2	5.2	6.0	6.0	6.0	6.0	6.1	6.1	6.1	6.1	6.1	ns
*LVTTL_S4	3.5	4.3	4.3	4.3	4.3	4.4	4.4	4.4	4.4	4.4	ns
*LVTTL_S6	2.8	3.6	3.6	3.6	3.6	3.7	3.7	3.7	3.7	3.7	ns
*LVTTL_S8	2.2	3.1	3.1	3.1	3.1	3.1	3.1	3.2	3.2	3.2	ns
*LVTTL_S12	2.0	2.9	2.9	2.9	2.9	2.9	2.9	3.0	3.0	3.0	ns
*LVTTL_S16	1.9	2.8	2.8	2.8	2.8	2.8	2.8	2.9	2.9	2.9	ns
*LVTTL_S24	1.8	2.6	2.6	2.7	2.7	2.7	2.7	2.7	2.7	2.8	ns
*LVTTL_F2	2.9	3.8	3.8	3.8	3.8	3.8	3.8	3.9	3.9	3.9	ns
*LVTTL_F4	1.7	2.6	2.6	2.6	2.6	2.6	2.6	2.7	2.7	2.7	ns
*LVTTL_F6	1.2	2.0	2.0	2.0	2.1	2.1	2.1	2.1	2.1	2.2	ns
*LVTTL_F8	1.1	1.9	1.9	1.9	1.9	2.0	2.0	2.0	2.0	2.0	ns
*LVTTL_F12	1.0	1.8	1.8	1.8	1.8	1.9	1.9	1.9	1.9	1.9	ns
*LVTTL_F16	0.9	1.7	1.8	1.8	1.8	1.8	1.8	1.8	1.9	1.9	ns
*LVTTL_F24	0.9	1.7	1.7	1.7	1.8	1.8	1.8	1.8	1.8	1.9	ns
LVCMOS2	1.1	1.9	1.9	1.9	2.0	2.0	2.0	2.0	2.0	2.1	ns
PCI33_3	1.5	2.4	2.4	2.4	2.4	2.4	2.4	2.5	2.5	2.5	ns
PCI33_5	1.4	2.2	2.2	2.3	2.3	2.3	2.3	2.3	2.3	2.4	ns
PCI66_3	1.1	1.9	1.9	2.0	2.0	2.0	2.0	2.0	2.1	2.1	ns
GTL	1.6	2.5	2.5	2.5	2.5	2.5	2.5	2.6	2.6	2.6	ns
GTL+	1.7	2.5	2.5	2.6	2.6	2.6	2.6	2.6	2.6	2.7	ns
HSTL I	1.1	1.9	1.9	1.9	1.9	2.0	2.0	2.0	2.0	2.0	ns
HSTL III	0.9	1.7	1.7	1.8	1.8	1.8	1.8	1.8	1.8	1.9	ns
HSTL IV	0.8	1.6	1.6	1.6	1.7	1.7	1.7	1.7	1.7	1.8	ns
SSTL2 I	0.9	1.7	1.7	1.7	1.7	1.8	1.8	1.8	1.8	1.8	ns
SSTL2 II	0.8	1.6	1.6	1.6	1.6	1.7	1.7	1.7	1.7	1.7	ns
SSTL3 I	0.8	1.6	1.7	1.7	1.7	1.7	1.7	1.7	1.8	1.8	ns
SSTL3 II	0.7	1.5	1.5	1.6	1.6	1.6	1.6	1.6	1.6	1.7	ns
CTT	1.0	1.8	1.8	1.8	1.9	1.9	1.9	1.9	1.9	2.0	ns
AGP	1.0	1.8	1.8	1.9	1.9	1.9	1.9	1.9	1.9	2.0	ns

*S = Slow Slew Rate, F = Fast Slew Rate

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Input and output timing is measured at 1.4 V for LVTTL. For other I/O standards, see Table 3. In all cases, an 8 pF external capacitive load is used.

Global Clock Set-Up and Hold for LVTTL Standard, *without* DLL

Description	Symbol	Device	Speed Grade				Units
			Min	-6	-5	-4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard.(2) For data input with different standards, adjust the setup time delay by the values shown in Input Delay Adjustments.							
Full Delay Global Clock and IFF, without DLL	T_{PSFD}/T_{PHFD}	XCV50	0.6 / 0	2.3 / 0	2.6 / 0	2.9 / 0	ns, min
		XCV100	0.6 / 0	2.3 / 0	2.6 / 0	3.0 / 0	ns, min
		XCV150	0.6 / 0	2.4 / 0	2.7 / 0	3.1 / 0	ns, min
		XCV200	0.7 / 0	2.5 / 0	2.8 / 0	3.2 / 0	ns, min
		XCV300	0.7 / 0	2.5 / 0	2.8 / 0	3.2 / 0	ns, min
		XCV400	0.7 / 0	2.6 / 0	2.9 / 0	3.3 / 0	ns, min
		XCV600	0.7 / 0	2.6 / 0	2.9 / 0	3.3 / 0	ns, min
		XCV800	0.7 / 0	2.7 / 0	3.1 / 0	3.5 / 0	ns, min
		XCV1000	0.7 / 0	2.8 / 0	3.1 / 0	3.6 / 0	ns, min

IFF = Input Flip-Flop or Latch

Notes: Notes:

1. Set-up time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
2. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Virtex Pin Definitions

Table 1: **Special Purpose Pins**

Pin Name	Dedicated Pin	Direction	Description
GCK0, GCK1, GCK2, GCK3	Yes	Input	Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin: it is an input for SelectMAP and slave-serial modes, and output in master-serial mode. After configuration, it is input only, logic level = Don't Care.
PROGRAM	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output can be open drain.
INIT	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. The pin becomes a user I/O after configuration.
BUSY/ DOUT	No	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration unless the SelectMAP port is retained. In bit-serial modes, DOUT provides header information to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In SelectMAP mode, D0 - D7 are configuration data pins. These pins become user I/Os after configuration unless the SelectMAP port is retained. In bit-serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
WRITE	No	Input	In SelectMAP mode, the active-low Write Enable signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
CS	No	Input	In SelectMAP mode, the active-low Chip Select signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary-scan Test-Access-Port pins, as defined in IEEE 1149.1.
DXN, DXP	Yes	N/A	Temperature-sensing diode pins. (Anode: DXP, cathode: DXN)
V_{CCINT}	Yes	Input	Power-supply pins for the internal core logic.
V_{CCO}	Yes	Input	Power-supply pins for the output drivers (subject to banking rules)
V_{REF}	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground

Table 2: **Virtex Pinout Tables (Chip-Scale and QFP Packages)** ***(Continued)***

Pin Name	Device	CS144	TQ144	PQ/HQ240
V_{REF}, Bank 6 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	H2, K1	116, 123	36, 50
	XCV100/150	... + J3	... + 118	... + 47
	XCV200/300	N/A	N/A	... + 54
	XCV400	N/A	N/A	... + 33
	XCV600	N/A	N/A	... + 48
	XCV800	N/A	N/A	... + 40
V_{REF}, Bank 7 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	D4, E1	133, 140	9, 23
	XCV100/150	... + D2	... + 138	... + 12
	XCV200/300	N/A	N/A	... + 5
	XCV400	N/A	N/A	... + 26
	XCV600	N/A	N/A	... + 11
	XCV800	N/A	N/A	... + 19
GND	All	A1, B9, B11, C7, D5, E4, E11, F1, G10, J1, J12, L3, L5, L7, L9, N12	9, 18, 26, 35, 46, 54, 64, 75, 83, 91, 100, 111, 120, 129, 136, 144,	1, 8, 14, 22, 29, 37, 45, 51, 59, 69, 75, 83, 91, 98, 106, 112, 119, 129, 135, 143, 151, 158, 166, 172, 182, 190, 196, 204, 211, 219, 227, 233

Table 4: **Virtex Pinout Tables (Fine-Pitch BGA) *(Continued)***

Pin Name	Device	FG256	FG456	FG676	FG680
V_{REF}, Bank 1 (VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	B9, C11	N/A	N/A	N/A
	XCV100/150	... + E11	A18, B13, E14	N/A	N/A
	XCV200/300	... + A14	... + A19	N/A	N/A
	XCV400	N/A	N/A	A14, C20, C21, D15, G16	N/A
	XCV600	N/A	N/A	... + B19	B6, B8, B18, D11, D13, D17
	XCV800	N/A	N/A	... + A17	... + B14
	XCV1000	N/A	N/A	N/A	... + B5
V_{REF}, Bank 2 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	F13, H13	N/A	N/A	N/A
	XCV100/150	... + F14	F21, H18, K21	N/A	N/A
	XCV200/300	... + E13	... + D22	N/A	N/A
	XCV400	N/A	N/A	F24, H23, K20, M23, M26	N/A
	XCV600	N/A	N/A	... + G26	G1, H4, J1, L2, V5, W3
	XCV800	N/A	N/A	... + K25	... + N1
	XCV1000	N/A	N/A	N/A	... + D2
V_{REF}, Bank 3 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	K16, L14	N/A	N/A	N/A
	XCV100/150	... + L13	N21, R19, U21	N/A	N/A
	XCV200/300	... + M13	... + U20	N/A	N/A
	XCV400	N/A	N/A	R23, R25, U21, W22, W23	N/A
	XCV600	N/A	N/A	... + W26	AC1, AJ2, AK3, AL4, AR1, Y1
	XCV800	N/A	N/A	... + U25	... + AF3
	XCV1000	N/A	N/A	N/A	... + AP4

Table 4: **Virtex Pinout Tables (Fine-Pitch BGA) *(Continued)***

Pin Name	Device	FG256	FG456	FG676	FG680
No Connect (No-connect pins are listed incrementally. All pins listed for both the required device and all larger devices listed in the same package are no connects.)	XCV800	N/A	N/A	A2, A3, A15, A25, B1, B6, B11, B16, B21, B24, B26, C1, C2, C25, C26, F2, F6, F21, F25, L2, L25, N25, P2, T2, T25, AA2, AA6, AA21, AA25, AD1, AD2, AD25, AE1, AE3, AE6, AE11, AE14, AE16, AE21, AE24, AE26, AF2, AF24, AF25	N/A
	XCV600	N/A	N/A	same as above	N/A
	XCV400	N/A	N/A	... + A9, A10, A13, A16, A24, AC1, AC25, AE12, AE15, AF3, AF10, AF11, AF13, AF14, AF16, AF18, AF23, B4, B12, B13, B15, B17, D1, D25, H26, J1, K26, L1, M1, M25, N1, N26, P1, P26, R2, R26, T1, T26, U26, V1	N/A
	XCV300	N/A	D4, D19, W4, W19	N/A	N/A
	XCV200	N/A	... + A2, A6, A12, B11, B16, C2, D1, D18, E17, E19, G2, G22, L2, L19, M2, M21, R3, R20, U3, U18, Y22, AA1, AA3, AA11, AA16, AB7, AB12, AB21,	N/A	N/A
	XCV150	N/A	... + A13, A14, C8, C9, E13, F11, H21, J1, J4, K2, K18, K19, M17, N1, P1, P5, P22, R22, W13, W15, AA9, AA10, AB8, AB14	N/A	N/A

BG352 Pin Function Diagram

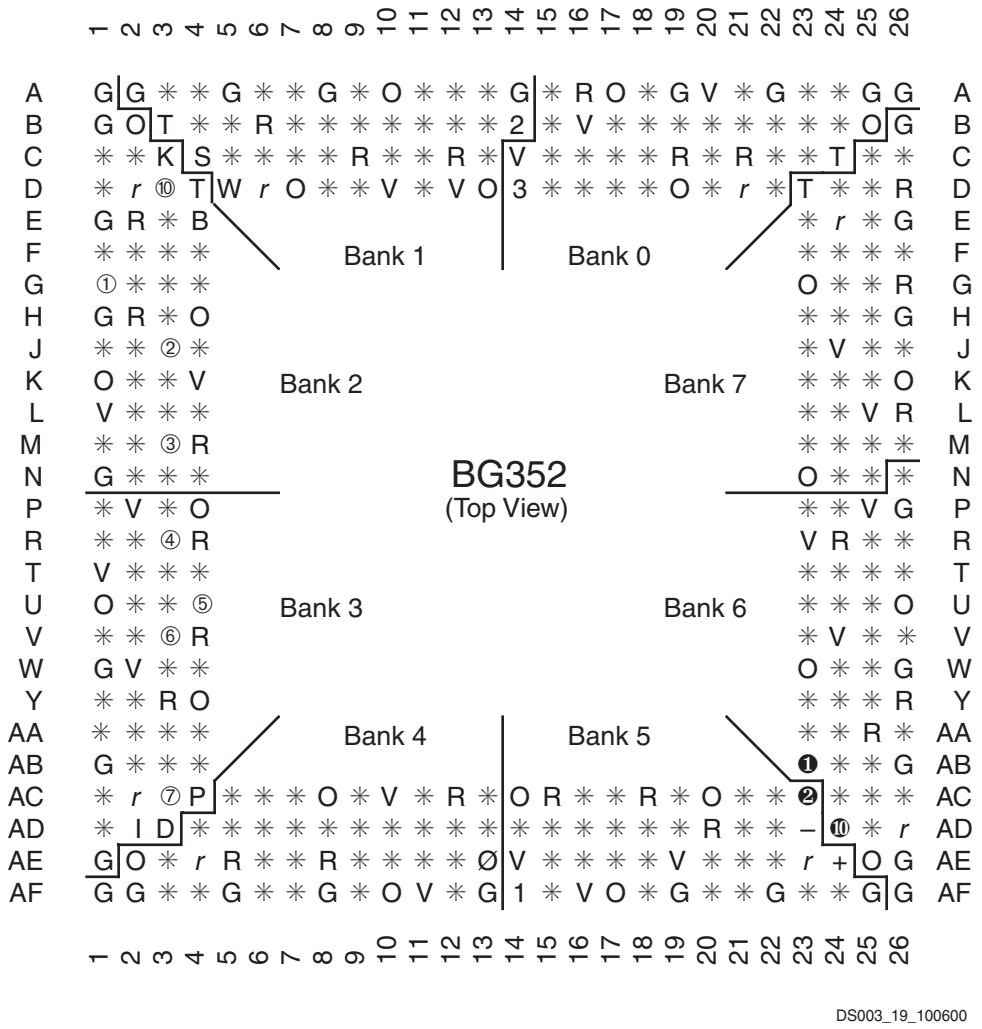

Figure 5: **BG352 Pin Function Diagram**

BG560 Pin Function Diagram

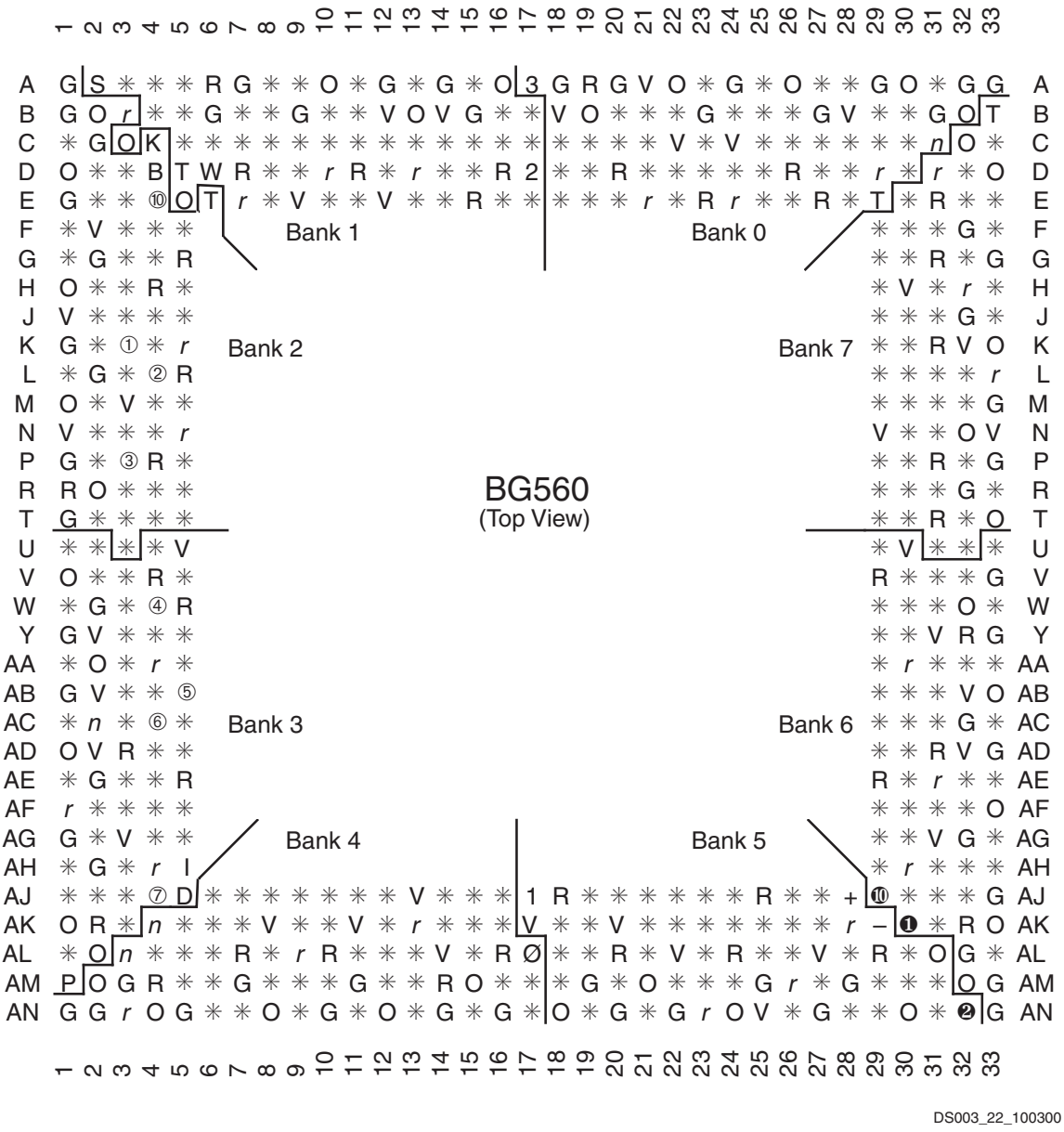

Figure 7: **BG560 Pin Function Diagram**

FG676 Pin Function Diagram

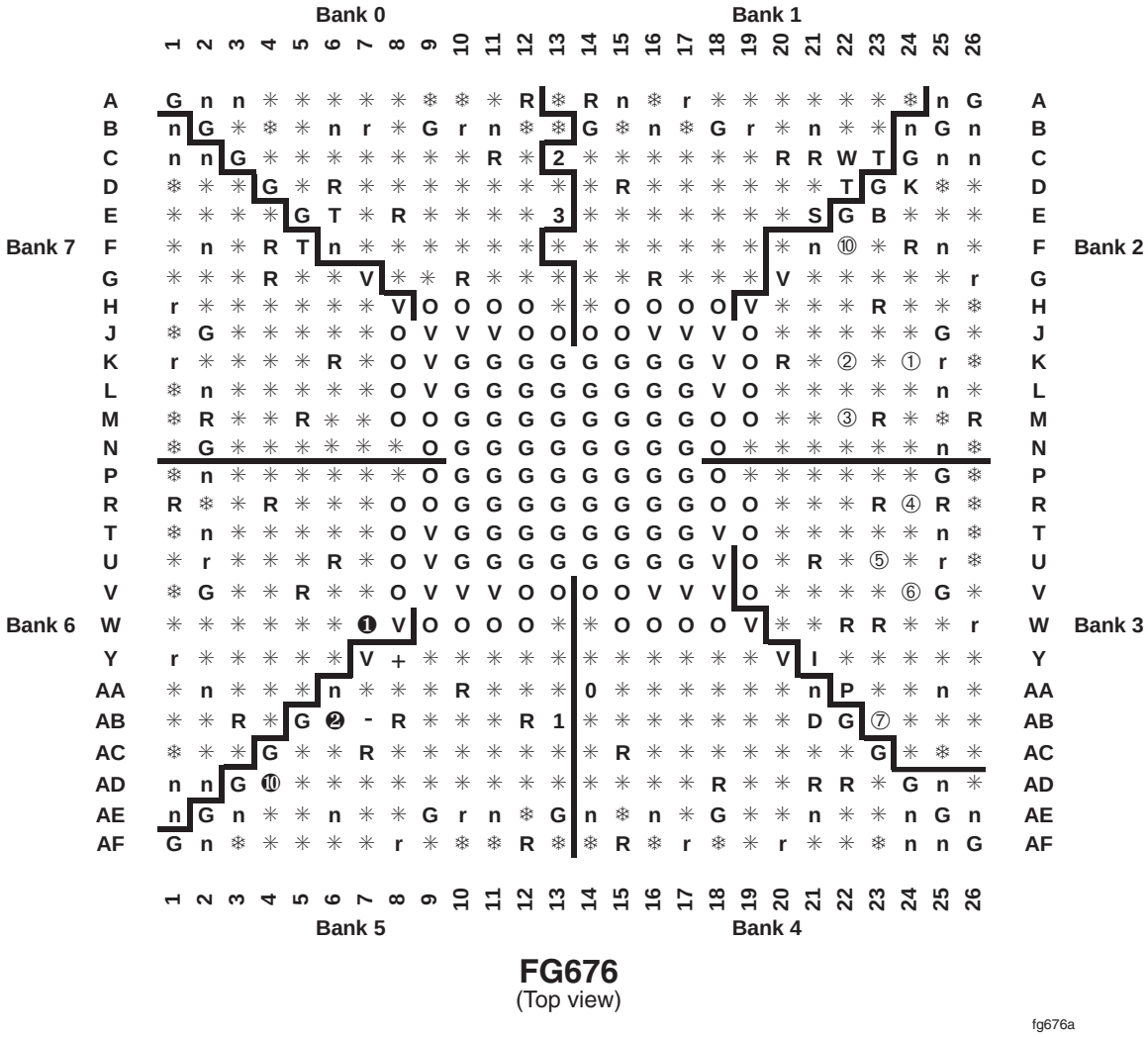

Figure 10: **FG676 Pin Function Diagram**

Notes:

Packages FG456 and FG676 are layout compatible.