AMD Xilinx - XCV150-4BG352C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	864
Number of Logic Elements/Cells	3888
Total RAM Bits	49152
Number of I/O	260
Number of Gates	164674
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	352-LBGA Exposed Pad, Metal
Supplier Device Package	352-MBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv150-4bg352c

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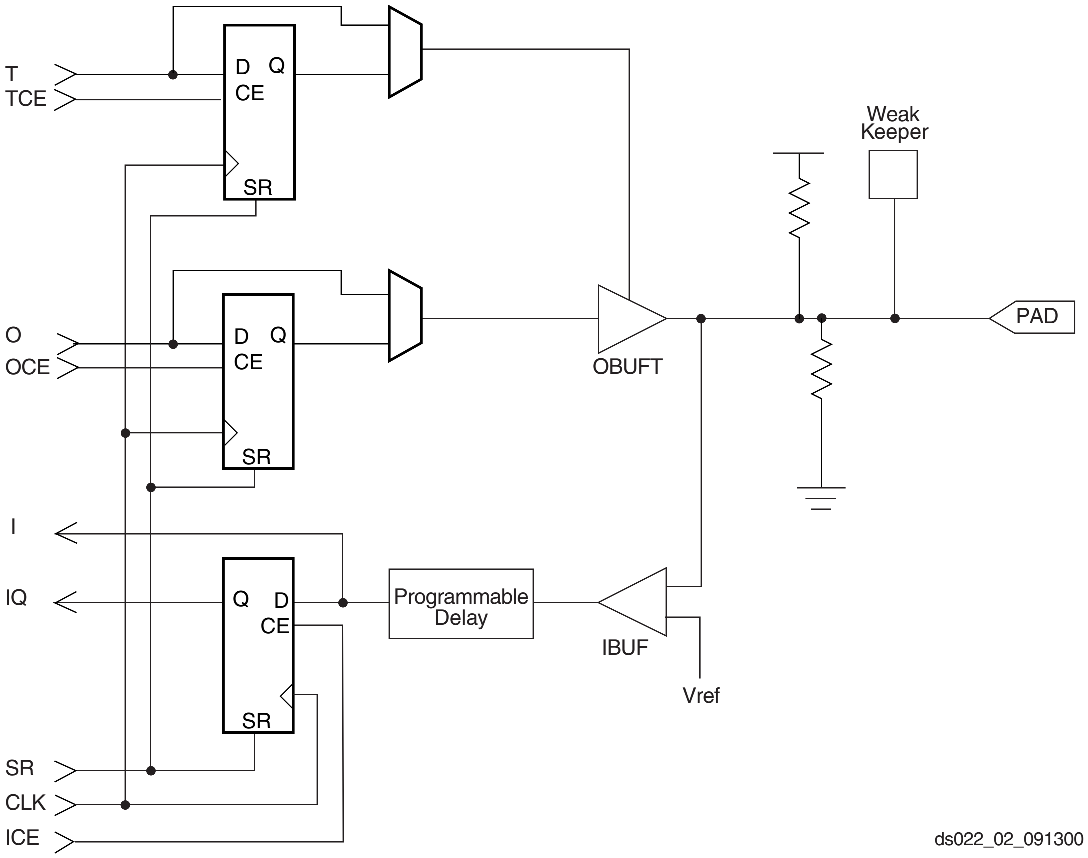


Figure 2: **Virtex Input/Output Block (IOB)**

Table 1: **Supported Select I/O Standards**

I/O Standard	Input Reference Voltage (V_{REF})	Output Source Voltage (V_{CCO})	Board Termination Voltage (V_{TT})	5 V Tolerant
LVTTL 2 – 24 mA	N/A	3.3	N/A	Yes
LVCMOS2	N/A	2.5	N/A	Yes
PCI, 5 V	N/A	3.3	N/A	Yes
PCI, 3.3 V	N/A	3.3	N/A	No
GTL	0.8	N/A	1.2	No
GTL+	1.0	N/A	1.5	No
HSTL Class I	0.75	1.5	0.75	No
HSTL Class III	0.9	1.5	1.5	No
HSTL Class IV	0.9	1.5	1.5	No
SSTL3 Class I &II	1.5	3.3	1.5	No
SSTL2 Class I & II	1.25	2.5	1.25	No
CTT	1.5	3.3	1.5	No
AGP	1.32	3.3	N/A	No

Input Path

A buffer In the Virtex IOB input path routes the input signal either directly to internal logic or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signalling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can used in close proximity to each other. See **I/O Banking**, page 3.

There are optional pull-up and pull-down resistors at each user I/O input for use after configuration. Their value is in the range 50 kΩ – 100 kΩ.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signalling standards. Each output buffer can source up to 24 mA and sink up to 48mA. Drive strength and slew rate controls minimize bus transients.

In most signalling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See **I/O Banking**, page 3.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signalling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages externally and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks, as shown in Figure 3. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

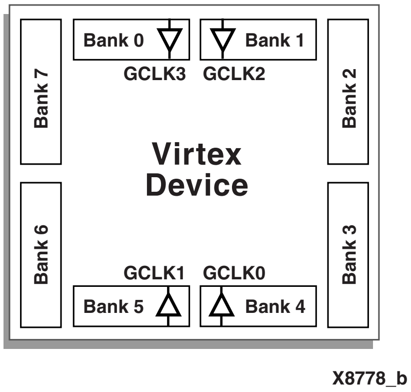


Figure 3: **Virtex I/O Banks**

Within a bank, output standards can be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 2. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}.

Table 2: **Compatible Output Standards**

V_{CCO}	Compatible Standards
3.3 V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+
2.5 V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+
1.5 V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, V_{REF}. In this case, certain user-I/O pins are automatically configured as inputs for the V_{REF} voltage. Approximately one in six of the I/O pins in the bank assume this role.

The V_{REF} pins within a bank are interconnected internally and consequently only one V_{REF} voltage can be used within each bank. All V_{REF} pins in the bank, however, must be connected to the external voltage source for correct operation.

Within a bank, inputs that require V_{REF} can be mixed with those that do not. However, only one V_{REF} voltage can be used within a bank. Input buffers that use V_{REF} are not 5 V tolerant. LVTTL, LVCMOS2, and PCI 33 MHz 5 V, are 5 V tolerant.

The V_{CCO} and V_{REF} pins for each bank appear in the device Pinout tables and diagrams. The diagrams also show the bank affiliation of each I/O.

Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary. All the V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage, and not used for I/O.

In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or can be connected to the V_{CCO} voltage to permit migration to a larger device if necessary.

In TQ144 and PQ/HQ240 packages, all V_{CCO} pins are bonded together internally, and consequently the same V_{CCO} voltage must be connected to all of them. In the CS144 package, bank pairs that share a side are interconnected internally, permitting four choices for V_{CCO}. In both cases, the V_{REF} pins remain internally connected as eight banks, and can be used as described previously.

Configurable Logic Block

The basic building block of the Virtex CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and a storage element. The output from the function generator in each LC drives both the CLB output and the D input of the flip-flop. Each Virtex CLB contains four LCs, organized in two similar slices, as shown in Figure 4.

Figure 5 shows a more detailed view of a single slice.

In addition to the four basic LCs, the Virtex CLB contains logic that combines function generators to provide functions of five or six inputs. Consequently, when estimating the number of system gates provided by a given device, each CLB counts as 4.5 LCs.

Look-Up Tables

Virtex function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16x1-bit dual-port synchronous RAM.

The Virtex LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

Storage Elements

The storage elements in the Virtex slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by the function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each Slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals can be configured to operate asynchronously. All of the control signals are independently invertible, and are shared by the two flip-flops within the slice.

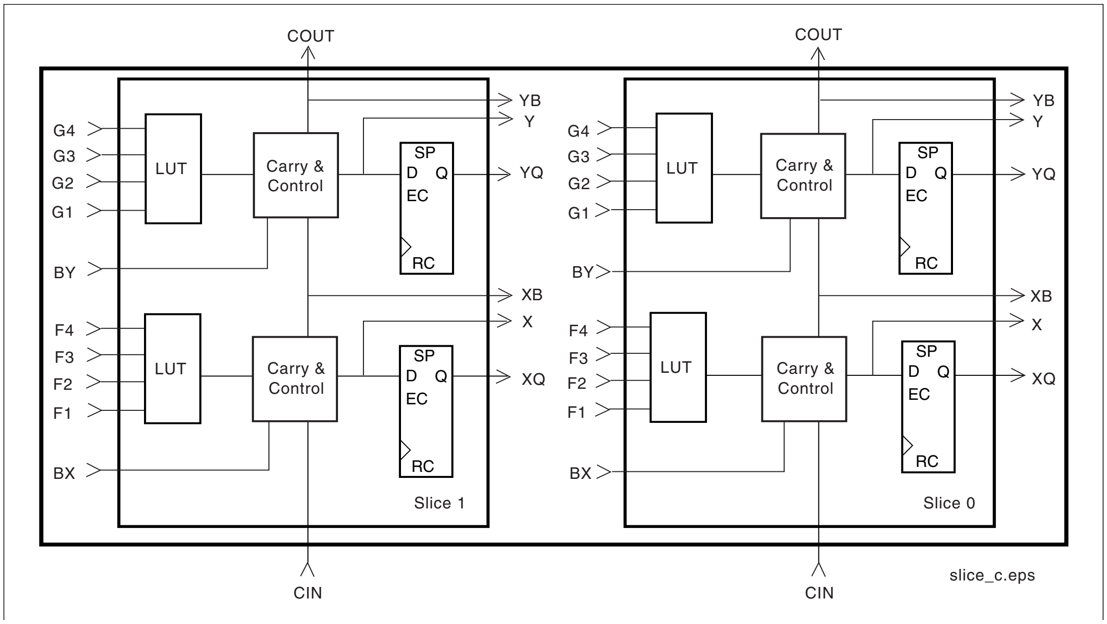


Figure 4: **2-Slice Virtex CLB**

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

Figure 10 is a diagram of the Virtex Series boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Instruction Set

The Virtex Series boundary scan instruction set also includes instructions to configure the device and read back configuration data (CFG_IN, CFG_OUT, and JSTART). The complete instruction set is coded as shown in Table 5.

Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out, and 3-State Control. Non-IOB pins have appropriate partial bit population if input-only or output-only. Each EXTEST CAPTURED-OR state captures all In, Out, and 3-state pins.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA supports up to two additional internal scan chains that can be specified using the BSCAN macro. The macro provides two user pins (SEL1 and SEL2) which are decodes of the USER1 and USER2 instructions respectively. For these instructions, two corresponding pins (TDO1 and TDO2) allow user scan data to be shifted out of TDO.

Likewise, there are individual clock pins (DRCK1 and DRCK2) for each user register. There is a common input pin (TDI) and shared output pins that represent the state of the TAP controller (RESET, SHIFT, and UPDATE).

Bit Sequence

The order within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

From a cavity-up view of the chip (as shown in EPIC), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 11.

BSDL (Boundary Scan Description Language) files for Virtex Series devices are available on the Xilinx web site in the File Download area.

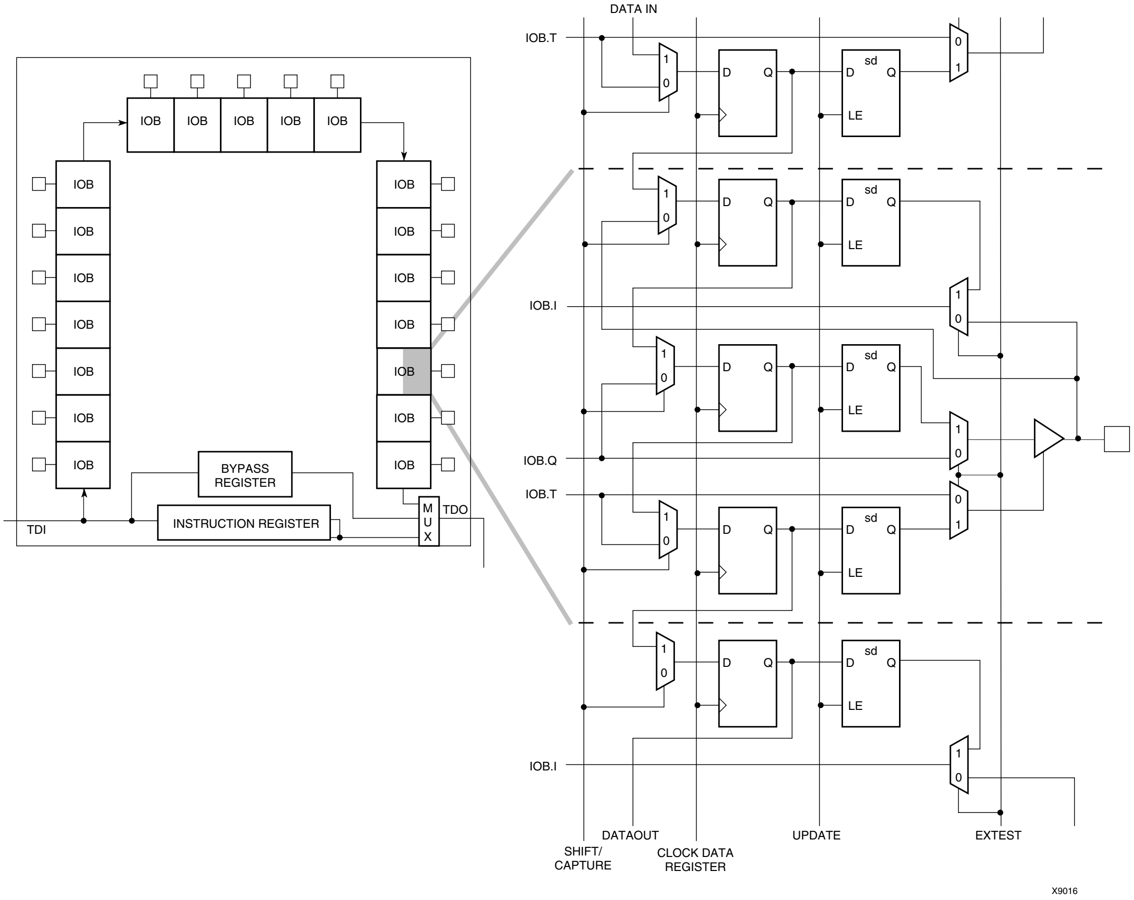
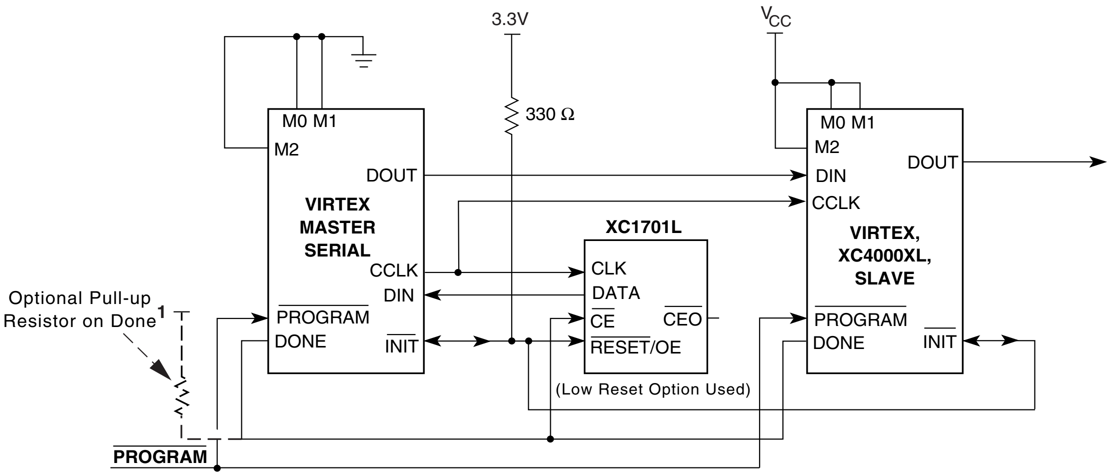


Figure 10: **Virtex Series Boundary Scan Logic**

Table 8: **Master/Slave Serial Mode Programming Switching**

	Description	Figure References	Symbol	Values	Units
CCLK	DIN setup/hold, slave mode	1/2	T_{DCC}/T_{CCD}	5.0 / 0	ns, min
	DIN setup/hold, master mode	1/2	T_{DSCK}/T_{CKDS}	5.0 / 0	ns, min
	DOUT	3	T_{CCO}	12.0	ns, max
	High time	4	T_{CCH}	5.0	ns, min
	Low time	5	T_{CCL}	5.0	ns, min
	Maximum Frequency		F_{CC}	66	MHz, max
	Frequency Tolerance, master mode with respect to nominal			+45% –30%	



Note 1: If none of the Virtex FPGAs have been selected to drive DONE, an external pull-up resistor of 330 Ω should be added to the common DONE line. (For Spartan-XL devices, add a 4.7K Ω pull-up resistor.) This pull-up is not needed if the DriveDONE attribute is set. If used, DriveDONE should be selected only for the last device in the configuration chain.

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Figure 12: **Master/Slave Serial Mode Circuit Diagram**

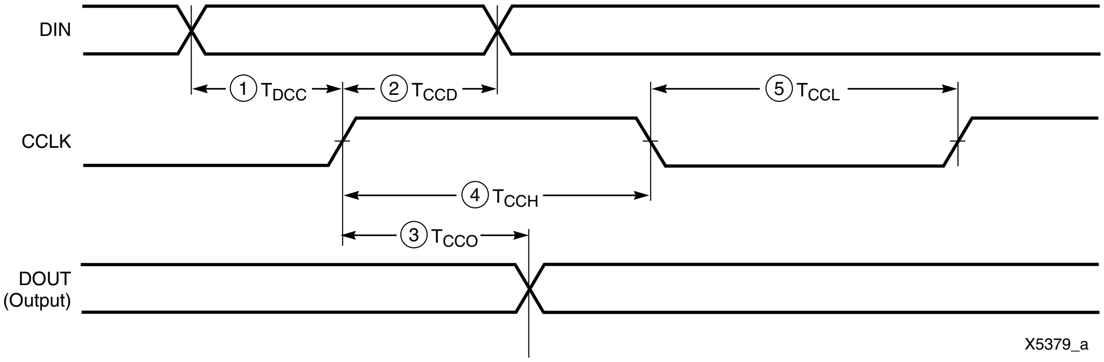

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Figure 13: **Slave-Serial Mode Programming Switching Characteristics**

3. At the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this has happened.
4. Repeat steps 2 and 3 until all the data has been sent.
5. De-assert $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$.

A flowchart for the write operation appears in Figure 17. Note that if CCLK is slower than f_{CCNH}, the FPGA never asserts BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

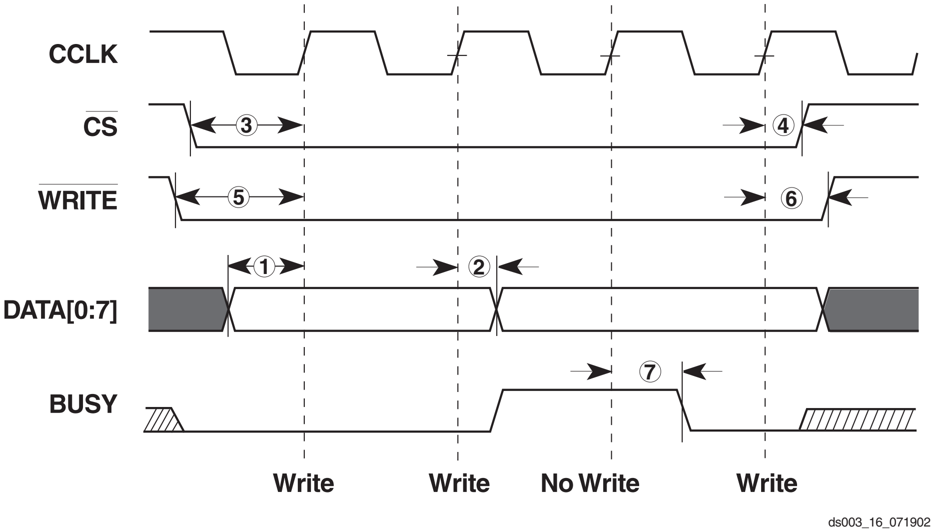


Figure 16: **Write Operations**

DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Device	Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage (below which configuration data can be lost)		All	2.0		V
V_{DRIO}	Data Retention V_{CCO} Voltage (below which configuration data can be lost)		All	1.2		V
I_{CCINTQ}	Quiescent V_{CCINT} supply current$^{(1,3)}$		XCV50		50	mA
			XCV100		50	mA
			XCV150		50	mA
			XCV200		75	mA
			XCV300		75	mA
			XCV400		75	mA
			XCV600		100	mA
			XCV800		100	mA
			XCV1000		100	mA
I_{CCOQ}	Quiescent V_{CCO} supply current$^{(1)}$		XCV50		2	mA
			XCV100		2	mA
			XCV150		2	mA
			XCV200		2	mA
			XCV300		2	mA
			XCV400		2	mA
			XCV600		2	mA
			XCV800		2	mA
			XCV1000		2	mA
I_{REF}	V_{REF} current per V_{REF} pin		All		20	µA
I_L	Input or output leakage current		All	–10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, PQ, HQ, packages	All		8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V, V_{CCO} = 3.3 V (sample tested)		All	Note (2)	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)			Note (2)	0.15	mA

Notes:

1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.
3. Multiply I_{CCINTQ} limit by two for industrial grade.

Virtex Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Virtex devices unless otherwise noted.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in , page 6.

Description	Device	Symbol	Speed Grade				Units
			Min	-6	-5	-4	
Propagation Delays							
Pad to I output, no delay	All	T_{IOPI}	0.39	0.8	0.9	1.0	ns, max
Pad to I output, with delay	XCV50	T_{IOPID}	0.8	1.5	1.7	1.9	ns, max
	XCV100		0.8	1.5	1.7	1.9	ns, max
	XCV150		0.8	1.5	1.7	1.9	ns, max
	XCV200		0.8	1.5	1.7	1.9	ns, max
	XCV300		0.8	1.5	1.7	1.9	ns, max
	XCV400		0.9	1.8	2.0	2.3	ns, max
	XCV600		0.9	1.8	2.0	2.3	ns, max
	XCV800		1.1	2.1	2.4	2.7	ns, max
	XCV1000		1.1	2.1	2.4	2.7	ns, max
Pad to output IQ via transparent latch, no delay	All	T_{IOPLI}	0.8	1.6	1.8	2.0	ns, max
Pad to output IQ via transparent latch, with delay	XCV50	T_{IOPLID}	1.9	3.7	4.2	4.8	ns, max
	XCV100		1.9	3.7	4.2	4.8	ns, max
	XCV150		2.0	3.9	4.3	4.9	ns, max
	XCV200		2.0	4.0	4.4	5.1	ns, max
	XCV300		2.0	4.0	4.4	5.1	ns, max
	XCV400		2.1	4.1	4.6	5.3	ns, max
	XCV600		2.1	4.2	4.7	5.4	ns, max
	XCV800		2.2	4.4	4.9	5.6	ns, max
	XCV1000		2.3	4.5	5.1	5.8	ns, max
Sequential Delays							
Clock CLK	All						
Minimum Pulse Width, High		T_{CH}	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low		T_{CL}	0.8	1.5	1.7	2.0	ns, min
Clock CLK to output IQ		T_{IOCKIQ}	0.2	0.7	0.7	0.8	ns, max

Calculation of T_{ioop} as a Function of Capacitance

T_{ioop} is the propagation delay from the O Input of the IOB to the pad. The values for T_{ioop} were based on the standard capacitive load (Csl) for each I/O standard as listed in Table 2.

Table 2: **Constants for Calculating T_{ioop}**

Standard	Csl (pF)	fl (ns/pF)
LVTTL Fast Slew Rate, 2mA drive	35	0.41
LVTTL Fast Slew Rate, 4mA drive	35	0.20
LVTTL Fast Slew Rate, 6mA drive	35	0.13
LVTTL Fast Slew Rate, 8mA drive	35	0.079
LVTTL Fast Slew Rate, 12mA drive	35	0.044
LVTTL Fast Slew Rate, 16mA drive	35	0.043
LVTTL Fast Slew Rate, 24mA drive	35	0.033
LVTTL Slow Slew Rate, 2mA drive	35	0.41
LVTTL Slow Slew Rate, 4mA drive	35	0.20
LVTTL Slow Slew Rate, 6mA drive	35	0.100
LVTTL Slow Slew Rate, 8mA drive	35	0.086
LVTTL Slow Slew Rate, 12mA drive	35	0.058
LVTTL Slow Slew Rate, 16mA drive	35	0.050
LVTTL Slow Slew Rate, 24mA drive	35	0.048
LVCMOS2	35	0.041
PCI 33MHz 5V	50	0.050
PCI 33MHZ 3.3 V	10	0.050
PCI 66 MHz 3.3 V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

Notes:

1. I/O parameter measurements are made with the capacitance values shown above. See Application Note XAPP133 on www.xilinx.com for appropriate terminations.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

For other capacitive loads, use the formulas below to calculate the corresponding T_{ioop}.

$$T_{ioop} = T_{ioop} + T_{opadjust} + (C_{load} - C_{sl}) * fl$$

Where:

$T_{opadjust}$ is reported above in the Output Delay Adjustment section.

C_{load} is the capacitive load for the design.

Table 3: **Delay Measurement Methodology**

Standard	V_L(1)	V_H(1)	Meas. Point	V_{REF} Typ(2)
LVTTL	0	3	1.4	-
LVCMOS2	0	2.5	1.125	-
PCI33_5	Per PCI Spec			-
PCI33_3	Per PCI Spec			-
PCI66_3	Per PCI Spec			-
GTL	$V_{REF} -0.2$	$V_{REF} +0.2$	V_{REF}	0.80
GTL+	$V_{REF} -0.2$	$V_{REF} +0.2$	V_{REF}	1.0
HSTL Class I	$V_{REF} -0.5$	$V_{REF} +0.5$	V_{REF}	0.75
HSTL Class III	$V_{REF} -0.5$	$V_{REF} +0.5$	V_{REF}	0.90
HSTL Class IV	$V_{REF} -0.5$	$V_{REF} +0.5$	V_{REF}	0.90
SSTL3 I & II	$V_{REF} -1.0$	$V_{REF} +1.0$	V_{REF}	1.5
SSTL2 I & II	$V_{REF} -0.75$	$V_{REF} +0.75$	V_{REF}	1.25
CTT	$V_{REF} -0.2$	$V_{REF} +0.2$	V_{REF}	1.5
AGP	$V_{REF} - (0.2 x V_{CCO})$	$V_{REF} + (0.2 x V_{CCO})$	V_{REF}	Per AGP Spec

Notes:

1. Input waveform switches between V_L and V_H.
2. Measurements are made at VREF (Typ), Maximum, and Minimum. Worst-case values are reported.
3. I/O parameter measurements are made with the capacitance values shown in Table 2. See Application Note XAPP133 on www.xilinx.com for appropriate terminations.
4. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

CLB SelectRAM Switching Characteristics

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Sequential Delays						
Clock CLK to X/Y outputs (WE active) 16 x 1 mode	$T_{SHCKO16}$	1.2	2.3	2.6	3.0	ns, max
Clock CLK to X/Y outputs (WE active) 32 x 1 mode	$T_{SHCKO32}$	1.2	2.7	3.1	3.5	ns, max
Shift-Register Mode						
Clock CLK to X/Y outputs	T_{REG}	1.2	3.7	4.1	4.7	ns, max
Setup and Hold Times before/after Clock CLK(1)	Setup Time / Hold Time					
F/G address inputs	T_{AS}/T_{AH}	0.25 / 0	0.5 / 0	0.6 / 0	0.7 / 0	ns, min
BX/BY data inputs (DIN)	T_{DS}/T_{DH}	0.34 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
CE input (WE)	T_{WS}/T_{WH}	0.38 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
Shift-Register Mode						
BX/BY data inputs (DIN)	T_{SHDICK}	0.34	0.7	0.8	0.9	ns, min
CE input (WS)	T_{SHCECK}	0.38	0.8	0.9	1.0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{WPH}	1.2	2.4	2.7	3.1	ns, min
Minimum Pulse Width, Low	T_{WPL}	1.2	2.4	2.7	3.1	ns, min
Minimum clock period to meet address write cycle time	T_{WC}	2.4	4.8	5.4	6.2	ns, min
Shift-Register Mode						
Minimum Pulse Width, High	T_{SRPH}	1.2	2.4	2.7	3.1	ns, min
Minimum Pulse Width, Low	T_{SRPL}	1.2	2.4	2.7	3.1	ns, min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Virtex Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL

Description	Symbol	Device	Speed Grade				Units
			Min	**-6**	**-5**	**-4**	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DLL. For data *output* with different standards, adjust delays with the values shown in Output Delay Adjustments.	$T_{ICKOFDLL}$	XCV50	1.0	3.1	3.3	3.6	ns, max
		XCV100	1.0	3.1	3.3	3.6	ns, max
		XCV150	1.0	3.1	3.3	3.6	ns, max
		XCV200	1.0	3.1	3.3	3.6	ns, max
		XCV300	1.0	3.1	3.3	3.6	ns, max
		XCV400	1.0	3.1	3.3	3.6	ns, max
		XCV600	1.0	3.1	3.3	3.6	ns, max
		XCV800	1.0	3.1	3.3	3.6	ns, max
		XCV1000	1.0	3.1	3.3	3.6	ns, max

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see Table 2 and Table 3.
3. DLL output jitter is already included in the timing calculation.

Global Clock Input-to-Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL

Description	Symbol	Device	Speed Grade				Units
			Min	**-6**	**-5**	**-4**	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DLL. For data *output* with different standards, adjust delays with the values shown in Input and Output Delay Adjustments. For I/O standards requiring V_{REF}, such as GTL, GTL+, SSTL, HSTL, CTT, and AGO, an additional 600 ps must be added.	T_{ICKOF}	XCV50	1.5	4.6	5.1	5.7	ns, max
		XCV100	1.5	4.6	5.1	5.7	ns, max
		XCV150	1.5	4.7	5.2	5.8	ns, max
		XCV200	1.5	4.7	5.2	5.8	ns, max
		XCV300	1.5	4.7	5.2	5.9	ns, max
		XCV400	1.5	4.8	5.3	6.0	ns, max
		XCV600	1.6	4.9	5.4	6.0	ns, max
		XCV800	1.6	4.9	5.5	6.2	ns, max
		XCV1000	1.7	5.0	5.6	6.3	ns, max

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see Table 2 and Table 3.

Virtex Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Set-Up and Hold for LVTTL Standard, *with* DLL

Description	Symbol	Device	Speed Grade				Units
			Min	-6	-5	-4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in Input Delay Adjustments.							
No Delay Global Clock and IFF, with DLL	T_{PSDLL}/T_{PHDLL}	XCV50	0.40 / –0.4	1.7 /–0.4	1.8 /–0.4	2.1 /–0.4	ns, min
		XCV100	0.40 /–0.4	1.7 /–0.4	1.9 /–0.4	2.1 /–0.4	ns, min
		XCV150	0.40 /–0.4	1.7 /–0.4	1.9 /–0.4	2.1 /–0.4	ns, min
		XCV200	0.40 /–0.4	1.7 /–0.4	1.9 /–0.4	2.1 /–0.4	ns, min
		XCV300	0.40 /–0.4	1.7 /–0.4	1.9 /–0.4	2.1 /–0.4	ns, min
		XCV400	0.40 /–0.4	1.7 /–0.4	1.9 /–0.4	2.1 /–0.4	ns, min
		XCV600	0.40 /–0.4	1.7 /–0.4	1.9 /–0.4	2.1 /–0.4	ns, min
		XCV800	0.40 /–0.4	1.7 /–0.4	1.9 /–0.4	2.1 /–0.4	ns, min
		XCV1000	0.40 /–0.4	1.7 /–0.4	1.9 /–0.4	2.1 /–0.4	ns, min

IFF = Input Flip-Flop or Latch

Notes:

1. Set-up time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
2. DLL output jitter is already included in the timing calculation.
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Description	Symbol	Speed Grade						Units
		-6		-5		-4		
		Min	Max	Min	Max	Min	Max	
Input Clock Frequency (CLKDLLHF)	FCLKINHF	60	200	60	180	60	180	MHz
Input Clock Frequency (CLKDLL)	FCLKINLF	25	100	25	90	25	90	MHz
Input Clock Pulse Width (CLKDLLHF)	$T_{DLLPWHF}$	2.0	-	2.4	-	2.4	-	ns
Input Clock Pulse Width (CLKDLL)	$T_{DLLPWLF}$	2.5	-	3.0		3.0	-	ns

Notes:

1. All specifications correspond to Commercial Operating Temperatures (0°C to + 85°C).

DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

Description	Symbol	F_{CLKIN}	CLKDLLHF		CLKDLL		Units
			Min	Max	Min	Max	
Input Clock Period Tolerance	T_{IPTOL}		-	1.0	-	1.0	ns
Input Clock Jitter Tolerance (Cycle to Cycle)	T_{IJITCC}		-	± 150	-	± 300	ps
Time Required for DLL to Acquire Lock	T_{LOCK}	> 60 MHz	-	20	-	20	µs
		50 - 60 MHz	-	-	-	25	µs
		40 - 50 MHz	-	-	-	50	µs
		30 - 40 MHz	-	-	-	90	µs
		25 - 30 MHz	-	-	-	120	µs
Output Jitter (cycle-to-cycle) for any DLL Clock Output(1)	T_{OJITCC}			± 60		± 60	ps
Phase Offset between CLKIN and CLKO(2)	T_{PHIO}			± 100		± 100	ps
Phase Offset between Clock Outputs on the DLL(3)	T_{PHOO}			± 140		± 140	ps
Maximum Phase Difference between CLKIN and CLKO(4)	T_{PHIOM}			± 160		± 160	ps
Maximum Phase Difference between Clock Outputs on the DLL(5)	T_{PHOOM}			± 200		± 200	ps

Notes:

1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* Output Jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN an CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase DIfference between Clock Outputs on the DLL** is the sum of Output JItter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges sue to DLL alone (*excluding* input clock jitter).
6. All specifications correspond to Commercial Operating Temperatures (0°C to +85°C).

Date	Version	Revision
01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
03/00	2.0	New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration.
05/00	2.1	Modified "Pins not listed..." statement. Speed grade update to Final status.
05/00	2.2	Modified Table 18.
09/00	2.3	• Added XCV400 values to table under **Minimum Clock-to-Out for Virtex Devices**. • Corrected Units column in table under **IOB Input Switching Characteristics**. • Added values to table under **CLB SelectRAM Switching Characteristics**.
10/00	2.4	• Corrected Pinout information for devices in the BG256, BG432, and BG560 packages in Table 18. • Corrected **BG256 Pin Function Diagram**.
04/02/01	2.5	• Revised minimums for **Global Clock Set-Up and Hold for LVTTL Standard, with DLL**. • Converted file to modularized format. See the **Virtex Data Sheet** section.
04/19/01	2.6	• Clarified TIOCKP and TIOCKON **IOB Output Switching Characteristics** descriptors.
07/19/01	2.7	• Under **Absolute Maximum Ratings**, changed (T_{SOL}) to 220 °C.
07/26/01	2.8	• Removed T_{SOL} parameter and added footnote to **Absolute Maximum Ratings** table.
10/29/01	2.9	• Updated the speed grade designations used in data sheets, and added Table 1, which shows the current speed grade designation for each device.
02/01/02	3.0	• Added footnote to **DC Input and Output Levels** table.
07/19/02	3.1	• Removed mention of MIL-M-38510/605 specification. • Added link to xapp158 from the **Power-On Power Supply Requirements** section.
09/10/02	3.2	• Added Clock CLK to **IOB Input Switching Characteristics** and **IOB Output Switching Characteristics**.
03/01/13	4.0	The products listed in this data sheet are obsolete. See **XCN10016** for further information.

Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

- DS003-1, Virtex 2.5V FPGAs:
  Introduction and Ordering Information (Module 1)
- DS003-2, Virtex 2.5V FPGAs:
  Functional Description (Module 2)
- DS003-3, Virtex 2.5V FPGAs:
  DC and Switching Characteristics (Module 3)
- DS003-4, Virtex 2.5V FPGAs:
  Pinout Tables (Module 4)

Table 3: **Virtex Pinout Tables (BGA)** ***(Continued)***

Pin Name	Device	BG256	BG352	BG432	BG560
V_{REF}, Bank 3 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	M18, V20	N/A	N/A	N/A
	XCV100/150	... + R19	R4, V4, Y3	N/A	N/A
	XCV200/300	... + P18	... + AC2	V2, AB4, AD4, AF3	N/A
	XCV400	N/A	N/A	... + U2	V4, W5, AD3, AE5, AK2
	XCV600	N/A	N/A	... + AC3	... + AF1
	XCV800	N/A	N/A	... + Y3	... + AA4
	XCV1000	N/A	N/A	N/A	... + AH4
V_{REF}, Bank 4 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	V12, Y18	N/A	N/A	N/A
	XCV100/150	... + W15	AC12, AE5, AE8,	N/A	N/A
	XCV200/300	... + V14	... + AE4	AJ7, AL4, AL8, AL13	N/A
	XCV400	N/A	N/A	... + AK15	AL7, AL10, AL16, AM4, AM14
	XCV600	N/A	N/A	... + AK8	... + AL9
	XCV800	N/A	N/A	... + AJ12	... + AK13
	XCV1000	N/A	N/A	N/A	... + AN3
V_{REF}, Bank 5 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	V9, Y3	N/A	N/A	N/A
	XCV100/150	... + W6	AC15, AC18, AD20	N/A	N/A
	XCV200/300	... + V7	... + AE23	AJ18, AJ25, AK23, AK27	N/A
	XCV400	N/A	N/A	... + AJ17	AJ18, AJ25, AL20, AL24, AL29
	XCV600	N/A	N/A	... + AL24	... + AM26
	XCV800	N/A	N/A	... + AH19	... + AN23
	XCV1000	N/A	N/A	N/A	... + AK28
V_{REF}, Bank 6 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	M2, R3	N/A	N/A	N/A
	XCV100/150	... + T1	R24, Y26, AA25,	N/A	N/A
	XCV200/300	... + T3	... + AD26	V28, AB28, AE30, AF28	N/A
	XCV400	N/A	N/A	... + U28	V29, Y32, AD31, AE29, AK32
	XCV600	N/A	N/A	... + AC28	... + AE31
	XCV800	N/A	N/A	... + Y30	... + AA30
	XCV1000	N/A	N/A	N/A	... + AH30

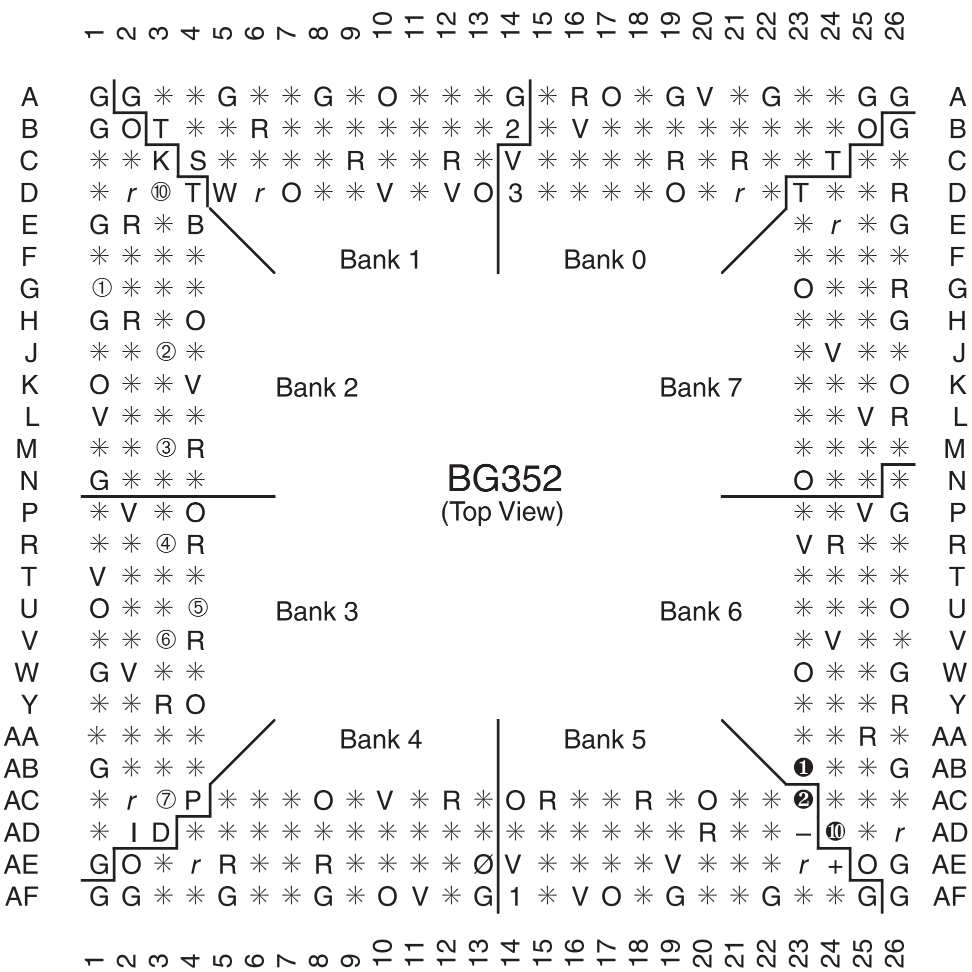
Table 4: **Virtex Pinout Tables (Fine-Pitch BGA) *(Continued)***

Pin Name	Device	FG256	FG456	FG676	FG680
V_{CCINT}	All	C3, C14, D4, D13, E5, E12, M5, M12, N4, N13, P3, P14	E5, E18, F6, F17, G7, G8, G9, G14, G15, G16, H7, H16, J7, J16, P7, P16, R7, R16, T7, T8, T9, T14, T15, T16, U6, U17, V5, V18	G7, G20, H8, H19, J9, J10, J11, J16, J17, J18, K9, K18, L9, L18, T9, T18, U9, U18, V9, V10, V11, V16, V17, V18, W8, W19, Y7, Y20	AD5, AD35, AE5, AE35, AL5, AL35, AM5, AM35, AR8, AR9, AR15, AR16, AR24, AR25, AR31, AR32, E8, E9, E15, E16, E24, E25, E31, E32, H5, H35, J5, J35, R5, R35, T5, T35
V_{CCO}, Bank 0	All	E8, F8	F7, F8, F9, F10 G10, G11	H9, H10, H11, H12, J12, J13	E26, E27, E29, E30, E33, E34
V_{CCO}, Bank 1	All	E9, F9	F13, F14, F15, F16, G12, G13	H15, H16, H17, H18, J14, J15	E6, E7, E10, E11, E13, E14
V_{CCO}, Bank 2	All	H11, H12	G17, H17, J17, K16, K17, L16	J19, K19, L19, M18, M19, N18	F5, G5, K5, L5, N5, P5
V_{CCO}, Bank 3	All	J11, J12	M16, N16, N17, P17, R17, T17	P18, R18, R19, T19, U19, V19	AF5, AG5, AN5, AK5, AJ5, AP5
V_{CCO}, Bank 4	All	L9. M9	T12, T13, U13, U14, U15, U16,	V14, V15, W15, W16, W17, W18	AR6, AR7, AR10, AR11, AR13, AR14
V_{CCO}, Bank 5	All	L8, M8	T10, T11, U7, U8, U9, U10	V12, V13, W9,W10, W11, W12	AR26, AR27, AR29, AR30, AR33, AR34
V_{CCO}, Bank 6	All	J5, J6	M7, N6, N7, P6, R6, T6	P9, R8, R9, T8, U8, V8	AF35, AG35, AJ35, AK35, AN35, AP35
V_{CCO}, Bank 7	All	H5, H6	G6, H6, J6, K6, K7, L7	J8, K8, L8, M8, M9, N9	F35, G35, K35, L35, N35, P35
V_{REF}, Bank 0 (VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	B4, B7	N/A	N/A	N/A
	XCV100/150	... + C6	A9, C6, E8	N/A	N/A
	XCV200/300	... + A3	... + B4	N/A	N/A
	XCV400	N/A	N/A	A12, C11, D6, E8, G10	
	XCV600	N/A	N/A	... + B7	A33, B28, B30, C23, C24, D33
	XCV800	N/A	N/A	... + B10	... + A26
	XCV1000	N/A	N/A	N/A	... + D34

Table 4: **Virtex Pinout Tables (Fine-Pitch BGA)** ***(Continued)***

Pin Name	Device	FG256	FG456	FG676	FG680
V_{REF}, Bank 1 (VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	B9, C11	N/A	N/A	N/A
	XCV100/150	... + E11	A18, B13, E14	N/A	N/A
	XCV200/300	... + A14	... + A19	N/A	N/A
	XCV400	N/A	N/A	A14, C20, C21, D15, G16	N/A
	XCV600	N/A	N/A	... + B19	B6, B8, B18, D11, D13, D17
	XCV800	N/A	N/A	... + A17	... + B14
	XCV1000	N/A	N/A	N/A	... + B5
V_{REF}, Bank 2 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	F13, H13	N/A	N/A	N/A
	XCV100/150	... + F14	F21, H18, K21	N/A	N/A
	XCV200/300	... + E13	... + D22	N/A	N/A
	XCV400	N/A	N/A	F24, H23, K20, M23, M26	N/A
	XCV600	N/A	N/A	... + G26	G1, H4, J1, L2, V5, W3
	XCV800	N/A	N/A	... + K25	... + N1
	XCV1000	N/A	N/A	N/A	... + D2
V_{REF}, Bank 3 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	K16, L14	N/A	N/A	N/A
	XCV100/150	... + L13	N21, R19, U21	N/A	N/A
	XCV200/300	... + M13	... + U20	N/A	N/A
	XCV400	N/A	N/A	R23, R25, U21, W22, W23	N/A
	XCV600	N/A	N/A	... + W26	AC1, AJ2, AK3, AL4, AR1, Y1
	XCV800	N/A	N/A	... + U25	... + AF3
	XCV1000	N/A	N/A	N/A	... + AP4

BG352 Pin Function Diagram

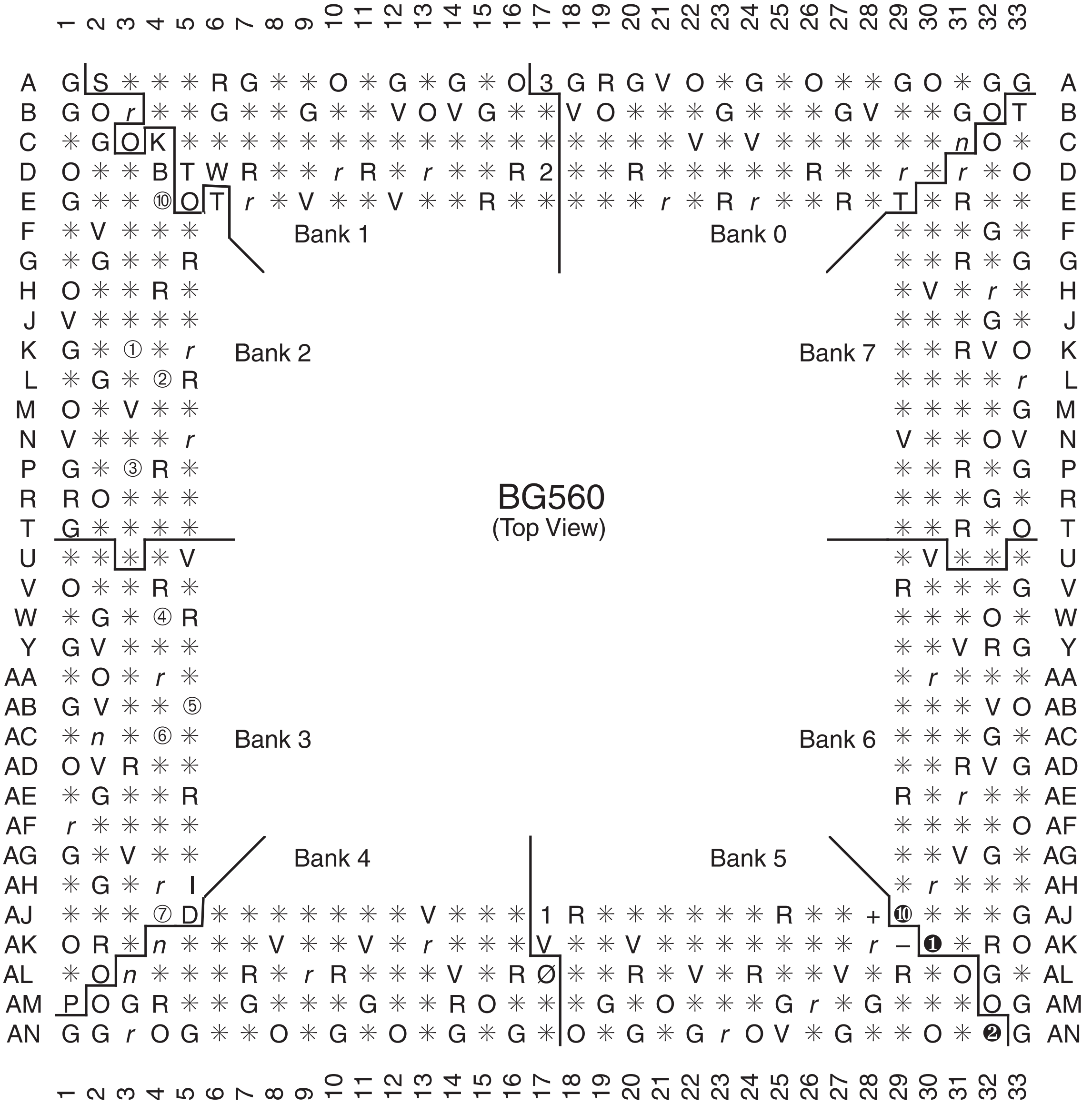


	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	G	G	✳	✳	G	✳	✳	G	✳	O	✳	✳	✳	G	✳	R	O	✳	G	V	✳	G	✳	✳	G	G	A
B	G	O	T	✳	✳	R	✳	✳	✳	✳	✳	✳	✳	2	✳	V	✳	✳	✳	✳	✳	✳	✳	✳	O	G	B
C	✳	✳	K	S	✳	✳	✳	✳	R	✳	✳	R	✳	V	✳	✳	✳	✳	R	✳	R	✳	✳	T	✳	✳	C
D	✳	*r*	⑩	T	W	*r*	O	✳	✳	V	✳	V	O	3	✳	✳	✳	✳	O	✳	*r*	✳	T	✳	✳	R	D
E	G	R	✳	B																			✳	*r*	✳	G	E
F	✳	✳	✳	✳																			✳	✳	✳	✳	F
G	①	✳	✳	✳																			O	✳	✳	R	G
H	G	R	✳	O																			✳	✳	✳	G	H
J	✳	✳	②	✳																			✳	V	✳	✳	J
K	O	✳	✳	V																			✳	✳	✳	O	K
L	V	✳	✳	✳																			✳	✳	V	R	L
M	✳	✳	③	R																			✳	✳	✳	✳	M
N	G	✳	✳	✳																			O	✳	✳	✳	N
P	✳	V	✳	O																			✳	✳	V	G	P
R	✳	✳	④	R																			V	R	✳	✳	R
T	V	✳	✳	✳																			✳	✳	✳	✳	T
U	O	✳	✳	⑤																			✳	✳	✳	O	U
V	✳	✳	⑥	R																			✳	V	✳	✳	V
W	G	V	✳	✳																			O	✳	✳	G	W
Y	✳	✳	R	O																			✳	✳	✳	R	Y
AA	✳	✳	✳	✳																			✳	✳	R	✳	AA
AB	G	✳	✳	✳																			❶	✳	✳	G	AB
AC	✳	*r*	⑦	P	✳	✳	✳	O	✳	V	✳	R	✳	O	R	✳	✳	R	✳	O	✳	✳	❷	✳	✳	✳	AC
AD	✳	I	D	✳	✳	✳	✳	✳	✳	✳	✳	✳	✳	✳	✳	✳	✳	✳	✳	R	✳	✳	–	❿	✳	*r*	AD
AE	G	O	✳	*r*	R	✳	✳	R	✳	✳	✳	✳	Ø	V	✳	✳	✳	✳	V	✳	✳	✳	*r*	+	O	G	AE
AF	G	G	✳	✳	G	✳	✳	G	✳	O	V	✳	G	1	✳	V	O	✳	G	✳	✳	G	✳	✳	G	G	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

DS003_19_100600

Figure 5: **BG352 Pin Function Diagram**

BG560 Pin Function Diagram



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	
A	G	S	✳	✳	✳	R	G	✳	✳	O	✳	G	✳	G	✳	O	3	G	R	G	V	O	✳	G	✳	O	✳	✳	G	O	✳	G	G	A
B	G	O	r	✳	✳	G	✳	✳	G	✳	✳	V	O	V	G	✳	✳	V	O	✳	✳	✳	G	✳	✳	✳	G	V	✳	✳	G	O	T	B
C	✳	G	O	K	✳	✳	✳	✳	✳	✳	✳	✳	✳	✳	✳	✳	✳	✳	✳	✳	✳	V	✳	V	✳	✳	✳	✳	✳	✳	n	O	✳	C
D	O	✳	✳	B	T	W	R	✳	✳	r	R	✳	r	✳	✳	R	2	✳	✳	R	✳	✳	✳	✳	✳	R	✳	✳	r	✳	r	✳	O	D
E	G	✳	✳	⑩	O	T	r	✳	V	✳	✳	V	✳	✳	R	✳	✳	✳	✳	✳	r	✳	R	r	✳	✳	R	✳	T	✳	R	✳	✳	E
F	✳	V	✳	✳	✳																								✳	✳	✳	G	✳	F
G	✳	G	✳	✳	R																								✳	✳	R	✳	G	G
H	O	✳	✳	R	✳																								✳	V	✳	r	✳	H
J	V	✳	✳	✳	✳																								✳	✳	✳	G	✳	J
K	G	✳	①	✳	r																								✳	✳	R	V	O	K
L	✳	G	✳	②	R																								✳	✳	✳	✳	r	L
M	O	✳	V	✳	✳																								✳	✳	✳	✳	G	M
N	V	✳	✳	✳	r																								V	✳	✳	O	V	N
P	G	✳	③	R	✳																								✳	✳	R	✳	G	P
R	R	O	✳	✳	✳																								✳	✳	✳	G	✳	R
T	G	✳	✳	✳	✳																								✳	✳	R	✳	O	T
U	✳	✳	✳	✳	V																								✳	V	✳	✳	✳	U
V	O	✳	✳	R	✳																								R	✳	✳	✳	G	V
W	✳	G	✳	④	R																								✳	✳	✳	O	✳	W
Y	G	V	✳	✳	✳																								✳	✳	V	R	G	Y
AA	✳	O	✳	r	✳																								✳	r	✳	✳	✳	AA
AB	G	V	✳	✳	⑤																								✳	✳	✳	V	O	AB
AC	✳	n	✳	⑥	✳																								✳	✳	✳	G	✳	AC
AD	O	V	R	✳	✳																								✳	✳	R	V	G	AD
AE	✳	G	✳	✳	R																								R	✳	r	✳	✳	AE
AF	r	✳	✳	✳	✳																								✳	✳	✳	✳	O	AF
AG	G	✳	V	✳	✳																								✳	✳	V	G	✳	AG
AH	✳	G	✳	r	I																								✳	r	✳	✳	✳	AH
AJ	✳	✳	✳	⑦	D	✳	✳	✳	✳	✳	✳	✳	V	✳	✳	✳	1	R	✳	✳	✳	✳	✳	✳	R	✳	✳	+	❿	✳	✳	✳	G	AJ
AK	O	R	✳	n	✳	✳	✳	V	✳	✳	V	✳	r	✳	✳	✳	V	✳	✳	V	✳	✳	✳	✳	✳	✳	✳	r	–	❶	✳	R	O	AK
AL	✳	O	n	✳	✳	✳	R	✳	r	R	✳	✳	✳	V	✳	R	Ø	✳	✳	R	✳	V	✳	R	✳	✳	V	✳	R	✳	O	G	✳	AL
AM	P	O	G	R	✳	✳	G	✳	✳	✳	G	✳	✳	R	O	✳	✳	✳	G	✳	O	✳	✳	✳	G	r	✳	G	✳	✳	✳	O	G	AM
AN	G	G	r	O	G	✳	✳	O	✳	G	✳	O	✳	G	✳	G	✳	O	✳	G	✳	G	r	O	V	✳	G	✳	✳	O	✳	❷	G	AN
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	

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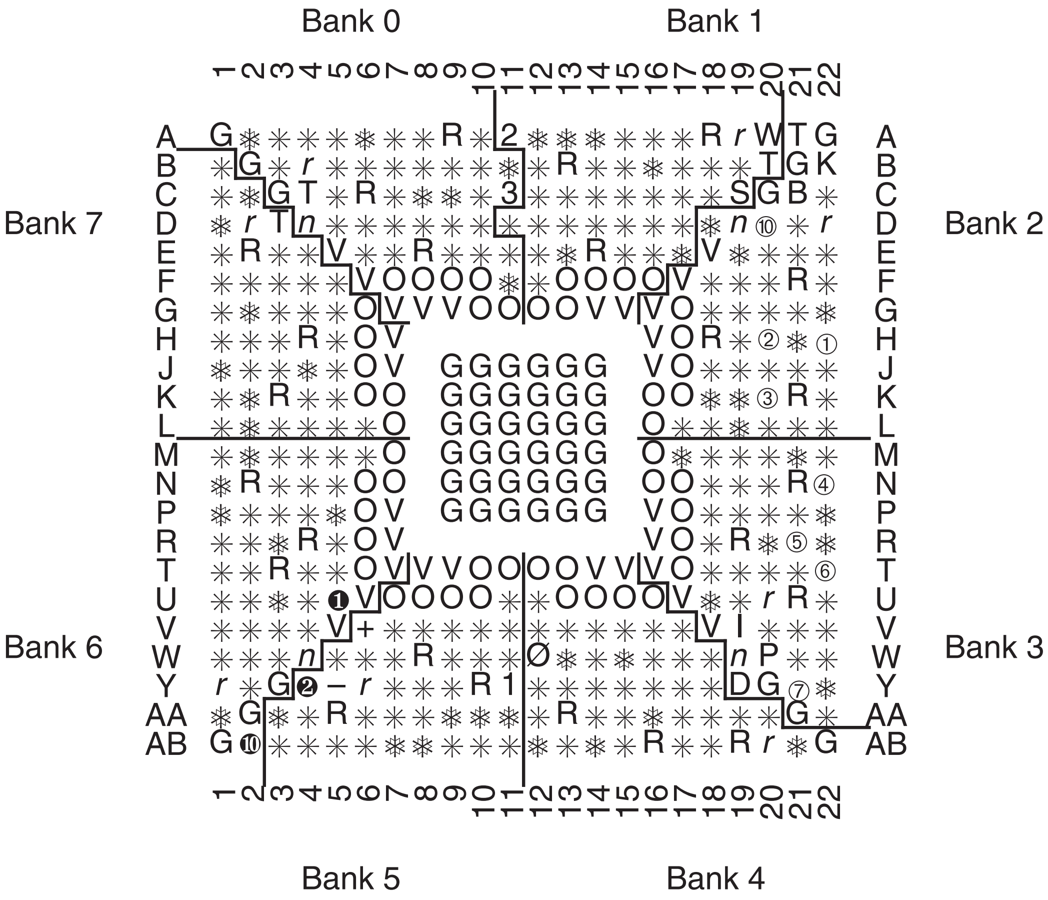
Figure 7: **BG560 Pin Function Diagram**

FG456 Pin Function Diagram



FG456
(Top view)

Figure 9: **FG456 Pin Function Diagram**

Notes:

Packages FG456 and FG676 are layout compatible.