AMD Xilinx - XCV150-4FG256I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	864
Number of Logic Elements/Cells	3888
Total RAM Bits	49152
Number of I/O	176
Number of Gates	164674
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv150-4fg256i

Virtex Architecture

Virtex devices feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing resources. The abundance of routing resources permits the Virtex family to accommodate even the largest and most complex designs.

Virtex FPGAs are SRAM-based, and are customized by loading configuration data into internal memory cells. In some modes, the FPGA reads its own configuration data from an external PROM (master serial mode). Otherwise, the configuration data is written into the FPGA (SelectMAP™, slave serial, and JTAG modes).

The standard Xilinx Foundation™ and Alliance Series™ Development systems deliver complete design support for Virtex, covering every aspect from behavioral and schematic entry, through simulation, automatic design translation and implementation, to the creation, downloading, and readback of a configuration bit stream.

Higher Performance

Virtex devices provide better performance than previous generations of FPGA. Designs can achieve synchronous system clock rates up to 200 MHz including I/O. Virtex inputs and outputs comply fully with PCI specifications, and interfaces can be implemented that operate at 33 MHz or 66 MHz. Additionally, Virtex supports the hot-swapping requirements of Compact PCI.

Xilinx thoroughly benchmarked the Virtex family. While performance is design-dependent, many designs operated internally at speeds in excess of 100 MHz and can achieve 200 MHz. Table 2 shows performance data for representative circuits, using worst-case timing parameters.

Table 2: **Performance for Common Circuit Functions**

Function	Bits	Virtex -6
Register-to-Register		
Adder	16	5.0 ns
	64	7.2 ns
Pipelined Multiplier	8 x 8	5.1 ns
	16 x 16	6.0 ns
Address Decoder	16	4.4 ns
	64	6.4 ns
16:1 Multiplexer		5.4 ns
Parity Tree	9	4.1 ns
	18	5.0 ns
	36	6.9 ns
Chip-to-Chip		
HSTL Class IV		200 MHz
LVTTL,16mA, fast slew		180 MHz

Input Path

A buffer In the Virtex IOB input path routes the input signal either directly to internal logic or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signalling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can used in close proximity to each other. See **I/O Banking**, page 3.

There are optional pull-up and pull-down resistors at each user I/O input for use after configuration. Their value is in the range 50 kΩ – 100 kΩ.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signalling standards. Each output buffer can source up to 24 mA and sink up to 48mA. Drive strength and slew rate controls minimize bus transients.

In most signalling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See **I/O Banking**, page 3.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signalling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages externally and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks, as shown in Figure 3. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

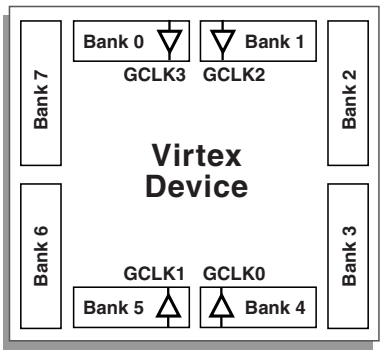


Figure 3: **Virtex I/O Banks**

Within a bank, output standards can be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 2. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}.

Table 2: **Compatible Output Standards**

V_{CCO}	Compatible Standards
3.3 V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+
2.5 V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+
1.5 V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, V_{REF}. In this case, certain user-I/O pins are automatically configured as inputs for the V_{REF} voltage. Approximately one in six of the I/O pins in the bank assume this role.

The V_{REF} pins within a bank are interconnected internally and consequently only one V_{REF} voltage can be used within each bank. All V_{REF} pins in the bank, however, must be connected to the external voltage source for correct operation.

Within a bank, inputs that require V_{REF} can be mixed with those that do not. However, only one V_{REF} voltage can be used within a bank. Input buffers that use V_{REF} are not 5 V tolerant. LVTTL, LVCMOS2, and PCI 33 MHz 5 V, are 5 V tolerant.

The V_{CCO} and V_{REF} pins for each bank appear in the device Pinout tables and diagrams. The diagrams also show the bank affiliation of each I/O.

Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices,

ers with a common user interface regardless of their choice of entry and verification tools. The XDM software simplifies the selection of implementation options with pull-down menus and on-line help.

Application programs ranging from schematic capture to Placement and Routing (PAR) can be accessed through the XDM software. The program command sequence is generated prior to execution, and stored for documentation.

Several advanced software features facilitate Virtex design. RPMs, for example, are schematic-based macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the Xilinx FPGA Foundation development system provides interfaces to the following synthesis design environments.

- Synopsys (FPGA Compiler, FPGA Express)
- Exemplar (Spectrum)
- Synplicity (Synplify)

For schematic design entry, the Xilinx FPGA Foundation and alliance development system provides interfaces to the following schematic-capture design environments.

- Mentor Graphics V8 (Design Architect, QuickSim II)
- Viewlogic Systems (Viewdraw)

Third-party vendors support many other environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Virtex FPGAs supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The “soft macro” portion of the library contains detailed descriptions of common logic functions, but does not contain any partitioning or placement information. The performance of these macros depends, therefore, on the partitioning and placement obtained during implementation.

RPMs, on the other hand, do contain predetermined partitioning and placement information that permits optimal implementation of these functions. Users can create their own library of soft macros or RPMs based on the macros and primitives in the standard library.

The design environment supports hierarchical design entry, with high-level schematics that comprise major functional blocks, while lower-level schematics define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF net list for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floor planning.

The implementation software incorporates Timing Wizard® timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered on a schematic in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the net list for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the TRACE® static timing analyzer.

For in-circuit debugging, the development system includes a download and readback cable. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

3. At the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this has happened.
4. Repeat steps 2 and 3 until all the data has been sent.
5. De-assert $\overline{CS}$ and $\overline{WRITE}$.

A flowchart for the write operation appears in Figure 17. Note that if CCLK is slower than f_{CCNH}, the FPGA never asserts BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

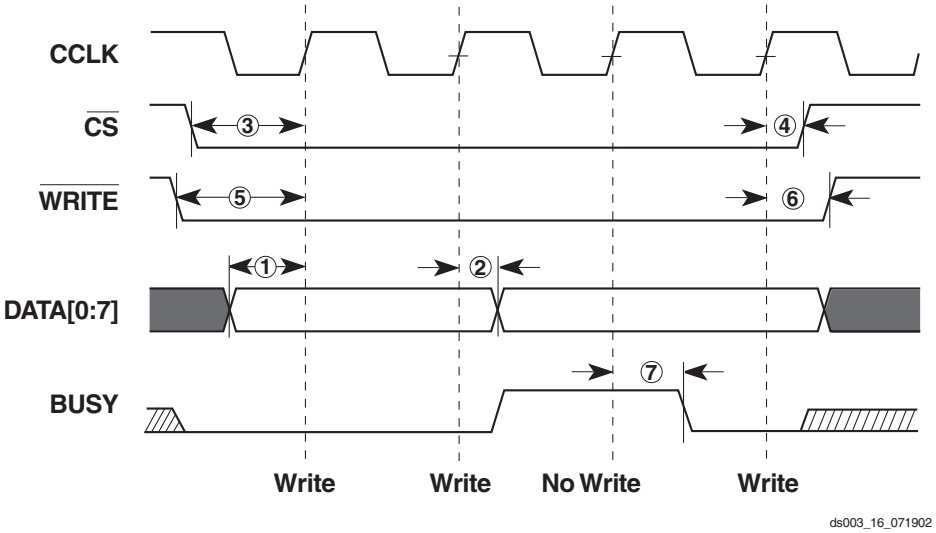


Figure 16: **Write Operations**

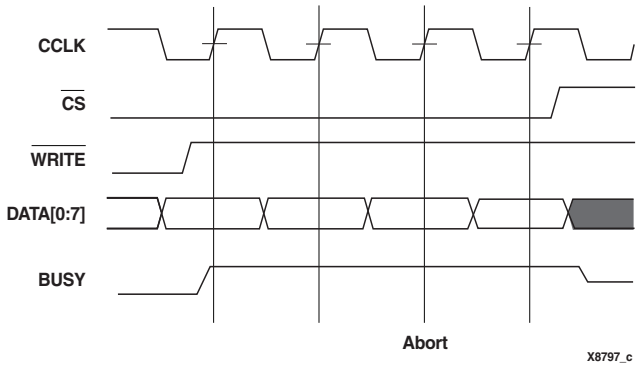


Figure 18: **SelectMAP Write Abort Waveforms**

Boundary-Scan Mode

In the boundary-scan mode, configuration is done through the IEEE 1149.1 Test Access Port. Note that the PROGRAM pin must be pulled High prior to reconfiguration. A Low on the PROGRAM pin resets the TAP controller and no JTAG operations can be performed.

Configuration through the TAP uses the CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port (when using TCK as a start-up clock).

1. Load the CFG_IN instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the JSTART instruction into IR
6. Enter the SDR state
7. Clock TCK through the startup sequence
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode is selected by a <101> or 001> on the mode pins (M2, M1, M0). For details on TAP characteristics, refer to XAPP139.

Configuration Sequence

The configuration of Virtex devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user, as described below. The configuration process can also be initiated by asserting PROGRAM.

The end of the memory-clearing phase is signalled by INIT going High, and the completion of the entire process is signalled by DONE going High.

The power-up timing of configuration signals is shown in Figure 19. The corresponding timing characteristics are listed in Table 10.

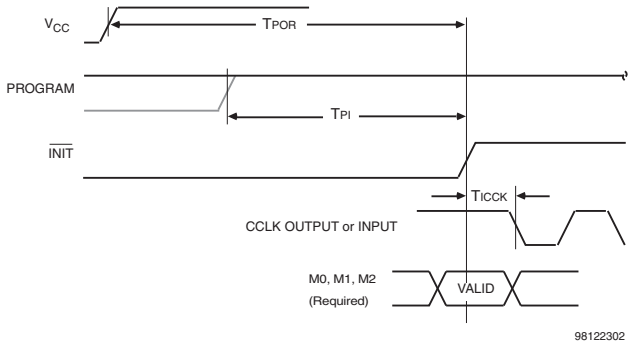


Figure 19: **Power-Up Timing Configuration Signals**

Table 10: **Power-up Timing Characteristics**

Description	Symbol	Value	Units
Power-on Reset	T_{POR}	2.0	ms, max
Program Latency	T_{PL}	100.0	µs, max
CCLK (output) Delay	T_{ICCK}	0.5	µs, min
		4.0	µs, max
Program Pulse Width	$T_{PROGRAM}$	300	ns, min

Delaying Configuration

INIT can be held Low using an open-drain driver. An open-drain is required since INIT is a bidirectional open-drain pin that is held Low by the FPGA while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

Start-Up Sequence

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed. In addition, the GTS, GSR, and GWE events can be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start in synchronism. The sequence can also be paused at any stage until lock has been achieved on any or all DLLs.

Description	Device	Symbol	Speed Grade				Units
			Min	-6	-5	-4	
Setup and Hold Times with respect to Clock CLK at IOB input register(1)			**Setup Time / Hold Time**				
Pad, no delay	All	T_{IOPICK}/T_{IOICKP}	0.8 / 0	1.6 / 0	1.8 / 0	2.0 / 0	ns, min
Pad, with delay	XCV50	$T_{IOPICKD}/T_{IOICKPD}$	1.9 / 0	3.7 / 0	4.1 / 0	4.7 / 0	ns, min
	XCV100		1.9 / 0	3.7 / 0	4.1 / 0	4.7 / 0	ns, min
	XCV150		1.9 / 0	3.8 / 0	4.3 / 0	4.9 / 0	ns, min
	XCV200		2.0 / 0	3.9 / 0	4.4 / 0	5.0 / 0	ns, min
	XCV300		2.0 / 0	3.9 / 0	4.4 / 0	5.0 / 0	ns, min
	XCV400		2.1 / 0	4.1 / 0	4.6 / 0	5.3 / 0	ns, min
	XCV600		2.1 / 0	4.2 / 0	4.7 / 0	5.4 / 0	ns, min
	XCV800		2.2 / 0	4.4 / 0	4.9 / 0	5.6 / 0	ns, min
	XCV1000		2.3 / 0	4.5 / 0	5.0 / 0	5.8 / 0	ns, min
ICE input	All	$T_{IOICECK}/T_{IOCKICE}$	0.37/ 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, max
Set/Reset Delays							
SR input (IFF, synchronous)	All	$T_{IOSRCKI}$	0.49	1.0	1.1	1.3	ns, max
SR input to IQ (asynchronous)	All	T_{IOSRIQ}	0.70	1.4	1.6	1.8	ns, max
GSR to output IQ	All	T_{GSRQ}	4.9	9.7	10.9	12.5	ns, max

Notes:
1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see Table 3.

IOB Input Switching Characteristics Standard Adjustments

Description	Symbol	Standard(1)	Speed Grade				Units
			Min	-6	-5	-4	
Data Input Delay Adjustments							
Standard-specific data input delay adjustments	T_{ILVTTL}	LVTTL	0	0	0	0	ns
	$T_{ILVCMOS2}$	LVCMOS2	–0.02	–0.04	–0.04	–0.05	ns
	T_{IPCI33_3}	PCI, 33 MHz, 3.3 V	–0.05	–0.11	–0.12	–0.14	ns
	T_{IPCI33_5}	PCI, 33 MHz, 5.0 V	0.13	0.25	0.28	0.33	ns
	T_{IPCI66_3}	PCI, 66 MHz, 3.3 V	–0.05	–0.11	–0.12	–0.14	ns
	T_{IGTL}	GTL	0.10	0.20	0.23	0.26	ns
	T_{IGTLP}	GTL+	0.06	0.11	0.12	0.14	ns
	T_{IHSTL}	HSTL	0.02	0.03	0.03	0.04	ns
	T_{ISSTL2}	SSTL2	–0.04	–0.08	–0.09	–0.10	ns
	T_{ISSTL3}	SSTL3	–0.02	–0.04	–0.05	–0.06	ns
	T_{ICTT}	CTT	0.01	0.02	0.02	0.02	ns
	T_{IAGP}	AGP	–0.03	–0.06	–0.07	–0.08	ns

Notes:
1. Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see Table 3.

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 9.

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Propagation Delays						
O input to Pad	T_{IOOP}	1.2	2.9	3.2	3.5	ns, max
O input to Pad via transparent latch	T_{IOOLP}	1.4	3.4	3.7	4.0	ns, max
3-State Delays						
T input to Pad high-impedance(1)	T_{IOTHZ}	1.0	2.0	2.2	2.4	ns, max
T input to valid data on Pad	T_{IOTON}	1.4	3.1	3.3	3.7	ns, max
T input to Pad high-impedance via transparent latch(1)	$T_{IOTLPHZ}$	1.2	2.4	2.6	3.0	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$	1.6	3.5	3.8	4.2	ns, max
GTS to Pad high impedance(1)	T_{GTS}	2.5	4.9	5.5	6.3	ns, max
Sequential Delays						
Clock CLK						
Minimum Pulse Width, High	T_{CH}	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low	T_{CL}	0.8	1.5	1.7	2.0	ns, min

Clock Distribution Guidelines

Description	Device	Symbol	Speed Grade			Units
			-6	-5	-4	
Global Clock Skew(1)						
Global Clock Skew between IOB Flip-flops	XCV50	$T_{GSKEWIOB}$	0.10	0.12	0.14	ns, max
	XCV100		0.12	0.13	0.15	ns, max
	XCV150		0.12	0.13	0.15	ns, max
	XCV200		0.13	0.14	0.16	ns, max
	XCV300		0.14	0.16	0.18	ns, max
	XCV400		0.13	0.13	0.14	ns, max
	XCV600		0.14	0.15	0.17	ns, max
	XCV800		0.16	0.17	0.20	ns, max
	XCV1000		0.20	0.23	0.25	ns, max

Notes:
1. These clock-skew delays are provided for guidance only. They reflect the delays encountered in a typical design under worst-case conditions. Precise values for a particular design are provided by the timing analyzer.

Clock Distribution Switching Characteristics

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
GCLK IOB and Buffer						
Global Clock PAD to output.	T_{GPIO}	0.33	0.7	0.8	0.9	ns, max
Global Clock Buffer I input to O output	T_{GIO}	0.34	0.7	0.8	0.9	ns, max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Combinatorial Delays						
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.29	0.6	0.7	0.8	ns, max
5-input function: F/G inputs to F5 output	T_{IF5}	0.32	0.7	0.8	0.9	ns, max
5-input function: F/G inputs to X output	T_{IF5X}	0.36	0.8	0.8	1.0	ns, max
6-input function: F/G inputs to Y output via F6 MUX	T_{IF6Y}	0.44	0.9	1.0	1.2	ns, max
6-input function: F5IN input to Y output	T_{F5INY}	0.17	0.32	0.36	0.42	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.31	0.7	0.7	0.8	ns, max
BY input to YB output	T_{BYYB}	0.27	0.53	0.6	0.7	ns, max
Sequential Delays						
FF Clock CLK to XQ/YQ outputs	T_{CKO}	0.54	1.1	1.2	1.4	ns, max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.6	1.2	1.4	1.6	ns, max
Setup and Hold Times before/after Clock CLK(1)	Setup Time / Hold Time					
4-input function: F/G Inputs	T_{ICK}/T_{CKI}	0.6 / 0	1.2 / 0	1.4 / 0	1.5 / 0	ns, min
5-input function: F/G inputs	T_{IF5CK}/T_{CKIF5}	0.7 / 0	1.3 / 0	1.5 / 0	1.7 / 0	ns, min
6-input function: F5IN input	T_{F5INCK}/T_{CKF5IN}	0.46 / 0	1.0 / 0	1.1 / 0	1.2 / 0	ns, min
6-input function: F/G inputs via F6 MUX	T_{IF6CK}/T_{CKIF6}	0.8 / 0	1.5 / 0	1.7 / 0	1.9 / 0	ns, min
BX/BY inputs	T_{DICK}/T_{CKDI}	0.30 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
CE input	T_{CECK}/T_{CKCE}	0.37 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
SR/BY inputs (synchronous)	$T_{RCK}T_{CKR}$	0.33 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{CH}	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low	T_{CL}	0.8	1.5	1.7	2.0	ns, min
Set/Reset						
Minimum Pulse Width, SR/BY inputs	T_{RPW}	1.3	2.5	2.8	3.3	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}	0.54	1.1	1.3	1.4	ns, max
Delay from GSR to XQ/YQ outputs	T_{IOGSRQ}	4.9	9.7	10.9	12.5	ns, max
Toggle Frequency (MHz) (for export control)	F_{TOG} (MHz)	625	333	294	250	MHz

Notes:
1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Virtex Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL

Description	Symbol	Device	Speed Grade				Units
			Min	-6	-5	-4	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DLL. For data *output* with different standards, adjust delays with the values shown in Output Delay Adjustments.	$T_{ICKOFDLL}$	XCV50	1.0	3.1	3.3	3.6	ns, max
		XCV100	1.0	3.1	3.3	3.6	ns, max
		XCV150	1.0	3.1	3.3	3.6	ns, max
		XCV200	1.0	3.1	3.3	3.6	ns, max
		XCV300	1.0	3.1	3.3	3.6	ns, max
		XCV400	1.0	3.1	3.3	3.6	ns, max
		XCV600	1.0	3.1	3.3	3.6	ns, max
		XCV800	1.0	3.1	3.3	3.6	ns, max
		XCV1000	1.0	3.1	3.3	3.6	ns, max

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see Table 2 and Table 3.
3. DLL output jitter is already included in the timing calculation.

Global Clock Input-to-Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL

Description	Symbol	Device	Speed Grade				Units
			Min	-6	-5	-4	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DLL. For data *output* with different standards, adjust delays with the values shown in Input and Output Delay Adjustments. For I/O standards requiring V_{REF}, such as GTL, GTL+, SSTL, HSTL, CTT, and AGO, an additional 600 ps must be added.	T_{ICKOF}	XCV50	1.5	4.6	5.1	5.7	ns, max
		XCV100	1.5	4.6	5.1	5.7	ns, max
		XCV150	1.5	4.7	5.2	5.8	ns, max
		XCV200	1.5	4.7	5.2	5.8	ns, max
		XCV300	1.5	4.7	5.2	5.9	ns, max
		XCV400	1.5	4.8	5.3	6.0	ns, max
		XCV600	1.6	4.9	5.4	6.0	ns, max
		XCV800	1.6	4.9	5.5	6.2	ns, max
		XCV1000	1.7	5.0	5.6	6.3	ns, max

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see Table 2 and Table 3.

Global Clock Set-Up and Hold for LVTTL Standard, *without* DLL

Description	Symbol	Device	Speed Grade				Units
			Min	-6	-5	-4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard.(2) For data input with different standards, adjust the setup time delay by the values shown in Input Delay Adjustments.							
Full Delay Global Clock and IFF, without DLL	T_{PSFD}/T_{PHFD}	XCV50	0.6 / 0	2.3 / 0	2.6 / 0	2.9 / 0	ns, min
		XCV100	0.6 / 0	2.3 / 0	2.6 / 0	3.0 / 0	ns, min
		XCV150	0.6 / 0	2.4 / 0	2.7 / 0	3.1 / 0	ns, min
		XCV200	0.7 / 0	2.5 / 0	2.8 / 0	3.2 / 0	ns, min
		XCV300	0.7 / 0	2.5 / 0	2.8 / 0	3.2 / 0	ns, min
		XCV400	0.7 / 0	2.6 / 0	2.9 / 0	3.3 / 0	ns, min
		XCV600	0.7 / 0	2.6 / 0	2.9 / 0	3.3 / 0	ns, min
		XCV800	0.7 / 0	2.7 / 0	3.1 / 0	3.5 / 0	ns, min
		XCV1000	0.7 / 0	2.8 / 0	3.1 / 0	3.6 / 0	ns, min

IFF = Input Flip-Flop or Latch

Notes: Notes:

1. Set-up time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
2. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Date	Version	Revision
01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
03/00	2.0	New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration.
05/00	2.1	Modified "Pins not listed..." statement. Speed grade update to Final status.
05/00	2.2	Modified Table 18.
09/00	2.3	• Added XCV400 values to table under **Minimum Clock-to-Out for Virtex Devices**. • Corrected Units column in table under **IOB Input Switching Characteristics**. • Added values to table under **CLB SelectRAM Switching Characteristics**.
10/00	2.4	• Corrected Pinout information for devices in the BG256, BG432, and BG560 packages in Table 18. • Corrected **BG256 Pin Function Diagram**.
04/02/01	2.5	• Revised minimums for **Global Clock Set-Up and Hold for LVTTL Standard, with DLL**. • Converted file to modularized format. See the **Virtex Data Sheet** section.
04/19/01	2.6	• Clarified TIOCKP and TIOCKON **IOB Output Switching Characteristics** descriptors.
07/19/01	2.7	• Under **Absolute Maximum Ratings**, changed (T_{SOL}) to 220 °C.
07/26/01	2.8	• Removed T_{SOL} parameter and added footnote to **Absolute Maximum Ratings** table.
10/29/01	2.9	• Updated the speed grade designations used in data sheets, and added Table 1, which shows the current speed grade designation for each device.
02/01/02	3.0	• Added footnote to **DC Input and Output Levels** table.
07/19/02	3.1	• Removed mention of MIL-M-38510/605 specification. • Added link to xapp158 from the **Power-On Power Supply Requirements** section.
09/10/02	3.2	• Added Clock CLK to **IOB Input Switching Characteristics** and **IOB Output Switching Characteristics**.
03/01/13	4.0	The products listed in this data sheet are obsolete. See **XCN10016** for further information.

Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

- DS003-1, Virtex 2.5V FPGAs:
  Introduction and Ordering Information (Module 1)
- DS003-2, Virtex 2.5V FPGAs:
  Functional Description (Module 2)
- DS003-3, Virtex 2.5V FPGAs:
  DC and Switching Characteristics (Module 3)
- DS003-4, Virtex 2.5V FPGAs:
  Pinout Tables (Module 4)

Table 2: **Virtex Pinout Tables (Chip-Scale and QFP Packages)** ***(Continued)***

Pin Name	Device	CS144	TQ144	PQ/HQ240
V_{CCO}	All	Banks 0 and 1: A2, A13, D7 Banks 2 and 3: B12, G11, M13 Banks 4 and 5: N1, N7, N13 Banks 6 and 7: B2, G2, M2	No I/O Banks in this package: 1, 17, 37, 55, 73, 92, 109, 128	No I/O Banks in this package: 15, 30, 44, 61, 76, 90, 105, 121, 136, 150, 165, 180, 197, 212, 226, 240
V_{REF}, Bank 0 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	C4, D6	5, 13	218, 232
	XCV100/150	... + B4	... + 7	... + 229
	XCV200/300	N/A	N/A	... + 236
	XCV400	N/A	N/A	... + 215
	XCV600	N/A	N/A	... + 230
	XCV800	N/A	N/A	... + 222
V_{REF}, Bank 1 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	A10, B8	22, 30	191, 205
	XCV100/150	... + D9	... + 28	... + 194
	XCV200/300	N/A	N/A	... + 187
	XCV400	N/A	N/A	... + 208
	XCV600	N/A	N/A	... + 193
	XCV800	N/A	N/A	... + 201
V_{REF}, Bank 2 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	D11, F10	42, 50	157, 171
	XCV100/150	... + D13	... + 44	... + 168
	XCV200/300	N/A	N/A	... + 175
	XCV400	N/A	N/A	... + 154
	XCV600	N/A	N/A	... + 169
	XCV800	N/A	N/A	... + 161

Table 3: **Virtex Pinout Tables (BGA)**

Pin Name	Device	BG256	BG352	BG432	BG560
GCK0	All	Y11	AE13	AL16	AL17
GCK1	All	Y10	AF14	AK16	AJ17
GCK2	All	A10	B14	A16	D17
GCK3	All	B10	D14	D17	A17
M0	All	Y1	AD24	AH28	AJ29
M1	All	U3	AB23	AH29	AK30
M2	All	W2	AC23	AJ28	AN32
CCLK	All	B19	C3	D4	C4
PROGRAM	All	Y20	AC4	AH3	AM1
DONE	All	W19	AD3	AH4	AJ5
INIT	All	U18	AD2	AJ2	AH5
BUSY/DOUT	All	D18	E4	D3	D4
D0/DIN	All	C19	D3	C2	E4
D1	All	E20	G1	K4	K3
D2	All	G19	J3	K2	L4
D3	All	J19	M3	P4	P3
D4	All	M19	R3	V4	W4
D5	All	P19	U4	AB1	AB5
D6	All	T20	V3	AB3	AC4
D7	All	V19	AC3	AG4	AJ4
WRITE	All	A19	D5	B4	D6
CS	All	B18	C4	D5	A2
TDI	All	C17	B3	B3	D5
TDO	All	A20	D4	C4	E6
TMS	All	D3	D23	D29	B33
TCK	All	A1	C24	D28	E29
DXN	All	W3	AD23	AH27	AK29
DXP	All	V4	AE24	AK29	AJ28

Pinout Diagrams

The following diagrams, **CS144 Pin Function Diagram**, page 17 through **FG680 Pin Function Diagram**, page 27, illustrate the locations of special-purpose pins on Virtex FPGAs. Table 5 lists the symbols used in these diagrams. The diagrams also show I/O-bank boundaries.

Table 5: **Pinout Diagram Symbols**

Symbol	Pin Function
✳	General I/O
❄	Device-dependent general I/O, n/c on smaller devices
V	V_{CCINT}
v	Device-dependent V_{CCINT}, n/c on smaller devices
O	V_{CCO}
R	V_{REF}
r	Device-dependent V_{REF}, remains I/O on smaller devices
G	Ground
Ø, 1, 2, 3	Global Clocks
⑩, ❶, ❷	M0, M1, M2
⑩, ①, ②, ③, ④, ⑤, ⑥, ⑦	D0/DIN, D1, D2, D3, D4, D5, D6, D7
B	DOUT/BUSY
D	DONE
P	$\overline{\text{PROGRAM}}$
I	$\overline{\text{INIT}}$
K	CCLK
W	$\overline{\text{WRITE}}$
S	$\overline{\text{CS}}$
T	Boundary-scan Test Access Port
+	Temperature diode, anode
–	Temperature diode, cathode
n	No connect

CS144 Pin Function Diagram

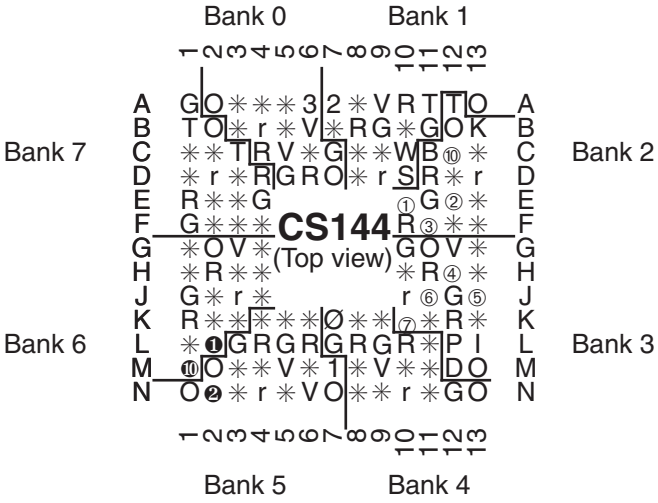


Figure 1: **CS144 Pin Function Diagram**

TQ144 Pin Function Diagram

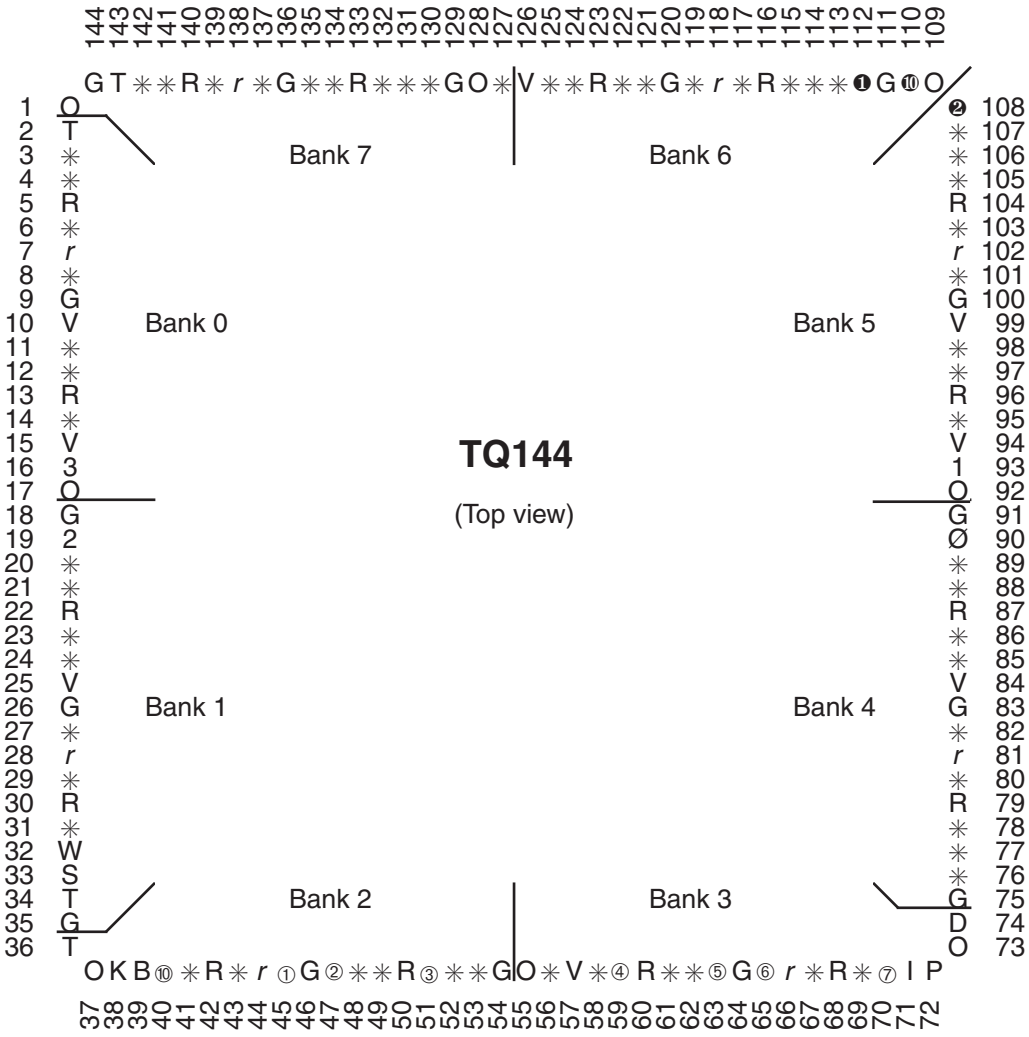


Figure 2: **TQ144 Pin Function Diagram**

BG432 Pin Function Diagram

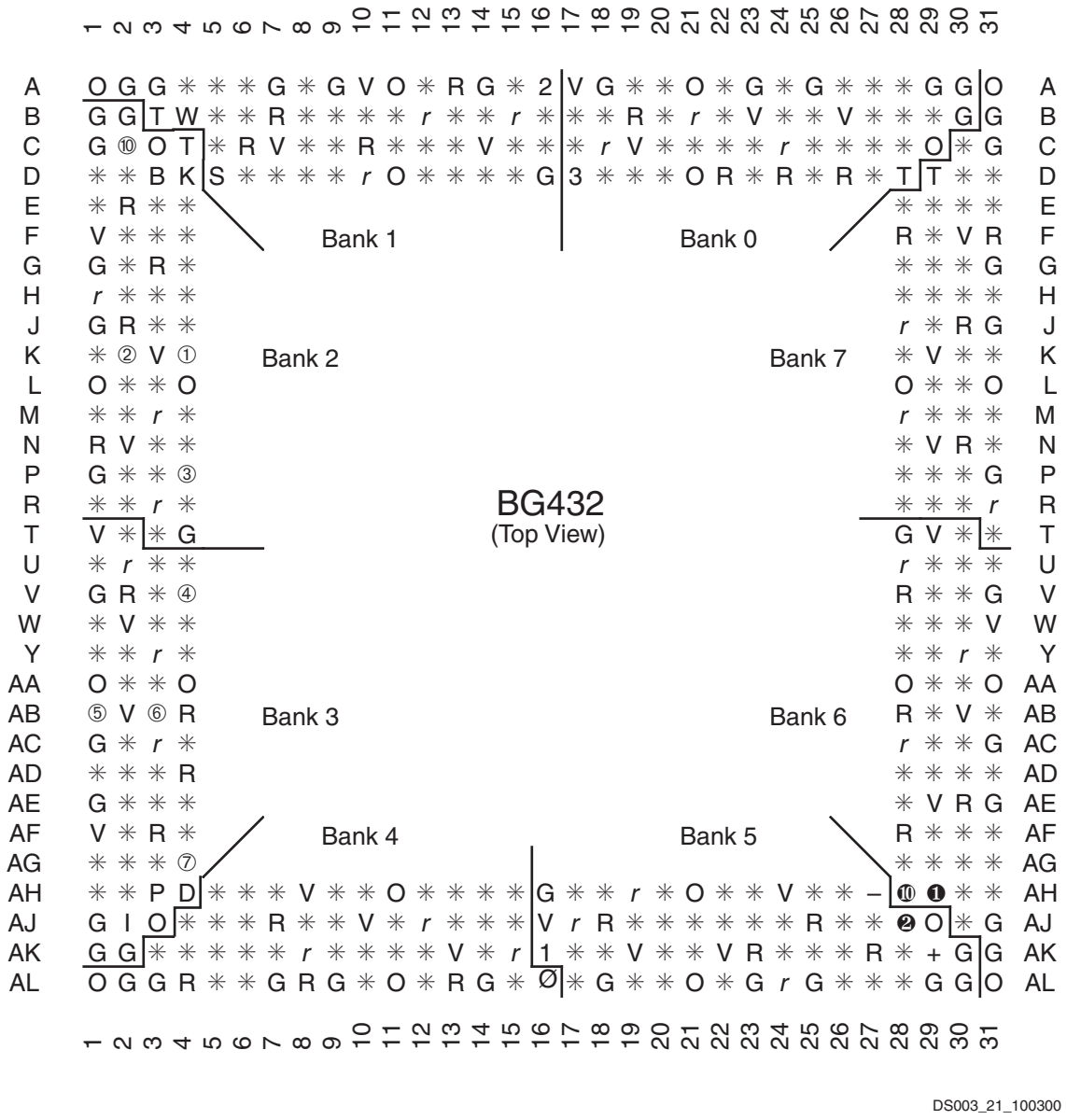


Figure 6: **BG432 Pin Function Diagram**

BG560 Pin Function Diagram

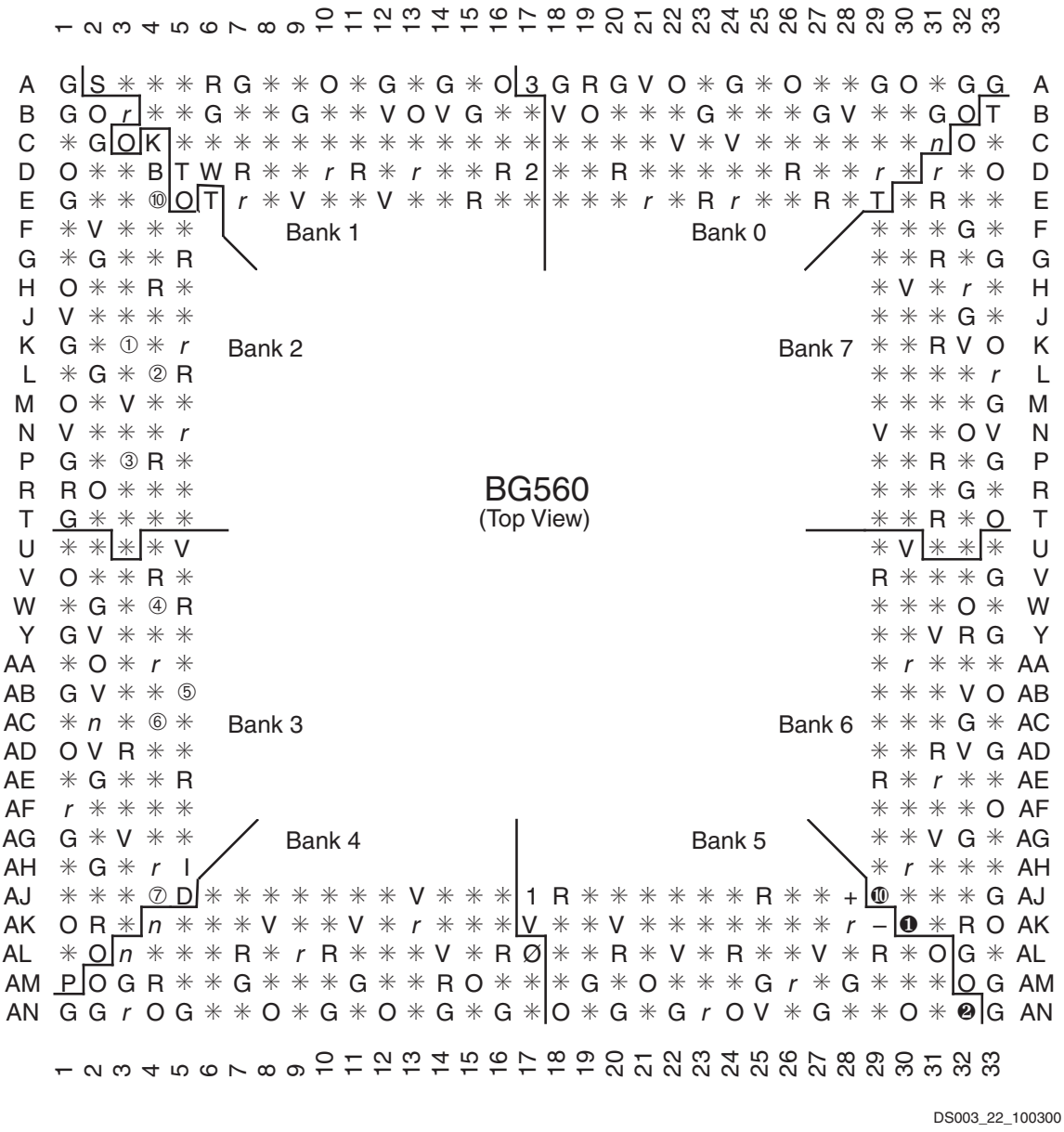
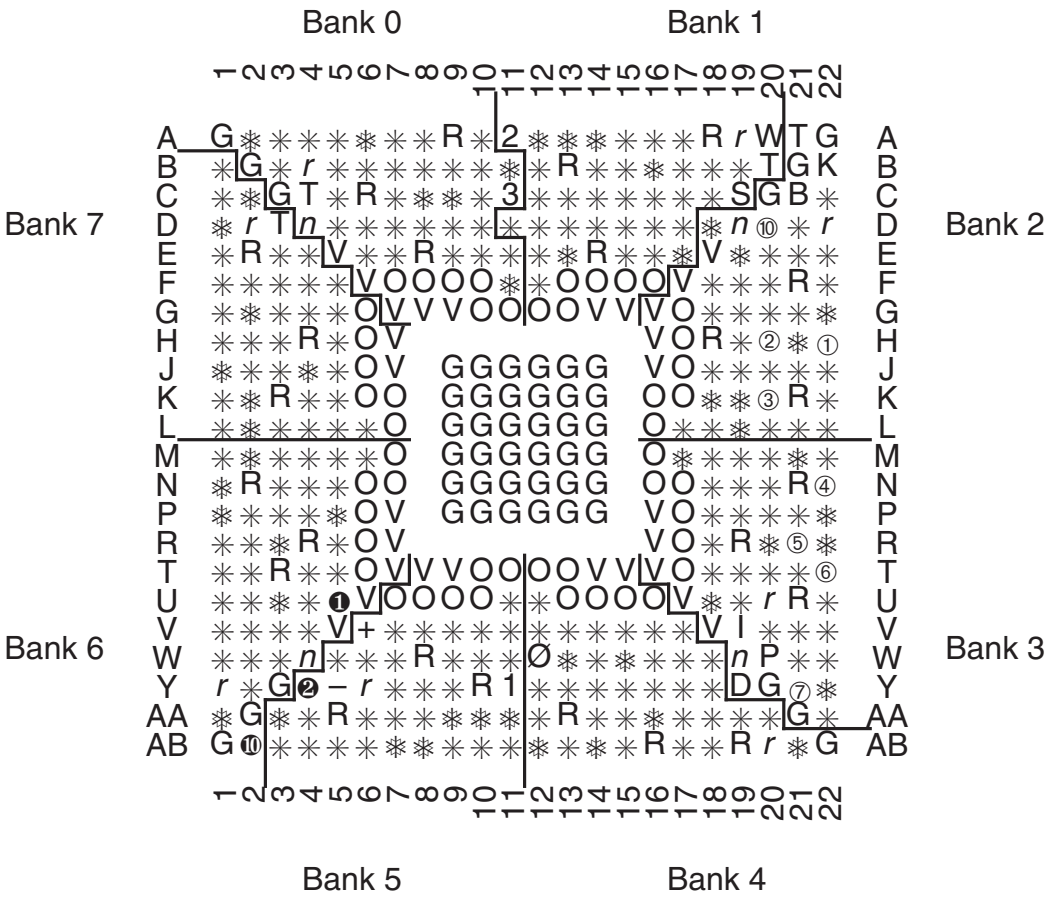


Figure 7: **BG560 Pin Function Diagram**

FG456 Pin Function Diagram



FG456
(Top view)

Figure 9: **FG456 Pin Function Diagram**

Notes:

Packages FG456 and FG676 are layout compatible.

Revision History

Date	Version	Revision
11/98	1.0	Initial Xilinx release.
01/99-02/99	1.2-1.3	Both versions updated package drawings and specs.
05/99	1.4	Addition of package drawings and specifications.
05/99	1.5	Replaced FG 676 & FG680 package drawings.
07/99	1.6	Changed Boundary Scan Information and changed Figure 11, Boundary Scan Bit Sequence. Updated IOB Input & Output delays. Added Capacitance info for different I/O Standards. Added 5 V tolerant information. Added DLL Parameters and waveforms and new Pin-to-pin Input and Output Parameter tables for Global Clock Input to Output and Setup and Hold. Changed Configuration Information including Figures 12, 14, 17 & 19. Added device-dependent listings for quiescent currents ICCINTQ and ICCOQ. Updated IOB Input and Output Delays based on default standard of LVTTL, 12 mA, Fast Slew Rate. Added IOB Input Switching Characteristics Standard Adjustments.
09/99	1.7	Speed grade update to preliminary status, Power-on specification and Clock-to-Out Minimums additions, "0" hold time listing explanation, quiescent current listing update, and Figure 6 ADDRA input label correction. Added T_{IJITCC} parameter, changed T_{OJIT} to T_{OPHASE}.
01/00	1.8	Update to speed.txt file 1.96. Corrections for CRs 111036,111137, 112697, 115479, 117153, 117154, and 117612. Modified notes for Recommended Operating Conditions (voltage and temperature). Changed Bank information for V_{CCO} in CS144 package on p.43.
01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
03/00	2.0	New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration.
05/00	2.1	Modified "Pins not listed..." statement. Speed grade update to Final status.
05/00	2.2	Modified Table 18.
09/00	2.3	• Added XCV400 values to table under **Minimum Clock-to-Out for Virtex Devices**. • Corrected Units column in table under **IOB Input Switching Characteristics**. • Added values to table under **CLB SelectRAM Switching Characteristics**.
10/00	2.4	• Corrected pinout info for devices in the BG256, BG432, and BG560 pkgs in Table 18. • Corrected **BG256 Pin Function Diagram**.
04/02/01	2.5	• Revised minimums for **Global Clock Set-Up and Hold for LVTTL Standard, with DLL**. • Converted file to modularized format. See section **Virtex Data Sheet**, below.
04/19/01	2.6	• Corrected pinout information for FG676 device in Table 4. (Added AB22 pin.)
07/19/01	2.7	• Clarified V_{CCINT} pinout information and added AE19 pin for BG352 devices in Table 3. • Changed pinouts listed for BG352 XCV400 devices in banks 0 thru 7.
07/19/02	2.8	• Changed pinouts listed for GND in TQ144 devices (see Table 2).
03/01/13	4.0	The products listed in this data sheet are obsolete. See **XCN10016** for further information.

Virtex Data Sheet

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- DS003-4, Virtex 2.5V FPGAs:
  Pinout Tables (Module 4)