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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 864 |
| Number of Logic Elements/Cells | 3888 |
| Total RAM Bits | 49152 |
| Number of I/O | 166 |
| Number of Gates | 164674 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 240-BFQFP |
| Supplier Device Package | 240-PQFP (32x32) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xcv150-4pq240i |

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## Virtex Device/Package Combinations and Maximum I/O

*Table 3:* **Virtex Family Maximum User I/O by Device/Package (Excluding Dedicated Clock Pins)**

| Package | XCV50 | XCV100 | XCV150 | XCV200 | XCV300 | XCV400 | XCV600 | XCV800 | XCV1000 |
|---|---|---|---|---|---|---|---|---|---|
| CS144 | 94 | 94 | | | | | | | |
| TQ144 | 98 | 98 | | | | | | | |
| PQ240 | 166 | 166 | 166 | 166 | 166 | | | | |
| HQ240 | | | | | | 166 | 166 | 166 | |
| BG256 | 180 | 180 | 180 | 180 | | | | | |
| BG352 | | | 260 | 260 | 260 | | | | |
| BG432 | | | | | 316 | 316 | 316 | 316 | |
| BG560 | | | | | | 404 | 404 | 404 | 404 |
| FG256 | 176 | 176 | 176 | 176 | | | | | |
| FG456 | | | 260 | 284 | 312 | | | | |
| FG676 | | | | | | 404 | 444 | 444 | |
| FG680 | | | | | | | 512 | 512 | 512 |

## Virtex Ordering Information

**Example: XCV300 -6 PQ 240 C**

Device Type

Speed Grade

-4
-5
-6

Temperature Range
C = Commercial ($T_J$ = 0°C to +85°C)
I = Industrial ($T_J$ = –40°C to +100°C)

Number of Pins

Package Type

BG = Ball Grid Array
FG = Fine-pitch Ball Grid Array
PQ = Plastic Quad Flat Pack
HQ = High Heat Dissipation QFP
TQ = Thin Quad Flat Pack
CS = Chip-scale Package

*Figure 1:* **Virtex Ordering Information**

## Revision History

| Date | Version | Revision |
|---|---|---|
| 11/98 | 1.0 | Initial Xilinx release. |
| 01/99-02/99 | 1.2-1.3 | Both versions updated package drawings and specs. |
| 05/99 | 1.4 | Addition of package drawings and specifications. |
| 05/99 | 1.5 | Replaced FG 676 & FG680 package drawings. |
| 07/99 | 1.6 | Changed Boundary Scan Information and changed Figure 11, Boundary Scan Bit Sequence. Updated IOB Input & Output delays. Added Capacitance info for different I/O Standards. Added 5 V tolerant information. Added DLL Parameters and waveforms and new Pin-to-pin Input and Output Parameter tables for Global Clock Input to Output and Setup and Hold. Changed Configuration Information including Figures 12, 14, 17 & 19. Added device-dependent listings for quiescent currents ICCINTQ and ICCOQ. Updated IOB Input and Output Delays based on default standard of LVTTL, 12 mA, Fast Slew Rate. Added IOB Input Switching Characteristics Standard Adjustments. |
| 09/99 | 1.7 | Speed grade update to preliminary status, Power-on specification and Clock-to-Out Minimums additions, "0" hold time listing explanation, quiescent current listing update, and Figure 6 ADDRA input label correction. Added $T_{IJITCC}$ parameter, changed $T_{OJIT}$ to $T_{OPHASE}$. |
| 01/00 | 1.8 | Update to speed.txt file 1.96. Corrections for CRs 111036,111137, 112697, 115479, 117153, 117154, and 117612. Modified notes for Recommended Operating Conditions (voltage and temperature). Changed Bank information for $V_{CCO}$ in CS144 package on p.43. |
| 01/00 | 1.9 | Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes. |
| 03/00 | 2.0 | New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration. |
| 05/00 | 2.1 | Modified "Pins not listed..." statement. Speed grade update to Final status. |
| 05/00 | 2.2 | Modified Table 18. |
| 09/00 | 2.3 | • Added XCV400 values to table under **Minimum Clock-to-Out for Virtex Devices**.<br>• Corrected Units column in table under **IOB Input Switching Characteristics**.<br>• Added values to table under **CLB SelectRAM Switching Characteristics**. |
| 10/00 | 2.4 | • Corrected Pinout information for devices in the BG256, BG432, and BG560 packages in Table 18.<br>• Corrected **BG256 Pin Function Diagram**. |
| 04/01 | 2.5 | • Revised minimums for **Global Clock Set-Up and Hold for LVTTL Standard, with DLL**.<br>• Converted file to modularized format. See **Virtex Data Sheet** section. |
| 03/13 | 4.0 | The products listed in this data sheet are obsolete. See XCN10016 for further information. |

## Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

- DS003-1, Virtex 2.5V FPGAs:
  Introduction and Ordering Information (Module 1)
- DS003-2, Virtex 2.5V FPGAs:
  Functional Description (Module 2)
- DS003-3, Virtex 2.5V FPGAs:
  DC and Switching Characteristics (Module 3)
- DS003-4, Virtex 2.5V FPGAs:
  Pinout Tables (Module 4)

XILINX®

# Virtex™ 2.5 V Field Programmable Gate Arrays

DS003-2 (v4.0) March 1, 2013 **Product Specification**

## Architectural Description

### Virtex Array

The Virtex user-programmable gate array, shown in Figure 1, comprises two major configurable elements: configurable logic blocks (CLBs) and input/output blocks (IOBs).

- CLBs provide the functional elements for constructing logic
- IOBs provide the interface between the package pins and the CLBs

CLBs interconnect through a general routing matrix (GRM). The GRM comprises an array of routing switches located at the intersections of horizontal and vertical routing channels. Each CLB nests into a VersaBlock™ that also provides local routing resources to connect the CLB to the GRM.

The VersaRing™ I/O interface provides additional routing resources around the periphery of the device. This routing improves I/O routability and facilitates pin locking.

The Virtex architecture also includes the following circuits that connect to the GRM.

- Dedicated block memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- 3-State buffers (BUFTs) associated with each CLB that drive dedicated segmentable horizontal routing resources

Values stored in static memory cells control the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

### Input/Output Block

The Virtex IOB, Figure 2, features SelectIO™ inputs and outputs that support a wide variety of I/O signalling standards, see Table 1.

The three IOB storage elements function either as edge-triggered D-type flip-flops or as level sensitive latches. Each IOB has a clock signal (CLK) shared by the three flip-flops and independent clock enable signals for each flip-flop.

In addition to the CLK and CE control signals, the three flip-flops share a Set/Reset (SR). For each flip-flop, this signal can be independently configured as a synchronous Set, a synchronous Reset, an asynchronous Preset, or an asynchronous Clear.

The output buffer and all of the IOB control signals have independent polarity controls.

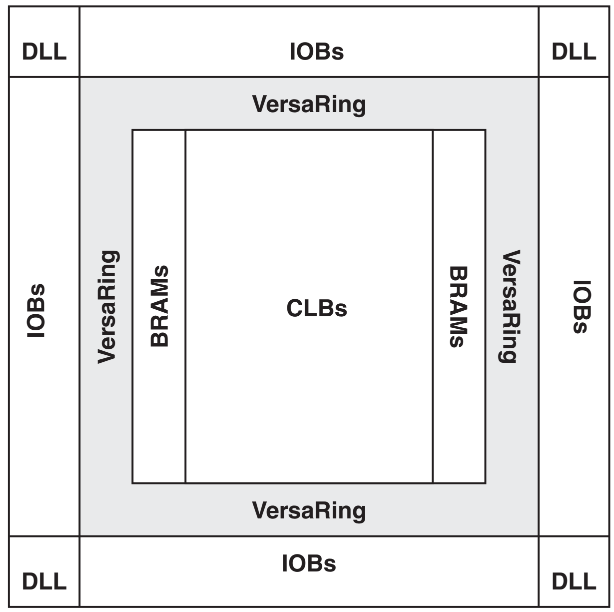


*Figure 1:* **Virtex Architecture Overview**

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Two forms of over-voltage protection are provided, one that permits 5 V compliance, and one that does not. For 5 V compliance, a Zener-like structure connected to ground turns on when the output rises to approximately 6.5 V. When PCI 3.3 V compliance is required, a conventional clamp diode is connected to the output supply voltage, $V_{CCO}$.

Optional pull-up and pull-down resistors and an optional weak-keeper circuit are attached to each pad. Prior to configuration, all pins not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but inputs can optionally be pulled up.

The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins will float. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All Virtex IOBs support IEEE 1149.1-compatible boundary scan testing.

more I/O pins convert to $V_{REF}$ pins. Since these are always a superset of the $V_{REF}$ pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary. All the $V_{REF}$ pins for the largest device anticipated must be connected to the $V_{REF}$ voltage, and not used for I/O.

In smaller devices, some $V_{CCO}$ pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or can be connected to the $V_{CCO}$ voltage to permit migration to a larger device if necessary.

In TQ144 and PQ/HQ240 packages, all $V_{CCO}$ pins are bonded together internally, and consequently the same $V_{CCO}$ voltage must be connected to all of them. In the CS144 package, bank pairs that share a side are interconnected internally, permitting four choices for $V_{CCO}$. In both cases, the $V_{REF}$ pins remain internally connected as eight banks, and can be used as described previously.

## Configurable Logic Block

The basic building block of the Virtex CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and a storage element. The output from the function generator in each LC drives both the CLB output and the D input of the flip-flop. Each Virtex CLB contains four LCs, organized in two similar slices, as shown in Figure 4.

Figure 5 shows a more detailed view of a single slice.

In addition to the four basic LCs, the Virtex CLB contains logic that combines function generators to provide functions of five or six inputs. Consequently, when estimating the number of system gates provided by a given device, each CLB counts as 4.5 LCs.

### *Look-Up Tables*

Virtex function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16x1-bit dual-port synchronous RAM.

The Virtex LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

### *Storage Elements*

The storage elements in the Virtex slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by the function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each Slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals can be configured to operate asynchronously. All of the control signals are independently invertible, and are shared by the two flip-flops within the slice.

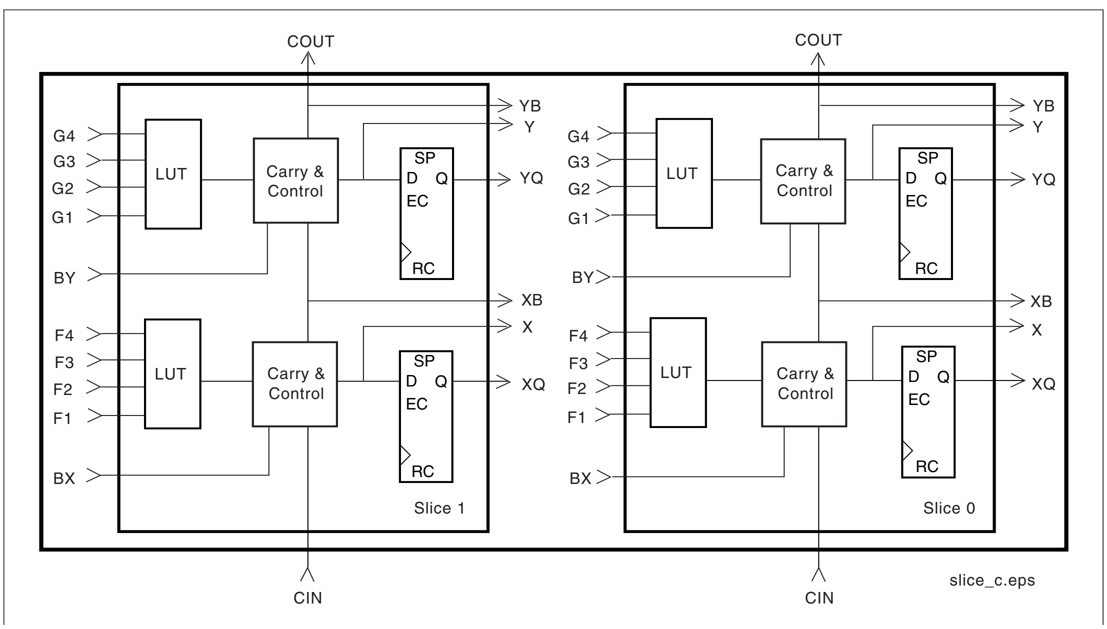


*Figure 4:* **2-Slice Virtex CLB**

ers with a common user interface regardless of their choice of entry and verification tools. The XDM software simplifies the selection of implementation options with pull-down menus and on-line help.

Application programs ranging from schematic capture to Placement and Routing (PAR) can be accessed through the XDM software. The program command sequence is generated prior to execution, and stored for documentation.

Several advanced software features facilitate Virtex design. RPMs, for example, are schematic-based macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the Xilinx FPGA Foundation development system provides interfaces to the following synthesis design environments.

- Synopsys (FPGA Compiler, FPGA Express)
- Exemplar (Spectrum)
- Synplicity (Synplify)

For schematic design entry, the Xilinx FPGA Foundation and alliance development system provides interfaces to the following schematic-capture design environments.

- Mentor Graphics V8 (Design Architect, QuickSim II)
- Viewlogic Systems (Viewdraw)

Third-party vendors support many other environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Virtex FPGAs supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The “soft macro” portion of the library contains detailed descriptions of common logic functions, but does not contain any partitioning or placement information. The performance of these macros depends, therefore, on the partitioning and placement obtained during implementation.

RPMs, on the other hand, do contain predetermined partitioning and placement information that permits optimal implementation of these functions. Users can create their own library of soft macros or RPMs based on the macros and primitives in the standard library.

The design environment supports hierarchical design entry, with high-level schematics that comprise major functional blocks, while lower-level schematics define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

## Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF net list for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floor planning.

The implementation software incorporates Timing Wizard® timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered on a schematic in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

## Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the net list for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the TRACE® static timing analyzer.

For in-circuit debugging, the development system includes a download and readback cable. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

## DC Characteristics Over Recommended Operating Conditions

| Symbol | Description | Device | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{DRINT}$ | Data Retention $V_{CCINT}$ Voltage (below which configuration data can be lost) | All | 2.0 | | V |
| $V_{DRIO}$ | Data Retention $V_{CCO}$ Voltage (below which configuration data can be lost) | All | 1.2 | | V |
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current[1,3] | XCV50 | | 50 | mA |
| | | XCV100 | | 50 | mA |
| | | XCV150 | | 50 | mA |
| | | XCV200 | | 75 | mA |
| | | XCV300 | | 75 | mA |
| | | XCV400 | | 75 | mA |
| | | XCV600 | | 100 | mA |
| | | XCV800 | | 100 | mA |
| | | XCV1000 | | 100 | mA |
| $I_{CCOQ}$ | Quiescent $V_{CCO}$ supply current[1] | XCV50 | | 2 | mA |
| | | XCV100 | | 2 | mA |
| | | XCV150 | | 2 | mA |
| | | XCV200 | | 2 | mA |
| | | XCV300 | | 2 | mA |
| | | XCV400 | | 2 | mA |
| | | XCV600 | | 2 | mA |
| | | XCV800 | | 2 | mA |
| | | XCV1000 | | 2 | mA |
| $I_{REF}$ | $V_{REF}$ current per $V_{REF}$ pin | All | | 20 | µA |
| $I_L$ | Input or output leakage current | All | –10 | +10 | µA |
| $C_{IN}$ | Input capacitance (sample tested) — BGA, PQ, HQ, packages | All | | 8 | pF |
| $I_{RPU}$ | Pad pull-up (when selected) @ $V_{in}$ = 0 V, $V_{CCO}$ = 3.3 V (sample tested) | All | Note (2) | 0.25 | mA |
| $I_{RPD}$ | Pad pull-down (when selected) @ $V_{in}$ = 3.6 V (sample tested) | | Note (2) | 0.15 | mA |

**Notes:**
1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.
3. Multiply $I_{CCINTQ}$ limit by two for industrial grade.

| Description | Symbol | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | Min | -6 | -5 | -4 | |
| Clock CLK to Pad delay with OBUFT enabled (non-3-state) | $T_{IOCKP}$ | 1.0 | 2.9 | 3.2 | 3.5 | ns, max |
| Clock CLK to Pad high-impedance (synchronous)(1) | $T_{IOCKHZ}$ | 1.1 | 2.3 | 2.5 | 2.9 | ns, max |
| Clock CLK to valid data on Pad delay, plus enable delay for OBUFT | $T_{IOCKON}$ | 1.5 | 3.4 | 3.7 | 4.1 | ns, max |
| **Setup and Hold Times before/after Clock CLK(2)** | | **Setup Time / Hold Time** | | | | |
| O input | $T_{IOOCK}/T_{IOCKO}$ | 0.51 / 0 | 1.1 / 0 | 1.2 / 0 | 1.3 / 0 | ns, min |
| OCE input | $T_{IOOCECK}/T_{IOCKOCE}$ | 0.37 / 0 | 0.8 / 0 | 0.9 / 0 | 1.0 / 0 | ns, min |
| SR input (OFF) | $T_{IOSRCKO}/T_{IOCKOSR}$ | 0.52 / 0 | 1.1 / 0 | 1.2 / 0 | 1.4 / 0 | ns, min |
| 3-State Setup Times, T input | $T_{IOTCK}/T_{IOCKT}$ | 0.34 / 0 | 0.7 / 0 | 0.8 / 0 | 0.9 / 0 | ns, min |
| 3-State Setup Times, TCE input | $T_{IOTCECK}/T_{IOCKTCE}$ | 0.41 / 0 | 0.9 / 0 | 0.9 / 0 | 1.1 / 0 | ns, min |
| 3-State Setup Times, SR input (TFF) | $T_{IOSRCKT}/T_{IOCKTSR}$ | 0.49 / 0 | 1.0 / 0 | 1.1 / 0 | 1.3 / 0 | ns, min |
| **Set/Reset Delays** | | | | | | |
| SR input to Pad (asynchronous) | $T_{IOSRP}$ | 1.6 | 3.8 | 4.1 | 4.6 | ns, max |
| SR input to Pad high-impedance (asynchronous)(1) | $T_{IOSRHZ}$ | 1.6 | 3.1 | 3.4 | 3.9 | ns, max |
| SR input to valid data on Pad (asynchronous) | $T_{IOSRON}$ | 2.0 | 4.2 | 4.6 | 5.1 | ns, max |
| GSR to Pad | $T_{IOGSRQ}$ | 4.9 | 9.7 | 10.9 | 12.5 | ns, max |

**Notes:**
1. 3-state turn-off delays should not be adjusted.
2. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

## IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

| Description | Symbol | Standard(1) | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | -6 | -5 | -4 | |
| **Output Delay Adjustments** | | | | | | | |
| Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl) | $T_{OLVTTL\_S2}$ | LVTTL, Slow, 2 mA | 4.2 | 14.7 | 15.8 | 17.0 | ns |
| | $T_{OLVTTL\_S4}$ | 4 mA | 2.5 | 7.5 | 8.0 | 8.6 | ns |
| | $T_{OLVTTL\_S6}$ | 6 mA | 1.8 | 4.8 | 5.1 | 5.6 | ns |
| | $T_{OLVTTL\_S8}$ | 8 mA | 1.2 | 3.0 | 3.3 | 3.5 | ns |
| | $T_{OLVTTL\_S12}$ | 12 mA | 1.0 | 1.9 | 2.1 | 2.2 | ns |
| | $T_{OLVTTL\_S16}$ | 16 mA | 0.9 | 1.7 | 1.9 | 2.0 | ns |
| | $T_{OLVTTL\_S24}$ | 24 mA | 0.8 | 1.3 | 1.4 | 1.6 | ns |
| | $T_{OLVTTL\_F2}$ | LVTTL, Fast, 2mA | 1.9 | 13.1 | 14.0 | 15.1 | ns |
| | $T_{OLVTTL\_F4}$ | 4 mA | 0.7 | 5.3 | 5.7 | 6.1 | ns |
| | $T_{OLVTTL\_F6}$ | 6 mA | 0.2 | 3.1 | 3.3 | 3.6 | ns |
| | $T_{OLVTTL\_F8}$ | 8 mA | 0.1 | 1.0 | 1.1 | 1.2 | ns |
| | $T_{OLVTTL\_F12}$ | 12 mA | 0 | 0 | 0 | 0 | ns |
| | $T_{OLVTTL\_F16}$ | 16 mA | –0.10 | –0.05 | –0.05 | –0.05 | ns |
| | $T_{OLVTTL\_F24}$ | 24 mA | –0.10 | –0.20 | –0.21 | –0.23 | ns |
| | $T_{OLVCMOS2}$ | LVCMOS2 | 0.10 | 0.10 | 0.11 | 0.12 | ns |
| | $T_{OPCI33\_3}$ | PCI, 33 MHz, 3.3 V | 0.50 | 2.3 | 2.5 | 2.7 | ns |
| | $T_{OPCI33\_5}$ | PCI, 33 MHz, 5.0 V | 0.40 | 2.8 | 3.0 | 3.3 | ns |
| | $T_{OPCI66\_3}$ | PCI, 66 MHz, 3.3 V | 0.10 | –0.40 | –0.42 | –0.46 | ns |
| | $T_{OGTL}$ | GTL | 0.6 | 0.50 | 0.54 | 0.6 | ns |
| | $T_{OGTLP}$ | GTL+ | 0.7 | 0.8 | 0.9 | 1.0 | ns |
| | $T_{OHSTL\_I}$ | HSTL I | 0.10 | –0.50 | –0.53 | –0.5 | ns |
| | $T_{OHSTL\_III}$ | HSTL III | –0.10 | –0.9 | –0.9 | –1.0 | ns |
| | $T_{OHSTL\_IV}$ | HSTL IV | –0.20 | –1.0 | –1.0 | –1.1 | ns |
| | $T_{OSSTL2\_I}$ | SSTL2 I | –0.10 | –0.50 | –0.53 | –0.5 | ns |
| | $T_{OSSLT2\_II}$ | SSTL2 II | –0.20 | –0.9 | –0.9 | –1.0 | ns |
| | $T_{OSSTL3\_I}$ | SSTL3 I | –0.20 | –0.50 | –0.53 | –0.5 | ns |
| | $T_{OSSTL3\_II}$ | SSTL3 II | –0.30 | –1.0 | –1.0 | –1.1 | ns |
| | $T_{OCTT}$ | CTT | 0 | –0.6 | –0.6 | –0.6 | ns |
| | $T_{OAGP}$ | AGP | 0 | –0.9 | –0.9 | –1.0 | ns |

**Notes:**

1. Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see Table 2 and Table 3.

## Clock Distribution Guidelines

| Description | Device | Symbol | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -6 | -5 | -4 | |
| Global Clock Skew[1] | | | | | | |
| Global Clock Skew between IOB Flip-flops | XCV50 | $T_{GSKEWIOB}$ | 0.10 | 0.12 | 0.14 | ns, max |
| | XCV100 | | 0.12 | 0.13 | 0.15 | ns, max |
| | XCV150 | | 0.12 | 0.13 | 0.15 | ns, max |
| | XCV200 | | 0.13 | 0.14 | 0.16 | ns, max |
| | XCV300 | | 0.14 | 0.16 | 0.18 | ns, max |
| | XCV400 | | 0.13 | 0.13 | 0.14 | ns, max |
| | XCV600 | | 0.14 | 0.15 | 0.17 | ns, max |
| | XCV800 | | 0.16 | 0.17 | 0.20 | ns, max |
| | XCV1000 | | 0.20 | 0.23 | 0.25 | ns, max |

**Notes:**
1. These clock-skew delays are provided for guidance only. They reflect the delays encountered in a typical design under worst-case conditions. Precise values for a particular design are provided by the timing analyzer.

## Clock Distribution Switching Characteristics

| Description | Symbol | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | Min | -6 | -5 | -4 | |
| GCLK IOB and Buffer | | | | | | |
| Global Clock PAD to output. | $T_{GPIO}$ | 0.33 | 0.7 | 0.8 | 0.9 | ns, max |
| Global Clock Buffer I input to O output | $T_{GIO}$ | 0.34 | 0.7 | 0.8 | 0.9 | ns, max |

## CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

| Description | Symbol | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | Min | -6 | -5 | -4 | |
| Combinatorial Delays | | | | | | |
| 4-input function: F/G inputs to X/Y outputs | $T_{ILO}$ | 0.29 | 0.6 | 0.7 | 0.8 | ns, max |
| 5-input function: F/G inputs to F5 output | $T_{IF5}$ | 0.32 | 0.7 | 0.8 | 0.9 | ns, max |
| 5-input function: F/G inputs to X output | $T_{IF5X}$ | 0.36 | 0.8 | 0.8 | 1.0 | ns, max |
| 6-input function: F/G inputs to Y output via F6 MUX | $T_{IF6Y}$ | 0.44 | 0.9 | 1.0 | 1.2 | ns, max |
| 6-input function: F5IN input to Y output | $T_{F5INY}$ | 0.17 | 0.32 | 0.36 | 0.42 | ns, max |
| Incremental delay routing through transparent latch to XQ/YQ outputs | $T_{IFNCTL}$ | 0.31 | 0.7 | 0.7 | 0.8 | ns, max |
| BY input to YB output | $T_{BYYB}$ | 0.27 | 0.53 | 0.6 | 0.7 | ns, max |
| Sequential Delays | | | | | | |
| FF Clock CLK to XQ/YQ outputs | $T_{CKO}$ | 0.54 | 1.1 | 1.2 | 1.4 | ns, max |
| Latch Clock CLK to XQ/YQ outputs | $T_{CKLO}$ | 0.6 | 1.2 | 1.4 | 1.6 | ns, max |
| Setup and Hold Times before/after Clock CLK[(1)] | Setup Time / Hold Time | | | | | |
| 4-input function: F/G Inputs | $T_{ICK}/T_{CKI}$ | 0.6 / 0 | 1.2 / 0 | 1.4 / 0 | 1.5 / 0 | ns, min |
| 5-input function: F/G inputs | $T_{IF5CK}/T_{CKIF5}$ | 0.7 / 0 | 1.3 / 0 | 1.5 / 0 | 1.7 / 0 | ns, min |
| 6-input function: F5IN input | $T_{F5INCK}/T_{CKF5IN}$ | 0.46 / 0 | 1.0 / 0 | 1.1 / 0 | 1.2 / 0 | ns, min |
| 6-input function: F/G inputs via F6 MUX | $T_{IF6CK}/T_{CKIF6}$ | 0.8 / 0 | 1.5 / 0 | 1.7 / 0 | 1.9 / 0 | ns, min |
| BX/BY inputs | $T_{DICK}/T_{CKDI}$ | 0.30 / 0 | 0.6 / 0 | 0.7 / 0 | 0.8 / 0 | ns, min |
| CE input | $T_{CECK}/T_{CKCE}$ | 0.37 / 0 | 0.8 / 0 | 0.9 / 0 | 1.0 / 0 | ns, min |
| SR/BY inputs (synchronous) | $T_{RCK}T_{CKR}$ | 0.33 / 0 | 0.7 / 0 | 0.8 / 0 | 0.9 / 0 | ns, min |
| Clock CLK | | | | | | |
| Minimum Pulse Width, High | $T_{CH}$ | 0.8 | 1.5 | 1.7 | 2.0 | ns, min |
| Minimum Pulse Width, Low | $T_{CL}$ | 0.8 | 1.5 | 1.7 | 2.0 | ns, min |
| Set/Reset | | | | | | |
| Minimum Pulse Width, SR/BY inputs | $T_{RPW}$ | 1.3 | 2.5 | 2.8 | 3.3 | ns, min |
| Delay from SR/BY inputs to XQ/YQ outputs (asynchronous) | $T_{RQ}$ | 0.54 | 1.1 | 1.3 | 1.4 | ns, max |
| Delay from GSR to XQ/YQ outputs | $T_{IOGSRQ}$ | 4.9 | 9.7 | 10.9 | 12.5 | ns, max |
| Toggle Frequency (MHz) (for export control) | $F_{TOG}$ (MHz) | 625 | 333 | 294 | 250 | MHz |

**Notes:**

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

## Virtex Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

### Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL

| Description | Symbol | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | -6 | -5 | -4 | |
| LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DLL. For data *output* with different standards, adjust delays with the values shown in Output Delay Adjustments. | $T_{ICKOFDLL}$ | XCV50 | 1.0 | 3.1 | 3.3 | 3.6 | ns, max |
| | | XCV100 | 1.0 | 3.1 | 3.3 | 3.6 | ns, max |
| | | XCV150 | 1.0 | 3.1 | 3.3 | 3.6 | ns, max |
| | | XCV200 | 1.0 | 3.1 | 3.3 | 3.6 | ns, max |
| | | XCV300 | 1.0 | 3.1 | 3.3 | 3.6 | ns, max |
| | | XCV400 | 1.0 | 3.1 | 3.3 | 3.6 | ns, max |
| | | XCV600 | 1.0 | 3.1 | 3.3 | 3.6 | ns, max |
| | | XCV800 | 1.0 | 3.1 | 3.3 | 3.6 | ns, max |
| | | XCV1000 | 1.0 | 3.1 | 3.3 | 3.6 | ns, max |

**Notes:**
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see Table 2 and Table 3.
3. DLL output jitter is already included in the timing calculation.

### Global Clock Input-to-Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL

| Description | Symbol | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | -6 | -5 | -4 | |
| LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DLL. For data *output* with different standards, adjust delays with the values shown in Input and Output Delay Adjustments. For I/O standards requiring $V_{REF}$, such as GTL, GTL+, SSTL, HSTL, CTT, and AGO, an additional 600 ps must be added. | $T_{ICKOF}$ | XCV50 | 1.5 | 4.6 | 5.1 | 5.7 | ns, max |
| | | XCV100 | 1.5 | 4.6 | 5.1 | 5.7 | ns, max |
| | | XCV150 | 1.5 | 4.7 | 5.2 | 5.8 | ns, max |
| | | XCV200 | 1.5 | 4.7 | 5.2 | 5.8 | ns, max |
| | | XCV300 | 1.5 | 4.7 | 5.2 | 5.9 | ns, max |
| | | XCV400 | 1.5 | 4.8 | 5.3 | 6.0 | ns, max |
| | | XCV600 | 1.6 | 4.9 | 5.4 | 6.0 | ns, max |
| | | XCV800 | 1.6 | 4.9 | 5.5 | 6.2 | ns, max |
| | | XCV1000 | 1.7 | 5.0 | 5.6 | 6.3 | ns, max |

**Notes:**
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see Table 2 and Table 3.

## Virtex Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

### Global Clock Set-Up and Hold for LVTTL Standard, *with* DLL

| Description | Symbol | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | -6 | -5 | -4 | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in Input Delay Adjustments. | | | | | | | |
| No Delay<br>Global Clock and IFF, with DLL | $T_{PSDLL}/T_{PHDLL}$ | XCV50 | 0.40 / –0.4 | 1.7 /–0.4 | 1.8 /–0.4 | 2.1 /–0.4 | ns, min |
| | | XCV100 | 0.40 /–0.4 | 1.7 /–0.4 | 1.9 /–0.4 | 2.1 /–0.4 | ns, min |
| | | XCV150 | 0.40 /–0.4 | 1.7 /–0.4 | 1.9 /–0.4 | 2.1 /–0.4 | ns, min |
| | | XCV200 | 0.40 /–0.4 | 1.7 /–0.4 | 1.9 /–0.4 | 2.1 /–0.4 | ns, min |
| | | XCV300 | 0.40 /–0.4 | 1.7 /–0.4 | 1.9 /–0.4 | 2.1 /–0.4 | ns, min |
| | | XCV400 | 0.40 /–0.4 | 1.7 /–0.4 | 1.9 /–0.4 | 2.1 /–0.4 | ns, min |
| | | XCV600 | 0.40 /–0.4 | 1.7 /–0.4 | 1.9 /–0.4 | 2.1 /–0.4 | ns, min |
| | | XCV800 | 0.40 /–0.4 | 1.7 /–0.4 | 1.9 /–0.4 | 2.1 /–0.4 | ns, min |
| | | XCV1000 | 0.40 /–0.4 | 1.7 /–0.4 | 1.9 /–0.4 | 2.1 /–0.4 | ns, min |

IFF = Input Flip-Flop or Latch

**Notes:**

1. Set-up time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
2. DLL output jitter is already included in the timing calculation.
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

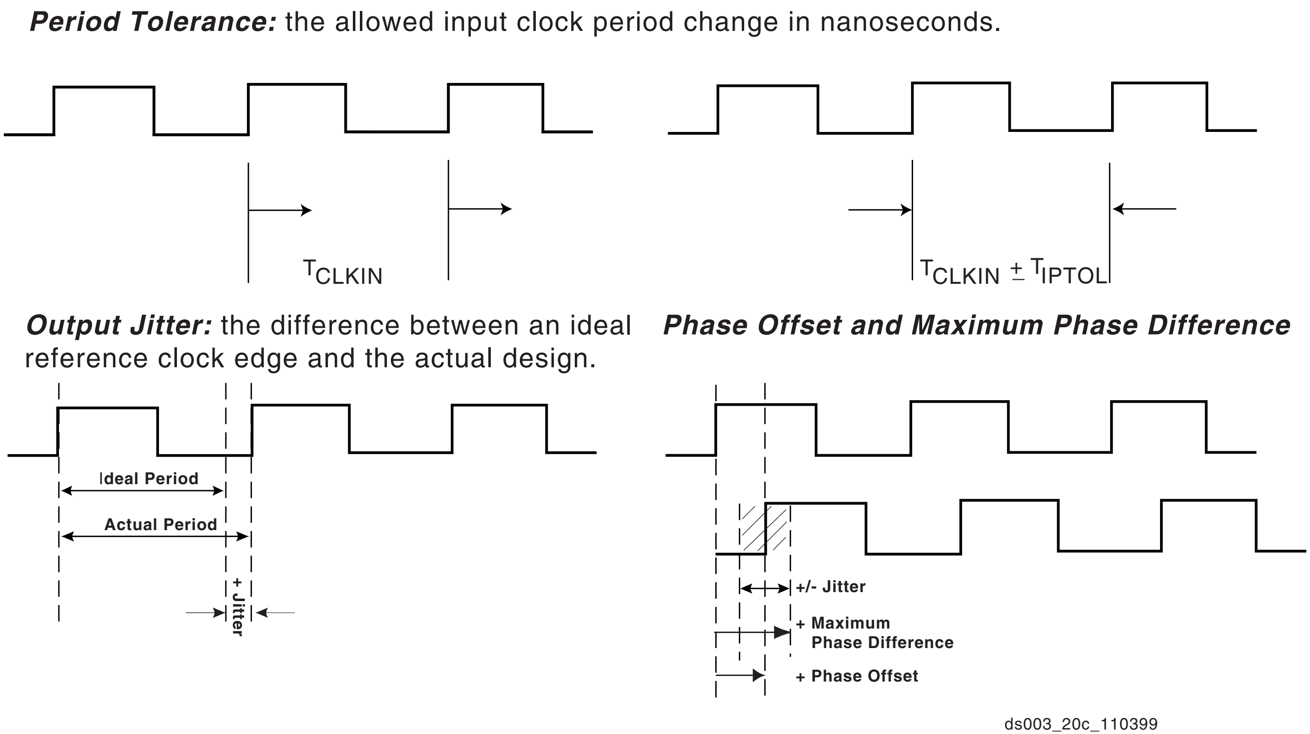


*Figure 1:* **Frequency Tolerance and Clock Jitter**

## Revision History

| Date | Version | Revision |
|---|---|---|
| 11/98 | 1.0 | Initial Xilinx release. |
| 01/99 | 1.2 | Updated package drawings and specs. |
| 02/99 | 1.3 | Update of package drawings, updated specifications. |
| 05/99 | 1.4 | Addition of package drawings and specifications. |
| 05/99 | 1.5 | Replaced FG 676 & FG680 package drawings. |
| 07/99 | 1.6 | Changed Boundary Scan Information and changed Figure 11, Boundary Scan Bit Sequence. Updated IOB Input & Output delays. Added Capacitance info for different I/O Standards. Added 5 V tolerant information. Added DLL Parameters and waveforms and new Pin-to-pin Input and Output Parameter tables for Global Clock Input to Output and Setup and Hold. Changed Configuration Information including Figures 12, 14, 17 & 19. Added device-dependent listings for quiescent currents ICCINTQ and ICCOQ. Updated IOB Input and Output Delays based on default standard of LVTTL, 12 mA, Fast Slew Rate. Added IOB Input Switching Characteristics Standard Adjustments. |
| 09/99 | 1.7 | Speed grade update to preliminary status, Power-on specification and Clock-to-Out Minimums additions, "0" hold time listing explanation, quiescent current listing update, and Figure 6 ADDRA input label correction. Added $T_{IJITCC}$ parameter, changed $T_{OJIT}$ to $T_{OPHASE}$. |
| 01/00 | 1.8 | Update to speed.txt file 1.96. Corrections for CRs 111036,111137, 112697, 115479, 117153, 117154, and 117612. Modified notes for Recommended Operating Conditions (voltage and temperature). Changed Bank information for $V_{CCO}$ in CS144 package on p.43. |

*Table 3:* **Virtex Pinout Tables (BGA)** ***(Continued)***

| Pin Name | Device | BG256 | BG352 | BG432 | BG560 |
|---|---|---|---|---|---|
| $V_{REF}$, Bank 7<br>($V_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)<br>Within each bank, if input reference voltage is not required, all $V_{REF}$ pins are general I/O. | XCV50 | G3, H1 | N/A | N/A | N/A |
| | XCV100/150 | ... + D1 | D26, G26, L26 | N/A | N/A |
| | XCV200/300 | ... + B2 | ... + E24 | F28, F31, J30, N30 | N/A |
| | XCV400 | N/A | N/A | ... + R31 | E31, G31, K31, P31, T31 |
| | XCV600 | N/A | N/A | ... + J28 | ... + H32 |
| | XCV800 | N/A | N/A | ... + M28 | ... + L33 |
| | XCV1000 | N/A | N/A | N/A | ... + D31 |
| GND | All | C3, C18, D4, D5, D9, D10, D11, D12, D16, D17, E4, E17, J4, J17, K4, K17, L4, L17, M4, M17, T4, T17, U4, U5, U9, U10, U11, U12, U16, U17, V3, V18 | A1, A2, A5, A8, A14, A19, A22, A25, A26, B1, B26, E1, E26, H1, H26, N1, P26, W1, W26, AB1, AB26, AE1, AE26, AF1, AF2, AF5, AF8, AF13, AF19, AF22, AF25, AF26 | A2, A3, A7, A9, A14, A18, A23, A25, A29, A30, B1, B2, B30, B31, C1, C31, D16, G1, G31, J1, J31, P1, P31, T4, T28, V1, V31, AC1, AC31, AE1, AE31, AH16, AJ1, AJ31, AK1, AK2, AK30, AK31, AL2, AL3, AL7, AL9 AL14, AL18 AL23, AL25, AL29, AL30 | A1, A7, A12, A14, A18, A20, A24, A29, A32, A33, B1, B6, B9, B15, B23, B27, B31, C2, E1, F32, G2, G33, J32, K1, L2, M33, P1, P33, R32, T1, V33, W2, Y1, Y33, AB1, AC32, AD33, AE2, AG1, AG32, AH2, AJ33, AL32, AM3, AM7, AM11, AM19, AM25, AM28, AM33, AN1, AN2, AN5, AN10, AN14, AN16, AN20, AN22, AN27, AN33 |
| GND(1) | All | J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12 | N/A | N/A | N/A |
| No Connect | All | N/A | N/A | N/A | C31, AC2, AK4, AL3 |

**Notes:**
1. 16 extra balls (grounded) at package center.

*Table 4:* **Virtex Pinout Tables (Fine-Pitch BGA)** ***(Continued)***

| Pin Name | Device | FG256 | FG456 | FG676 | FG680 |
|---|---|---|---|---|---|
| $V_{REF}$, Bank 4 (${V_{REF}}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all $V_{REF}$ pins are general I/O. | XCV50 | P9, T12 | N/A | N/A | N/A |
| | XCV100/150 | ... + T11 | AA13, AB16, AB19 | N/A | N/A |
| | XCV200/300 | ... + R13 | ... + AB20 | N/A | N/A |
| | XCV400 | N/A | N/A | AC15, AD18, AD21, AD22, AF15 | N/A |
| | XCV600 | N/A | N/A | ... + AF20 | AT19, AU7, AU17, AV8, AV10, AW11 |
| | XCV800 | N/A | N/A | ... + AF17 | ... + AV14 |
| | XCV1000 | N/A | N/A | N/A | ... + AU6 |
| $V_{REF}$, Bank 5 ($V_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all $V_{REF}$ pins are general I/O. | XCV50 | T4, P8 | N/A | N/A | N/A |
| | XCV100/150 | ... + R5 | W8, Y10, AA5 | N/A | N/A |
| | XCV200/300 | ... + T2 | ... + Y6 | N/A | N/A |
| | XCV400 | N/A | N/A | AA10, AB8, AB12, AC7, AF12 | N/A |
| | XCV600 | N/A | N/A | ... + AF8 | AT27, AU29, AU31, AV35, AW21, AW23 |
| | XCV800 | N/A | N/A | ... + AE10 | ... + AT25 |
| | XCV1000 | N/A | N/A | N/A | ... + AV36 |
| $V_{REF}$, Bank 6 ($V_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all $V_{REF}$ pins are general I/O. | XCV50 | J3, N1 | N/A | N/A | N/A |
| | XCV100/150 | ... + M1 | N2, R4, T3 | N/A | N/A |
| | XCV200/300 | ... + N2 | ... + Y1 | N/A | N/A |
| | XCV400 | N/A | N/A | AB3, R1, R4, U6, V5 | N/A |
| | XCV600 | N/A | N/A | ... + Y1 | AB35, AD37, AH39, AK39, AM39, AN36 |
| | XCV800 | N/A | N/A | ... + U2 | ... + AE39 |
| | XCV1000 | N/A | N/A | N/A | ... + AT39 |

*Table 4:* **Virtex Pinout Tables (Fine-Pitch BGA) *(Continued)***

| Pin Name | Device | FG256 | FG456 | FG676 | FG680 |
|---|---|---|---|---|---|
| $V_{REF}$, Bank 7<br>($V_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)<br>Within each bank, if input reference voltage is not required, all $V_{REF}$ pins are general I/O. | XCV50 | C1, H3 | N/A | N/A | N/A |
| | XCV100/150 | ... + D1 | E2, H4, K3 | N/A | N/A |
| | XCV200/300 | ... + B1 | ... + D2 | N/A | N/A |
| | XCV400 | N/A | N/A | F4, G4, K6, M2, M5 | N/A |
| | XCV600 | N/A | N/A | ... + H1 | E38, G38, L36, N36, U36, U38 |
| | XCV800 | N/A | N/A | ... + K1 | ... + N38 |
| | XCV1000 | N/A | N/A | N/A | ... + F36 |
| GND | All | A1, A16, B2, B15, F6, F7, F10, F11, G6, G7, G8, G9, G10, G11, H7, H8, H9, H10, J7, J8, J9, J10, K6, K7, K8, K9, K10, K11, L6, L7, L10, L11, R2, R15, T1, T16 | A1, A22, B2, B21, C3, C20, J9, J10, J11, J12, J13, J14, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N9, N10, N11, N12, N13, N14, P9, P10, P11, P12, P13, P14, Y3, Y20, AA2, AA21, AB1, AB22 | A1, A26, B2, B9, B14, B18, B25, C3, C24, D4, D23, E5, E22, J2, J25, K10, K11, K12, K13, K14, K15, K16, K17, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N2, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, P25, R10, R11, R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17, V2, V25, AB5, AB22, AC4, AC23, AD3, AD24, AE2, AE9, AE13, AE18, AE25, AF1, AF26 | A1, A2, A3, A37, A38, A39, AA5, AA35, AH4, AH5, AH35, AH36, AR5, AR12, AR19, AR20, AR21, AR28, AR35, AT4, AT12, AT20, AT28, AT36, AU1, AU3, AU20, AU37, AU39, AV1, AV2, AV38, AV39, AW1, AW2, AW3, AW37, AW38, AW39, B1, B2, B38, B39, C1, C3, C20, C37, C39, D4, D12, D20, D28, D36, E5, E12, E19, E20, E21, E28, E35, M4, M5, M35, M36, W5, W35, Y3, Y4, Y5, Y35, Y36, Y37 |

*Table 4:* **Virtex Pinout Tables (Fine-Pitch BGA) *(Continued)***

| Pin Name | Device | FG256 | FG456 | FG676 | FG680 |
|---|---|---|---|---|---|
| No Connect<br>(No-connect pins are listed incrementally. All pins listed for both the required device and all larger devices listed in the same package are no connects.) | XCV800 | N/A | N/A | A2, A3, A15, A25, B1, B6, B11, B16, B21, B24, B26, C1, C2, C25, C26, F2, F6, F21, F25, L2, L25, N25, P2, T2, T25, AA2, AA6, AA21, AA25, AD1, AD2, AD25, AE1, AE3, AE6, AE11, AE14, AE16, AE21, AE24, AE26, AF2, AF24, AF25 | N/A |
| | XCV600 | N/A | N/A | same as above | N/A |
| | XCV400 | N/A | N/A | ... + A9, A10, A13, A16, A24, AC1, AC25, AE12, AE15, AF3, AF10, AF11, AF13, AF14, AF16, AF18, AF23, B4, B12, B13, B15, B17, D1, D25, H26, J1, K26, L1, M1, M25, N1, N26, P1, P26, R2, R26, T1, T26, U26, V1 | N/A |
| | XCV300 | N/A | D4, D19, W4, W19 | N/A | N/A |
| | XCV200 | N/A | ... + A2, A6, A12, B11, B16, C2, D1, D18, E17, E19, G2, G22, L2, L19, M2, M21, R3, R20, U3, U18, Y22, AA1, AA3, AA11, AA16, AB7, AB12, AB21, | N/A | N/A |
| | XCV150 | N/A | ... + A13, A14, C8, C9, E13, F11, H21, J1, J4, K2, K18, K19, M17, N1, P1, P5, P22, R22, W13, W15, AA9, AA10, AB8, AB14 | N/A | N/A |

## TQ144 Pin Function Diagram

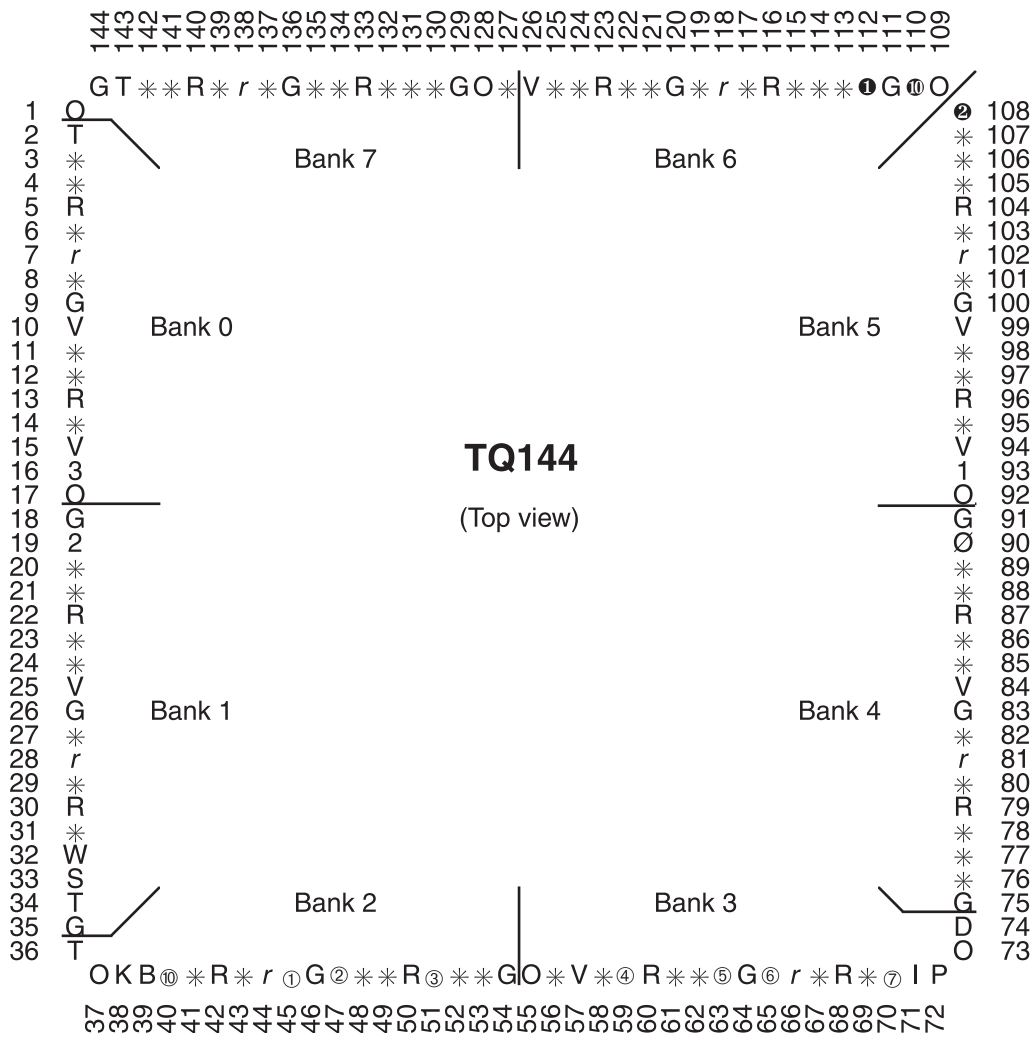


*Figure 2:* **TQ144 Pin Function Diagram**

## PQ240/HQ240 Pin Function Diagram

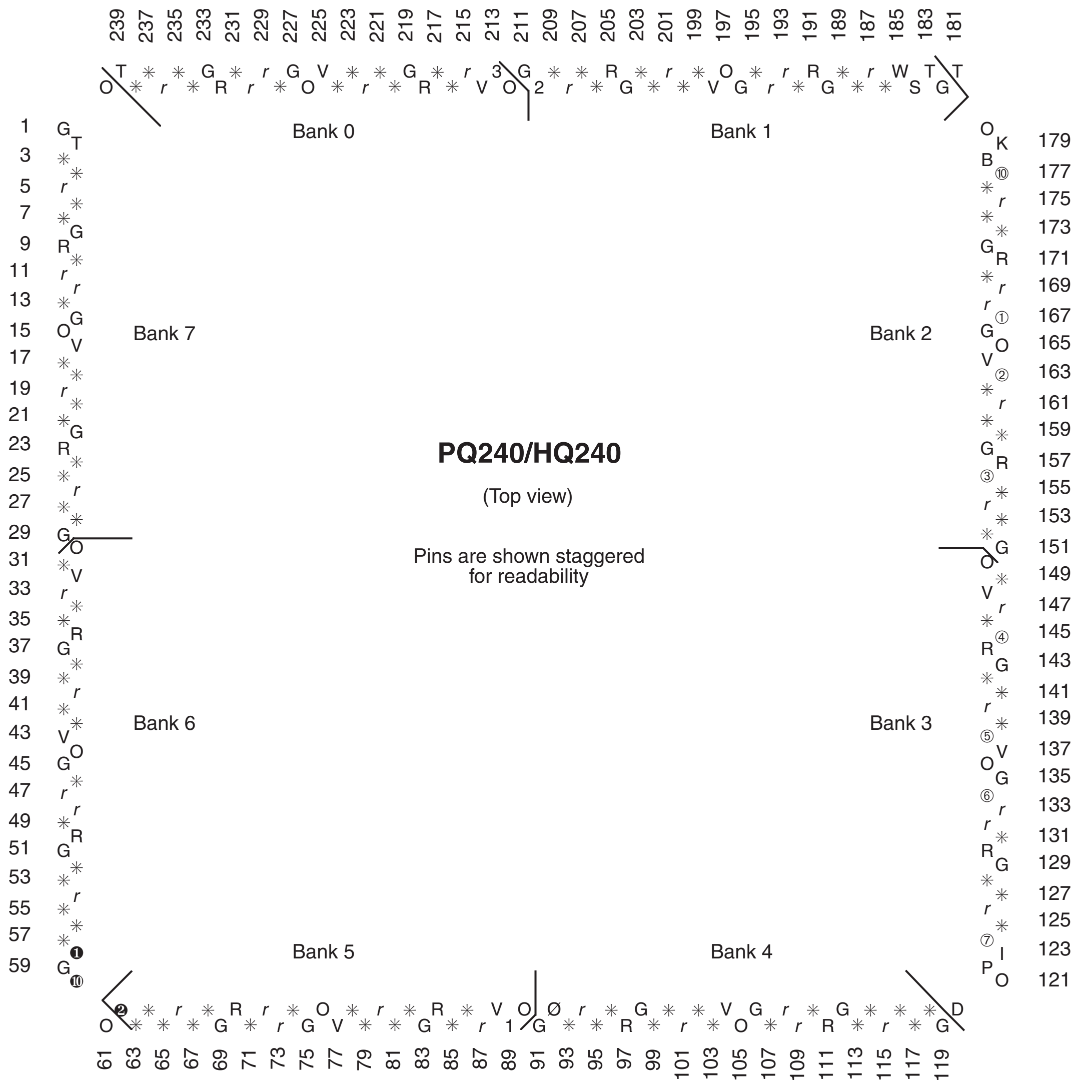


*Figure 3:* **PQ240/HQ240 Pin Function Diagram**