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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	864
Number of Logic Elements/Cells	3888
Total RAM Bits	49152
Number of I/O	260
Number of Gates	164674
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv150-6fg456c

Virtex Device/Package Combinations and Maximum I/O

Table 3: Virtex Family Maximum User I/O by Device/Package (Excluding Dedicated Clock Pins)

Package	XCV50	XCV100	XCV150	XCV200	XCV300	XCV400	XCV600	XCV800	XCV1000
CS144	94	94							
TQ144	98	98							
PQ240	166	166	166	166	166				
HQ240						166	166	166	
BG256	180	180	180	180					
BG352			260	260	260				
BG432					316	316	316	316	
BG560						404	404	404	404
FG256	176	176	176	176					
FG456			260	284	312				
FG676						404	444	444	
FG680							512	512	512

Virtex Ordering Information

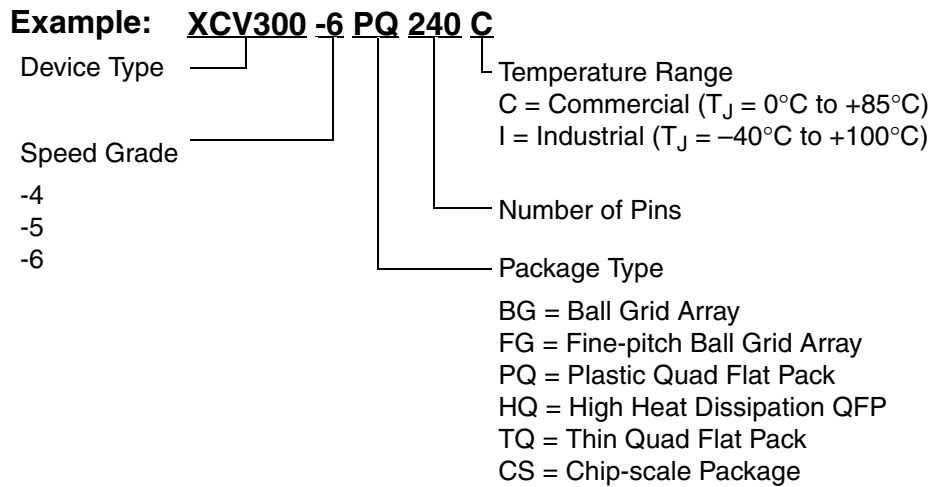


Figure 1: Virtex Ordering Information

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is

selected either from these pads or from signals in the general purpose routing.

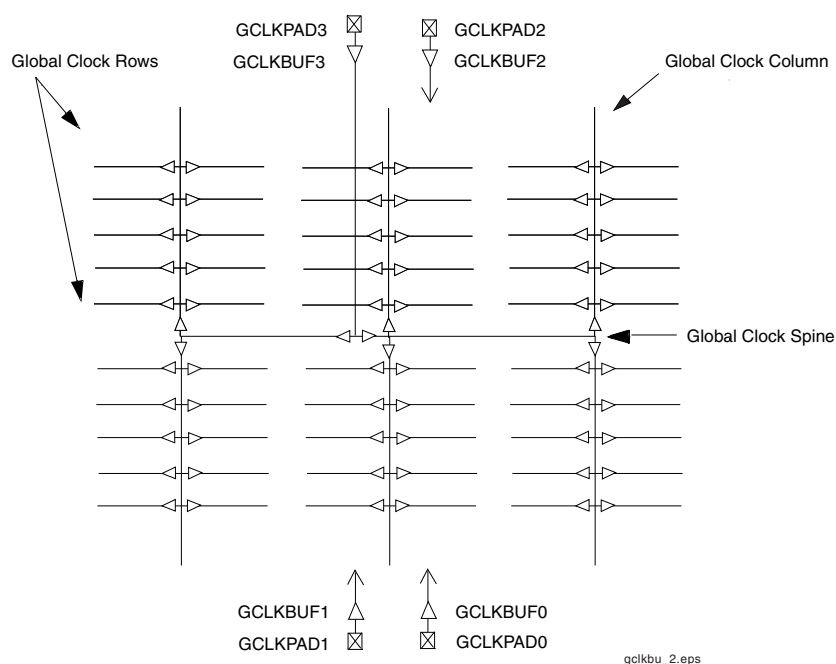


Figure 9: Global Clock Distribution Network

Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Clock edges reach internal flip-flops one to four clock periods after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to de-skew a board level clock among multiple Virtex devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

See **DLL Timing Parameters**, page 21 of Module 3, for frequency range information.

Boundary Scan

Virtex devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, and HIGHZ instructions. The TAP also supports two internal scan chains and configuration/readback of the device. The TAP uses dedicated package pins that always operate using LVTTTL. For TDO to operate using LVTTTL, the V_{CCO} for Bank 2 should be 3.3 V. Otherwise, TDO switches rail-to-rail between ground and V_{CCO} .

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including un-bonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections, provided the user design or application is turned off.

Table 5 lists the boundary-scan instructions supported in Virtex FPGAs. Internal signals can be captured during EXTEST by connecting them to un-bonded or unused IOBs. They can also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Before the device is configured, all instructions except USER1 and USER2 are available. After configuration, all instructions are available. During configuration, it is recommended that those operations using the boundary-scan register (SAMPLE/PRELOAD, INTEST, EXTEST) not be performed.

Configuration

Virtex devices are configured by loading configuration data into the internal configuration memory. Some of the pins used for this are dedicated configuration pins, while others can be re-used as general purpose inputs and outputs once configuration is complete.

The following are dedicated pins:

- Mode pins (M2, M1, M0)
- Configuration clock pin (CCLK)
- $\overline{\text{PROGRAM}}$ pin
- DONE pin
- Boundary-scan pins (TDI, TDO, TMS, TCK)

Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or it can be generated externally and provided to the FPGA as an input. The $\overline{\text{PROGRAM}}$ pin must be pulled High prior to reconfiguration.

Note that some configuration pins can act as outputs. For correct operation, these pins can require a V_{CCO} of 3.3 V to permit LVTTTL operation. All the pins affected are in banks 2 or 3. The configuration pins needed for SelectMap (CS, Write) are located in bank 1.

Table 7: Configuration Codes

Configuration Mode	M2	M1	M0	CCLK Direction	Data Width	Serial D _{out}	Configuration Pull-ups
Master-serial mode	0	0	0	Out	1	Yes	No
Boundary-scan mode	1	0	1	N/A	1	No	No
SelectMAP mode	1	1	0	In	8	No	No
Slave-serial mode	1	1	1	In	1	Yes	No
Master-serial mode	1	0	0	Out	1	Yes	Yes
Boundary-scan mode	0	0	1	N/A	1	No	Yes
SelectMAP mode	0	1	0	In	8	No	Yes
Slave-serial mode	0	1	1	In	1	Yes	Yes

Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other source of serial configuration data. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

For more information on serial PROMs, see the PROM data sheet at:

<http://www.xilinx.com/bvdocs/publications/ds026.pdf>.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin. The data on the DOUT pin changes on the rising edge of CCLK.

The change of DOUT on the rising edge of CCLK differs from previous families, but does not cause a problem for

After Virtex devices are configured, unused IOBs function as 3-state OBUFTs with weak pull downs. For a more detailed description than that given below, see the XAPP138, Virtex Configuration and Readback.

Configuration Modes

Virtex supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- SelectMAP mode
- Boundary-scan mode

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in Table 7.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected. However, it is recommended to drive the configuration mode pins externally.

mixed configuration chains. This change was made to improve serial configuration rates for Virtex-only chains.

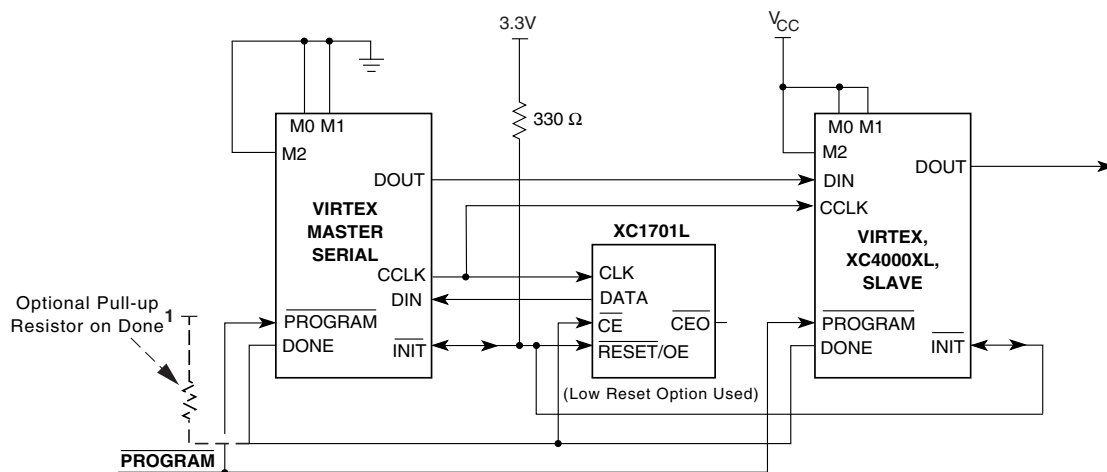
Figure 12 shows a full master/slave system. A Virtex device in slave-serial mode should be connected as shown in the third device from the left.

Slave-serial mode is selected by applying <111> or <011> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave-serial the default mode if the pins are left unconnected. However, it is recommended to drive the configuration mode pins externally. Figure 13 shows slave-serial mode programming switching characteristics.

Table 8 provides more detail about the characteristics shown in Figure 13. Configuration must be delayed until the $\overline{\text{INIT}}$ pins of all daisy-chained FPGAs are High.

Table 8: Master/Slave Serial Mode Programming Switching

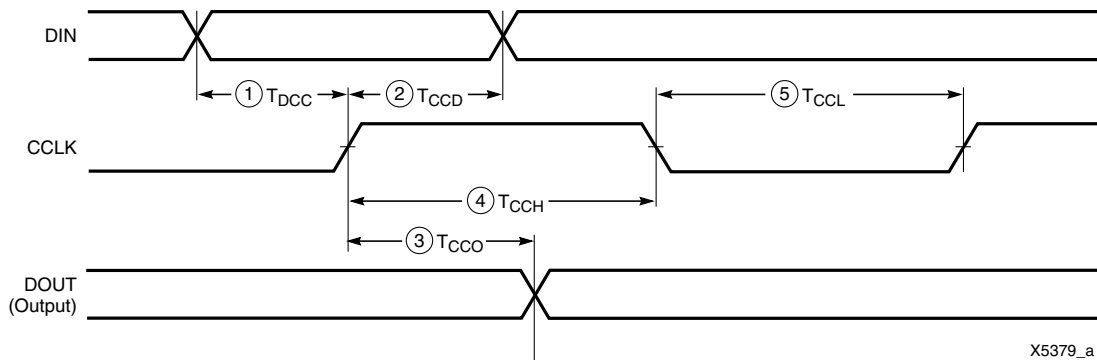
	Description	Figure References	Symbol	Values	Units
CCLK	DIN setup/hold, slave mode	1/2	T_{DCC}/T_{CCD}	5.0 / 0	ns, min
	DIN setup/hold, master mode	1/2	T_{DSCK}/T_{CKDS}	5.0 / 0	ns, min
	DOUT	3	T_{CCO}	12.0	ns, max
	High time	4	T_{CCH}	5.0	ns, min
	Low time	5	T_{CCL}	5.0	ns, min
	Maximum Frequency		F_{CC}	66	MHz, max
	Frequency Tolerance, master mode with respect to nominal			+45% -30%	



Note 1: If none of the Virtex FPGAs have been selected to drive DONE, an external pull-up resistor of 330 Ω should be added to the common DONE line. (For Spartan-XL devices, add a 4.7K Ω pull-up resistor.) This pull-up is not needed if the DriveDONE attribute is set. If used, DriveDONE should be selected only for the last device in the configuration chain.

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Figure 12: Master/Slave Serial Mode Circuit Diagram



X5379_a

Figure 13: Slave-Serial Mode Programming Switching Characteristics

Master-Serial Mode

In master-serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM that feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge.

The interface is identical to slave-serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration. Switching to a lower frequency is prohibited.

The CCLK frequency is set using the ConfigRate option in the bitstream generation software. The maximum CCLK frequency that can be selected is 60 MHz. When selecting a CCLK frequency, ensure that the serial PROM and any

daisy-chained FPGAs are fast enough to support the clock rate.

On power-up, the CCLK frequency is 2.5 MHz. This frequency is used until the ConfigRate bits have been loaded when the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz.

Figure 12 shows a full master/slave system. In this system, the left-most device operates in master-serial mode. The remaining devices operate in slave-serial mode. The SPROM $\overline{\text{RESET}}$ pin is driven by $\overline{\text{INIT}}$, and the $\overline{\text{CE}}$ input is driven by DONE. There is the potential for contention on the DONE pin, depending on the start-up sequence options chosen.

Figure 14 shows the timing of master-serial configuration. Master-serial mode is selected by a <000> or <100> on the mode pins (M2, M1, M0). Table 8 shows the timing information for Figure 14.

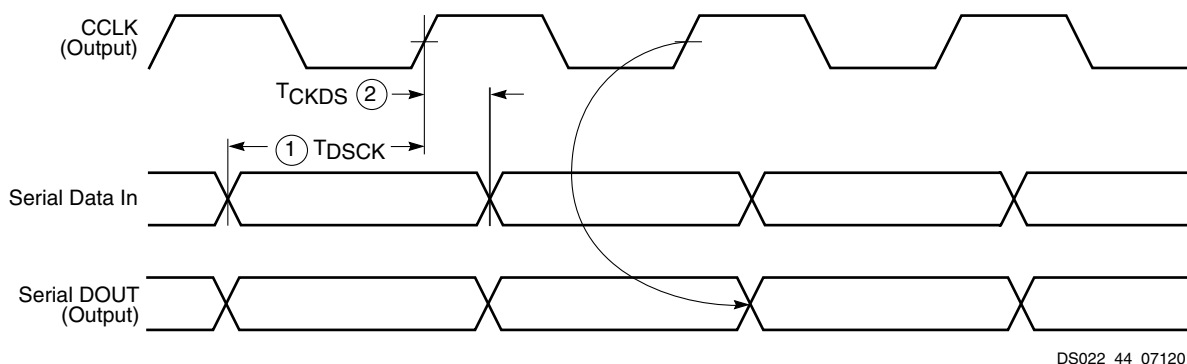


Figure 14: Master-Serial Mode Programming Switching Characteristics

At power-up, V_{CC} must rise from 1.0 V to V_{CC} min in less than 50 ms, otherwise delay configuration by pulling $\overline{\text{PROGRAM}}$ Low until V_{CC} is valid.

The sequence of operations necessary to configure a Virtex FPGA serially appears in Figure 15.

SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the FPGA with a $\overline{\text{BUSY}}$ flag controlling the flow of data.

An external data source provides a byte stream, CCLK, a Chip Select ($\overline{\text{CS}}$) signal and a Write signal ($\overline{\text{WRITE}}$). If $\overline{\text{BUSY}}$ is asserted (High) by the FPGA, the data must be held until $\overline{\text{BUSY}}$ goes Low.

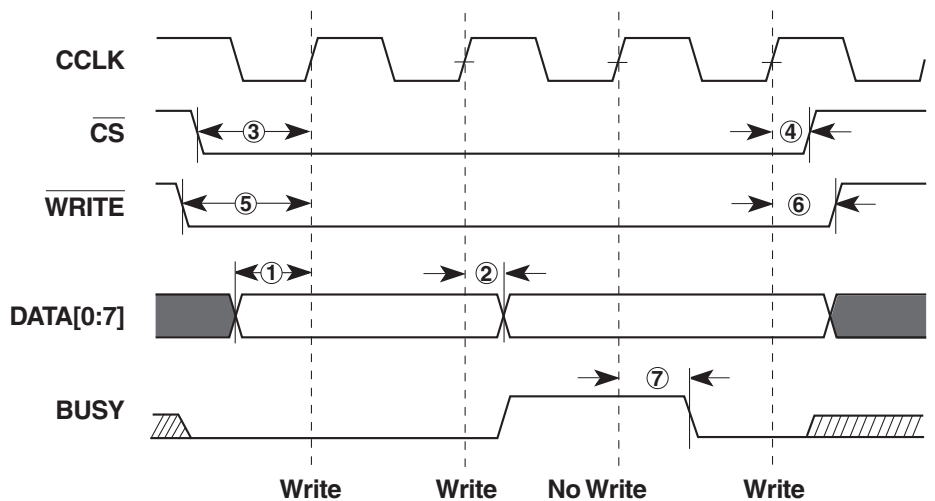
Data can also be read using the SelectMAP mode. If $\overline{\text{WRITE}}$ is not asserted, configuration data is read out of the FPGA as part of a readback operation.

In the SelectMAP mode, multiple Virtex devices can be chained in parallel. DATA pins (D7:D0), CCLK, $\overline{\text{WRITE}}$, $\overline{\text{BUSY}}$, $\overline{\text{PROGRAM}}$, DONE, and $\overline{\text{INIT}}$ can be connected in parallel between all the FPGAs. Note that the data is organized with the MSB of each byte on pin D0 and the LSB of each byte on D7. The $\overline{\text{CS}}$ pins are kept separate, insuring that each FPGA can be selected individually. $\overline{\text{WRITE}}$ should be Low before loading the first bitstream and returned High after the last device has been programmed. Use $\overline{\text{CS}}$ to select the appropriate FPGA for loading the bitstream and sending the configuration data. At the end of the bitstream, deselect the loaded device and select the next target FPGA by setting its $\overline{\text{CS}}$ pin High. A free-running oscillator or other externally generated signal can be used for CCLK. The $\overline{\text{BUSY}}$ signal can be ignored for frequencies below 50 MHz. For details about frequencies above 50 MHz, see XAPP138, Virtex Configuration and Readback. Once all the devices have been programmed, the DONE pin goes High.

3. At the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this has happened.
4. Repeat steps 2 and 3 until all the data has been sent.

5. De-assert $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$.

A flowchart for the write operation appears in [Figure 17](#). Note that if CCLK is slower than f_{CCNH} , the FPGA never asserts BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.



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Figure 16: Write Operations

Data Stream Format

Virtex devices are configured by sequentially loading frames of data. **Table 11** lists the total number of bits required to configure each device. For more detailed information, see application note XAPP151 “Virtex Configuration Architecture Advanced Users Guide”.

Table 11: Virtex Bit-Stream Lengths

Device	# of Configuration Bits
XCV50	559,200
XCV100	781,216
XCV150	1,040,096
XCV200	1,335,840
XCV300	1,751,808
XCV400	2,546,048
XCV600	3,607,968
XCV800	4,715,616
XCV1000	6,127,744

Readback

The configuration data stored in the Virtex configuration memory can be readback for verification. Along with the configuration data it is possible to readback the contents all flip-flops/latches, LUTRAMs, and block RAMs. This capability is used for real-time debugging.

For more detailed information, see Application Note XAPP138: *Virtex FPGA Series Configuration and Readback*, available online at www.xilinx.com.

Revision History

Date	Version	Revision
11/98	1.0	Initial Xilinx release.
01/99	1.2	Updated package drawings and specs.
02/99	1.3	Update of package drawings, updated specifications.
05/99	1.4	Addition of package drawings and specifications.
05/99	1.5	Replaced FG 676 & FG680 package drawings.
07/99	1.6	Changed Boundary Scan Information and changed Figure 11, Boundary Scan Bit Sequence. Updated IOB Input & Output delays. Added Capacitance info for different I/O Standards. Added 5 V tolerant information. Added DLL Parameters and waveforms and new Pin-to-pin Input and Output Parameter tables for Global Clock Input to Output and Setup and Hold. Changed Configuration Information including Figures 12, 14, 17 & 19. Added device-dependent listings for quiescent currents ICCINTQ and ICCOQ. Updated IOB Input and Output Delays based on default standard of LVTTTL, 12 mA, Fast Slew Rate. Added IOB Input Switching Characteristics Standard Adjustments.
09/99	1.7	Speed grade update to preliminary status, Power-on specification and Clock-to-Out Minimums additions, “0” hold time listing explanation, quiescent current listing update, and Figure 6 ADDRA input label correction. Added T _{IJITCC} parameter, changed T _{OJIT} to T _{OPHASE} .
01/00	1.8	Update to speed.txt file 1.96. Corrections for CRs 111036, 111137, 112697, 115479, 117153, 117154, and 117612. Modified notes for Recommended Operating Conditions (voltage and temperature). Changed Bank information for V _{CCO} in CS144 package on p.43.



Virtex™ 2.5 V Field Programmable Gate Arrays

DS003-3 (v4.0) March 1, 2013

Production Product Specification

Virtex Electrical Characteristics

Definition of Terms

Electrical and switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. Contact the factory for design considerations requiring more detailed information.

Table 1 correlates the current status of each Virtex device with a corresponding speed file designation.

Table 1: Virtex Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XCV50			–6, –5, –4
XCV100			–6, –5, –4
XCV150			–6, –5, –4
XCV200			–6, –5, –4
XCV300			–6, –5, –4
XCV400			–6, –5, –4
XCV600			–6, –5, –4
XCV800			–6, –5, –4
XCV1000			–6, –5, –4

All specifications are subject to change without notice.

DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Device	Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage (below which configuration data can be lost)	All	2.0		V
V_{DRIO}	Data Retention V_{CCO} Voltage (below which configuration data can be lost)	All	1.2		V
I_{CCINTQ}	Quiescent V_{CCINT} supply current ^(1,3)	XCV50		50	mA
		XCV100		50	mA
		XCV150		50	mA
		XCV200		75	mA
		XCV300		75	mA
		XCV400		75	mA
		XCV600		100	mA
		XCV800		100	mA
		XCV1000		100	mA
I_{CCOQ}	Quiescent V_{CCO} supply current ⁽¹⁾	XCV50		2	mA
		XCV100		2	mA
		XCV150		2	mA
		XCV200		2	mA
		XCV300		2	mA
		XCV400		2	mA
		XCV600		2	mA
		XCV800		2	mA
		XCV1000		2	mA
I_{REF}	V_{REF} current per V_{REF} pin	All		20	μ A
I_L	Input or output leakage current	All	-10	+10	μ A
C_{IN}	Input capacitance (sample tested)	BGA, PQ, HQ, packages		8	pF
I_{RPU}	Pad pull-up (when selected) @ $V_{in} = 0$ V, $V_{CCO} = 3.3$ V (sample tested)	All	Note (2)	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ $V_{in} = 3.6$ V (sample tested)		Note (2)	0.15	mA

Notes:

1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.
3. Multiply I_{CCINTQ} limit by two for industrial grade.

Virtex Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL

Description	Symbol	Device	Speed Grade				Units
			Min	-6	-5	-4	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, <i>with</i> DLL. For data <i>output</i> with different standards, adjust delays with the values shown in Output Delay Adjustments.	T _{ICKOFDLL}	XCV50	1.0	3.1	3.3	3.6	ns, max
		XCV100	1.0	3.1	3.3	3.6	ns, max
		XCV150	1.0	3.1	3.3	3.6	ns, max
		XCV200	1.0	3.1	3.3	3.6	ns, max
		XCV300	1.0	3.1	3.3	3.6	ns, max
		XCV400	1.0	3.1	3.3	3.6	ns, max
		XCV600	1.0	3.1	3.3	3.6	ns, max
		XCV800	1.0	3.1	3.3	3.6	ns, max
		XCV1000	1.0	3.1	3.3	3.6	ns, max

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see [Table 2](#) and [Table 3](#).
3. DLL output jitter is already included in the timing calculation.

Global Clock Input-to-Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL

Description	Symbol	Device	Speed Grade				Units
			Min	-6	-5	-4	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, <i>without</i> DLL. For data <i>output</i> with different standards, adjust delays with the values shown in Input and Output Delay Adjustments. For I/O standards requiring V _{REF} such as GTL, GTL+, SSTL, HSTL, CTT, and AGO, an additional 600 ps must be added.	T _{ICKOF}	XCV50	1.5	4.6	5.1	5.7	ns, max
		XCV100	1.5	4.6	5.1	5.7	ns, max
		XCV150	1.5	4.7	5.2	5.8	ns, max
		XCV200	1.5	4.7	5.2	5.8	ns, max
		XCV300	1.5	4.7	5.2	5.9	ns, max
		XCV400	1.5	4.8	5.3	6.0	ns, max
		XCV600	1.6	4.9	5.4	6.0	ns, max
		XCV800	1.6	4.9	5.5	6.2	ns, max
		XCV1000	1.7	5.0	5.6	6.3	ns, max

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see [Table 2](#) and [Table 3](#).

Minimum Clock-to-Out for Virtex Devices

I/O Standard	With DLL	Without DLL									
	All Devices	V50	V100	V150	V200	V300	V400	V600	V800	V1000	Units
*LVTTTL_S2	5.2	6.0	6.0	6.0	6.0	6.1	6.1	6.1	6.1	6.1	ns
*LVTTTL_S4	3.5	4.3	4.3	4.3	4.3	4.4	4.4	4.4	4.4	4.4	ns
*LVTTTL_S6	2.8	3.6	3.6	3.6	3.6	3.7	3.7	3.7	3.7	3.7	ns
*LVTTTL_S8	2.2	3.1	3.1	3.1	3.1	3.1	3.1	3.2	3.2	3.2	ns
*LVTTTL_S12	2.0	2.9	2.9	2.9	2.9	2.9	2.9	3.0	3.0	3.0	ns
*LVTTTL_S16	1.9	2.8	2.8	2.8	2.8	2.8	2.8	2.9	2.9	2.9	ns
*LVTTTL_S24	1.8	2.6	2.6	2.7	2.7	2.7	2.7	2.7	2.7	2.8	ns
*LVTTTL_F2	2.9	3.8	3.8	3.8	3.8	3.8	3.8	3.9	3.9	3.9	ns
*LVTTTL_F4	1.7	2.6	2.6	2.6	2.6	2.6	2.6	2.7	2.7	2.7	ns
*LVTTTL_F6	1.2	2.0	2.0	2.0	2.1	2.1	2.1	2.1	2.1	2.2	ns
*LVTTTL_F8	1.1	1.9	1.9	1.9	1.9	2.0	2.0	2.0	2.0	2.0	ns
*LVTTTL_F12	1.0	1.8	1.8	1.8	1.8	1.9	1.9	1.9	1.9	1.9	ns
*LVTTTL_F16	0.9	1.7	1.8	1.8	1.8	1.8	1.8	1.8	1.9	1.9	ns
*LVTTTL_F24	0.9	1.7	1.7	1.7	1.8	1.8	1.8	1.8	1.8	1.9	ns
LVCMS2	1.1	1.9	1.9	1.9	2.0	2.0	2.0	2.0	2.0	2.1	ns
PCI33_3	1.5	2.4	2.4	2.4	2.4	2.4	2.4	2.5	2.5	2.5	ns
PCI33_5	1.4	2.2	2.2	2.3	2.3	2.3	2.3	2.3	2.3	2.4	ns
PCI66_3	1.1	1.9	1.9	2.0	2.0	2.0	2.0	2.0	2.1	2.1	ns
GTL	1.6	2.5	2.5	2.5	2.5	2.5	2.5	2.6	2.6	2.6	ns
GTL+	1.7	2.5	2.5	2.6	2.6	2.6	2.6	2.6	2.6	2.7	ns
HSTL I	1.1	1.9	1.9	1.9	1.9	2.0	2.0	2.0	2.0	2.0	ns
HSTL III	0.9	1.7	1.7	1.8	1.8	1.8	1.8	1.8	1.8	1.9	ns
HSTL IV	0.8	1.6	1.6	1.6	1.7	1.7	1.7	1.7	1.7	1.8	ns
SSTL2 I	0.9	1.7	1.7	1.7	1.7	1.8	1.8	1.8	1.8	1.8	ns
SSTL2 II	0.8	1.6	1.6	1.6	1.6	1.7	1.7	1.7	1.7	1.7	ns
SSTL3 I	0.8	1.6	1.7	1.7	1.7	1.7	1.7	1.7	1.8	1.8	ns
SSTL3 II	0.7	1.5	1.5	1.6	1.6	1.6	1.6	1.6	1.6	1.7	ns
CTT	1.0	1.8	1.8	1.8	1.9	1.9	1.9	1.9	1.9	2.0	ns
AGP	1.0	1.8	1.8	1.9	1.9	1.9	1.9	1.9	1.9	2.0	ns

*S = Slow Slew Rate, F = Fast Slew Rate

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Input and output timing is measured at 1.4 V for LVTTTL. For other I/O standards, see [Table 3](#). In all cases, an 8 pF external capacitive load is used.

Virtex Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Set-Up and Hold for LVTTL Standard, *with DLL*

Description	Symbol	Device	Speed Grade				Units
			Min	-6	-5	-4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in Input Delay Adjustments.							
No Delay Global Clock and IFF, with DLL	T_{PSDLL}/T_{PHDLL}	XCV50	0.40 / -0.4	1.7 / -0.4	1.8 / -0.4	2.1 / -0.4	ns, min
		XCV100	0.40 / -0.4	1.7 / -0.4	1.9 / -0.4	2.1 / -0.4	ns, min
		XCV150	0.40 / -0.4	1.7 / -0.4	1.9 / -0.4	2.1 / -0.4	ns, min
		XCV200	0.40 / -0.4	1.7 / -0.4	1.9 / -0.4	2.1 / -0.4	ns, min
		XCV300	0.40 / -0.4	1.7 / -0.4	1.9 / -0.4	2.1 / -0.4	ns, min
		XCV400	0.40 / -0.4	1.7 / -0.4	1.9 / -0.4	2.1 / -0.4	ns, min
		XCV600	0.40 / -0.4	1.7 / -0.4	1.9 / -0.4	2.1 / -0.4	ns, min
		XCV800	0.40 / -0.4	1.7 / -0.4	1.9 / -0.4	2.1 / -0.4	ns, min
		XCV1000	0.40 / -0.4	1.7 / -0.4	1.9 / -0.4	2.1 / -0.4	ns, min

IFF = Input Flip-Flop or Latch

Notes:

1. Set-up time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
2. DLL output jitter is already included in the timing calculation.
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Date	Version	Revision
01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
03/00	2.0	New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration.
05/00	2.1	Modified "Pins not listed..." statement. Speed grade update to Final status.
05/00	2.2	Modified Table 18.
09/00	2.3	<ul style="list-style-type: none"> Added XCV400 values to table under Minimum Clock-to-Out for Virtex Devices. Corrected Units column in table under IOB Input Switching Characteristics. Added values to table under CLB SelectRAM Switching Characteristics.
10/00	2.4	<ul style="list-style-type: none"> Corrected Pinout information for devices in the BG256, BG432, and BG560 packages in Table 18. Corrected BG256 Pin Function Diagram.
04/02/01	2.5	<ul style="list-style-type: none"> Revised minimums for Global Clock Set-Up and Hold for LVTTTL Standard, with DLL. Converted file to modularized format. See the Virtex Data Sheet section.
04/19/01	2.6	<ul style="list-style-type: none"> Clarified TIOCKP and TIOCKON IOB Output Switching Characteristics descriptors.
07/19/01	2.7	<ul style="list-style-type: none"> Under Absolute Maximum Ratings, changed (T_{SOL}) to 220 °C.
07/26/01	2.8	<ul style="list-style-type: none"> Removed T_{SOL} parameter and added footnote to Absolute Maximum Ratings table.
10/29/01	2.9	<ul style="list-style-type: none"> Updated the speed grade designations used in data sheets, and added Table 1, which shows the current speed grade designation for each device.
02/01/02	3.0	<ul style="list-style-type: none"> Added footnote to DC Input and Output Levels table.
07/19/02	3.1	<ul style="list-style-type: none"> Removed mention of MIL-M-38510/605 specification. Added link to xapp158 from the Power-On Power Supply Requirements section.
09/10/02	3.2	<ul style="list-style-type: none"> Added Clock CLK to IOB Input Switching Characteristics and IOB Output Switching Characteristics.
03/01/13	4.0	The products listed in this data sheet are obsolete. See XCN10016 for further information.

Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

- DS003-1, Virtex 2.5V FPGAs:
Introduction and Ordering Information (Module 1)
- DS003-2, Virtex 2.5V FPGAs:
Functional Description (Module 2)
- DS003-3, Virtex 2.5V FPGAs:
DC and Switching Characteristics (Module 3)
- DS003-4, Virtex 2.5V FPGAs:
Pinout Tables (Module 4)



Virtex™ 2.5 V Field Programmable Gate Arrays

DS003-4 (v4.0) March 1, 2013

Production Product Specification

Virtex Pin Definitions

Table 1: Special Purpose Pins

Pin Name	Dedicated Pin	Direction	Description
GCK0, GCK1, GCK2, GCK3	Yes	Input	Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin: it is an input for SelectMAP and slave-serial modes, and output in master-serial mode. After configuration, it is input only, logic level = Don't Care.
PROGRAM	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output can be open drain.
INIT	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. The pin becomes a user I/O after configuration.
BUSY/ DOUT	No	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration unless the SelectMAP port is retained. In bit-serial modes, DOUT provides header information to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In SelectMAP mode, D0 - D7 are configuration data pins. These pins become user I/Os after configuration unless the SelectMAP port is retained. In bit-serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
WRITE	No	Input	In SelectMAP mode, the active-low Write Enable signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
CS	No	Input	In SelectMAP mode, the active-low Chip Select signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary-scan Test-Access-Port pins, as defined in IEEE 1149.1.
DXN, DXP	Yes	N/A	Temperature-sensing diode pins. (Anode: DXP, cathode: DXN)
V _{CCINT}	Yes	Input	Power-supply pins for the internal core logic.
V _{CCO}	Yes	Input	Power-supply pins for the output drivers (subject to banking rules)
V _{REF}	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground

Table 2: Virtex Pinout Tables (Chip-Scale and QFP Packages) (Continued)

Pin Name	Device	CS144	TQ144	PQ/HQ240
V_{REF} Bank 3 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	H11, K12	60, 68	130, 144
	XCV100/150	... + J10	... + 66	... + 133
	XCV200/300	N/A	N/A	... + 126
	XCV400	N/A	N/A	... + 147
	XCV600	N/A	N/A	... + 132
	XCV800	N/A	N/A	... + 140
V_{REF} Bank 4 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	L8, L10	79, 87	97, 111
	XCV100/150	... + N10	... + 81	... + 108
	XCV200/300	N/A	N/A	... + 115
	XCV400	N/A	N/A	... + 94
	XCV600	N/A	N/A	... + 109
	XCV800	N/A	N/A	... + 101
V_{REF} Bank 5 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	L4, L6	96, 104	70, 84
	XCV100/150	... + N4	... + 102	... + 73
	XCV200/300	N/A	N/A	... + 66
	XCV400	N/A	N/A	... + 87
	XCV600	N/A	N/A	... + 72
	XCV800	N/A	N/A	... + 80

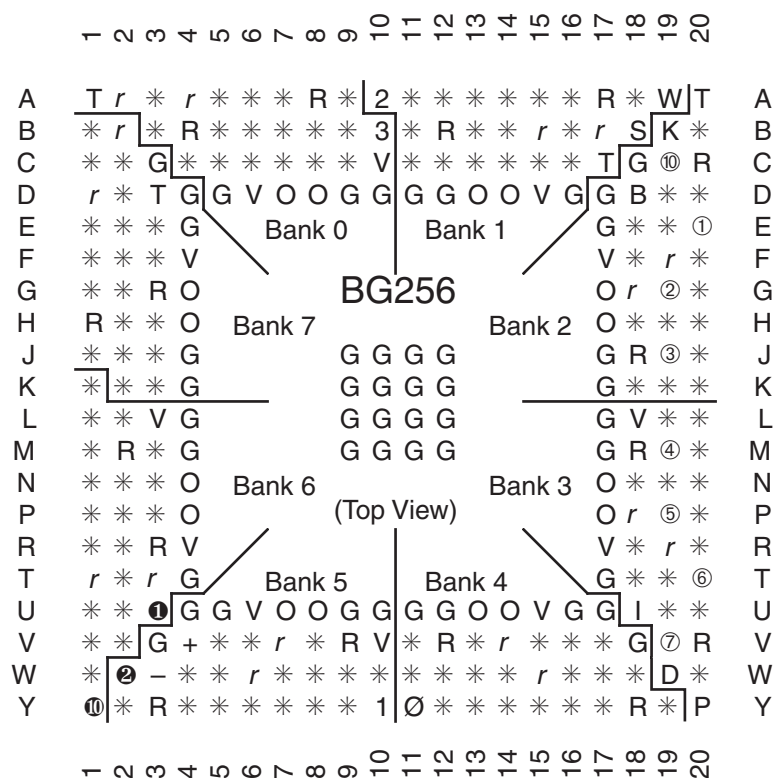
Table 3: Virtex Pinout Tables (BGA) (Continued)

Pin Name	Device	BG256	BG352	BG432	BG560
V_{REF} Bank 3 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	M18, V20	N/A	N/A	N/A
	XCV100/150	... + R19	R4, V4, Y3	N/A	N/A
	XCV200/300	... + P18	... + AC2	V2, AB4, AD4, AF3	N/A
	XCV400	N/A	N/A	... + U2	V4, W5, AD3, AE5, AK2
	XCV600	N/A	N/A	... + AC3	... + AF1
	XCV800	N/A	N/A	... + Y3	... + AA4
	XCV1000	N/A	N/A	N/A	... + AH4
V_{REF} Bank 4 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	V12, Y18	N/A	N/A	N/A
	XCV100/150	... + W15	AC12, AE5, AE8,	N/A	N/A
	XCV200/300	... + V14	... + AE4	AJ7, AL4, AL8, AL13	N/A
	XCV400	N/A	N/A	... + AK15	AL7, AL10, AL16, AM4, AM14
	XCV600	N/A	N/A	... + AK8	... + AL9
	XCV800	N/A	N/A	... + AJ12	... + AK13
	XCV1000	N/A	N/A	N/A	... + AN3
V_{REF} Bank 5 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	V9, Y3	N/A	N/A	N/A
	XCV100/150	... + W6	AC15, AC18, AD20	N/A	N/A
	XCV200/300	... + V7	... + AE23	AJ18, AJ25, AK23, AK27	N/A
	XCV400	N/A	N/A	... + AJ17	AJ18, AJ25, AL20, AL24, AL29
	XCV600	N/A	N/A	... + AL24	... + AM26
	XCV800	N/A	N/A	... + AH19	... + AN23
	XCV1000	N/A	N/A	N/A	... + AK28
V_{REF} Bank 6 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	M2, R3	N/A	N/A	N/A
	XCV100/150	... + T1	R24, Y26, AA25,	N/A	N/A
	XCV200/300	... + T3	... + AD26	V28, AB28, AE30, AF28	N/A
	XCV400	N/A	N/A	... + U28	V29, Y32, AD31, AE29, AK32
	XCV600	N/A	N/A	... + AC28	... + AE31
	XCV800	N/A	N/A	... + Y30	... + AA30
	XCV1000	N/A	N/A	N/A	... + AH30

Table 4: Virtex Pinout Tables (Fine-Pitch BGA) (Continued)

Pin Name	Device	FG256	FG456	FG676	FG680
No Connect (No-connect pins are listed incrementally. All pins listed for both the required device and all larger devices listed in the same package are no connects.)	XCV800	N/A	N/A	A2, A3, A15, A25, B1, B6, B11, B16, B21, B24, B26, C1, C2, C25, C26, F2, F6, F21, F25, L2, L25, N25, P2, T2, T25, AA2, AA6, AA21, AA25, AD1, AD2, AD25, AE1, AE3, AE6, AE11, AE14, AE16, AE21, AE24, AE26, AF2, AF24, AF25	N/A
	XCV600	N/A	N/A	same as above	N/A
	XCV400	N/A	N/A	... + A9, A10, A13, A16, A24, AC1, AC25, AE12, AE15, AF3, AF10, AF11, AF13, AF14, AF16, AF18, AF23, B4, B12, B13, B15, B17, D1, D25, H26, J1, K26, L1, M1, M25, N1, N26, P1, P26, R2, R26, T1, T26, U26, V1	N/A
	XCV300	N/A	D4, D19, W4, W19	N/A	N/A
	XCV200	N/A	... + A2, A6, A12, B11, B16, C2, D1, D18, E17, E19, G2, G22, L2, L19, M2, M21, R3, R20, U3, U18, Y22, AA1, AA3, AA11, AA16, AB7, AB12, AB21,	N/A	N/A
	XCV150	N/A	... + A13, A14, C8, C9, E13, F11, H21, J1, J4, K2, K18, K19, M17, N1, P1, P5, P22, R22, W13, W15, AA9, AA10, AB8, AB14	N/A	N/A

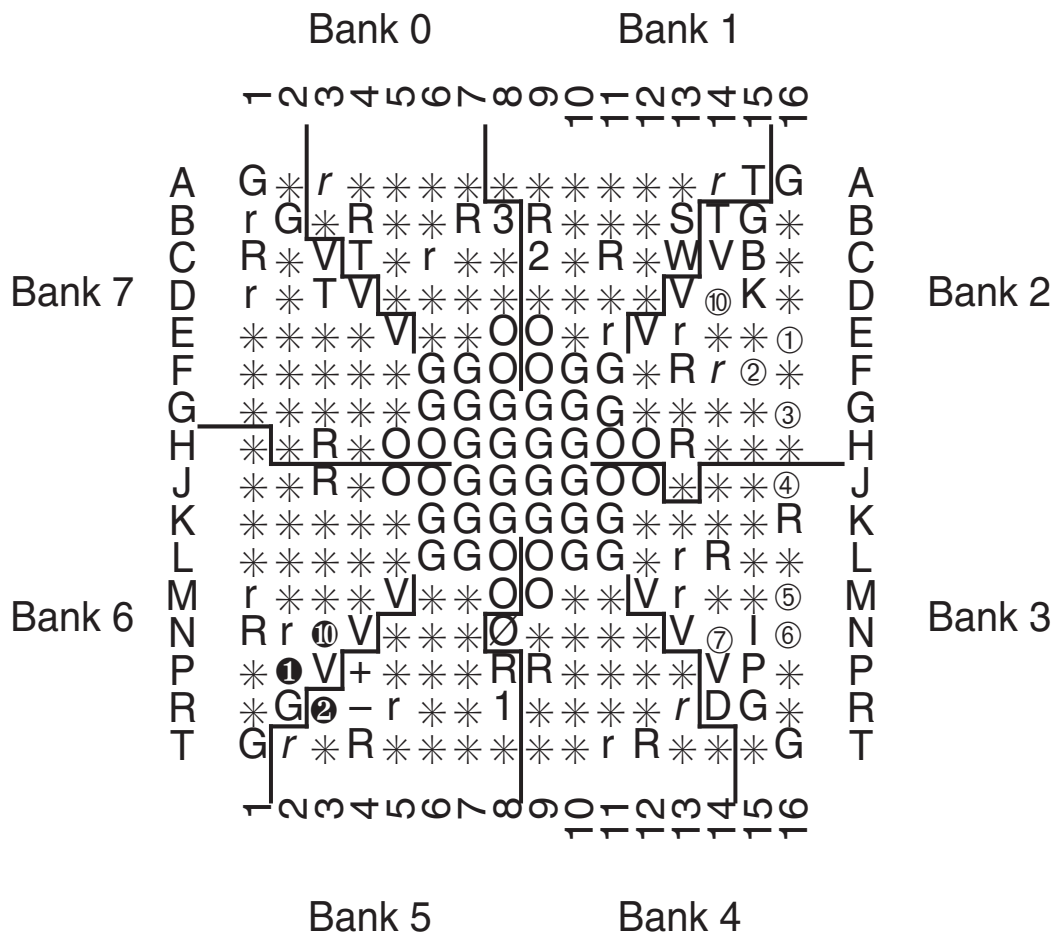
BG256 Pin Function Diagram



DS003 18 100300

Figure 4: BG256 Pin Function Diagram

FG256 Pin Function Diagram



FG256
(Top view)

Figure 8: FG256 Pin Function Diagram