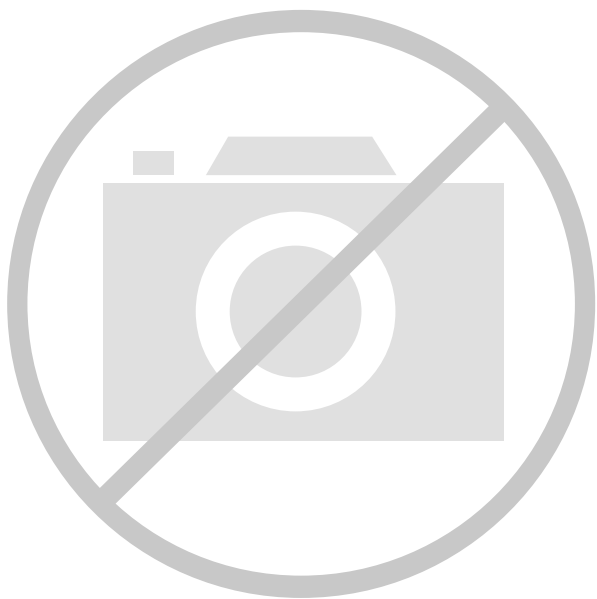




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

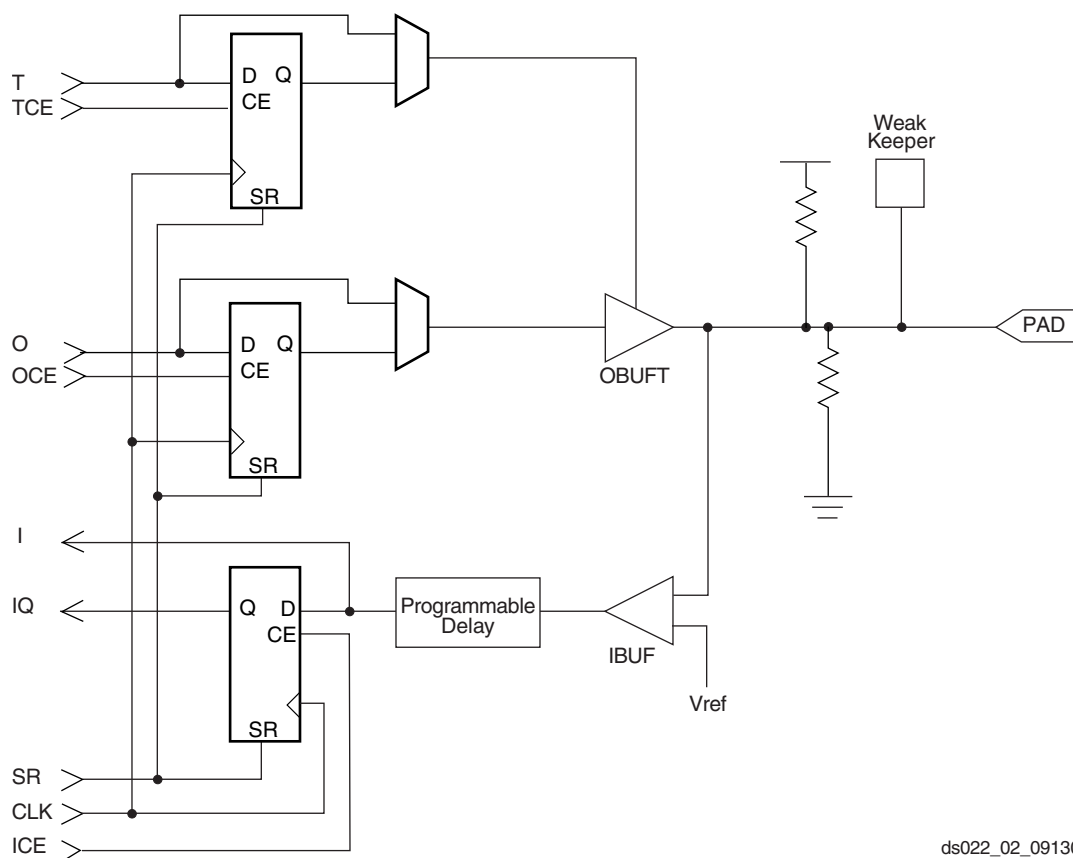
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1536
Number of Logic Elements/Cells	6912
Total RAM Bits	65536
Number of I/O	316
Number of Gates	322970
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	432-LBGA Exposed Pad, Metal
Supplier Device Package	432-MBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv300-4bg432c



ds022_02_091300

Figure 2: Virtex Input/Output Block (IOB)

Table 1: Supported Select I/O Standards

I/O Standard	Input Reference Voltage (V_{REF})	Output Source Voltage (V_{CCO})	Board Termination Voltage (V_{TT})	5 V Tolerant
LVTTL 2 – 24 mA	N/A	3.3	N/A	Yes
LVC MOS2	N/A	2.5	N/A	Yes
PCI, 5 V	N/A	3.3	N/A	Yes
PCI, 3.3 V	N/A	3.3	N/A	No
GTL	0.8	N/A	1.2	No
GTL+	1.0	N/A	1.5	No
HSTL Class I	0.75	1.5	0.75	No
HSTL Class III	0.9	1.5	1.5	No
HSTL Class IV	0.9	1.5	1.5	No
SSTL3 Class I & II	1.5	3.3	1.5	No
SSTL2 Class I & II	1.25	2.5	1.25	No
CTT	1.5	3.3	1.5	No
AGP	1.32	3.3	N/A	No

Each block SelectRAM cell, as illustrated in Figure 6, is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

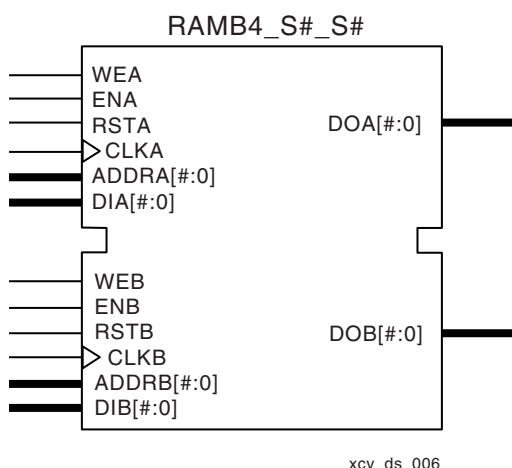


Figure 6: Dual-Port Block SelectRAM

Table 4 shows the depth and width aspect ratios for the block SelectRAM.

Table 4: Block SelectRAM Port Aspect Ratios

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

The Virtex block SelectRAM also includes dedicated routing to provide an efficient interface with both CLBs and other block SelectRAMs. Refer to XAPP130 for block SelectRAM timing waveforms.

Programmable Routing Matrix

It is the longest delay path that limits the speed of any worst-case design. Consequently, the Virtex routing architecture and its place-and-route software were defined in a single optimization process. This joint optimization minimizes long-path delays, and consequently, yields the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

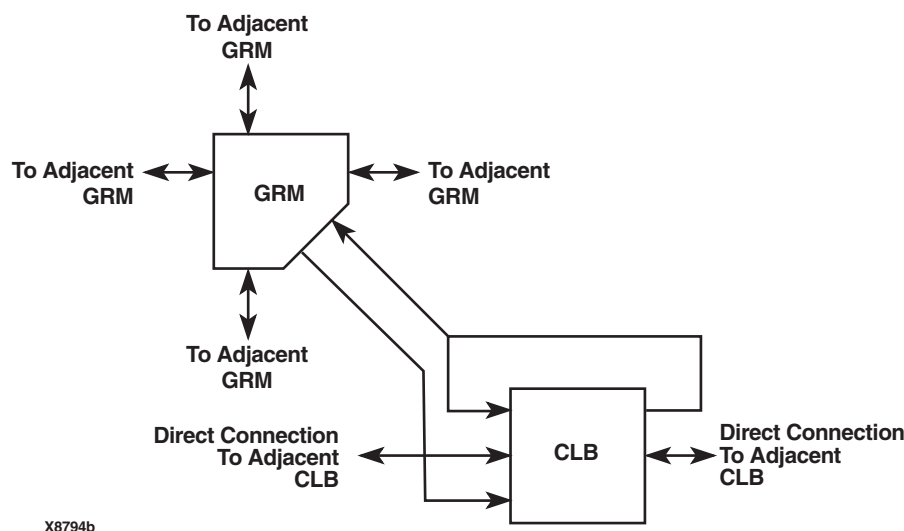


Figure 7: Virtex Local Routing

Local Routing

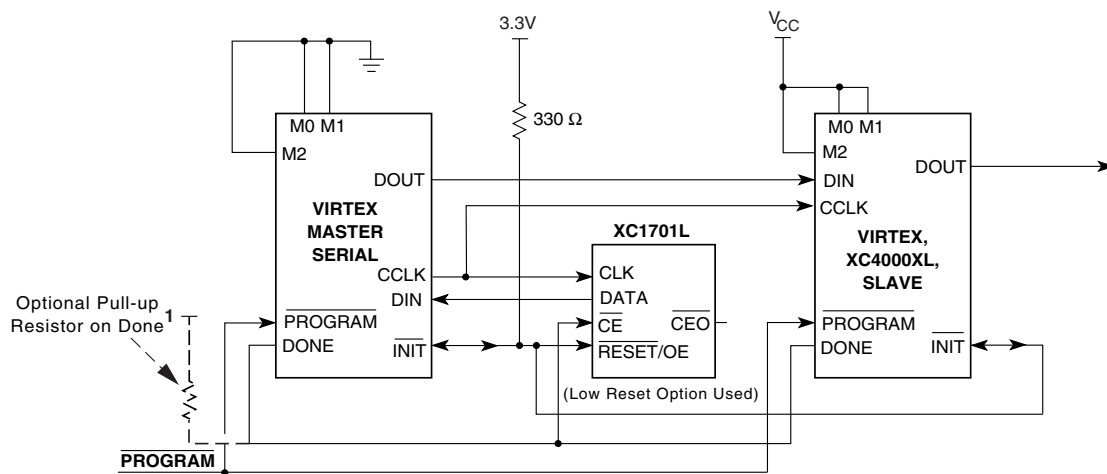
The VersaBlock provides local routing resources, as shown in Figure 7, providing the following three types of connections.

- Interconnections among the LUTs, flip-flops, and GRM

- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM.

Table 8: Master/Slave Serial Mode Programming Switching

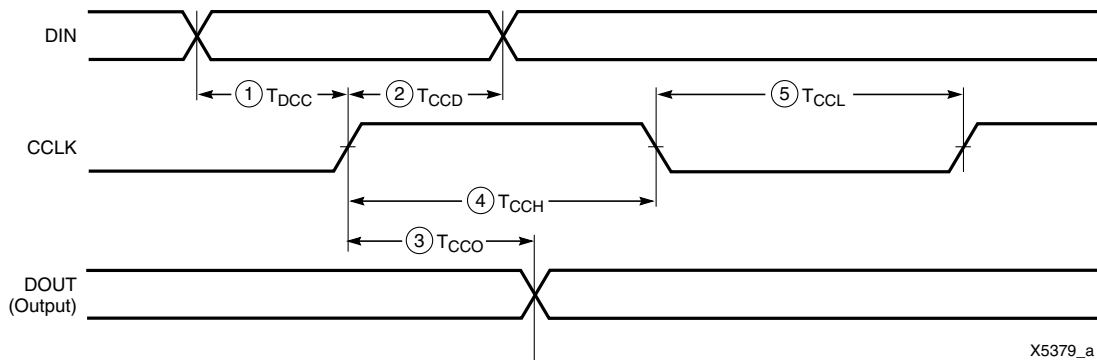
	Description	Figure References	Symbol	Values	Units
CCLK	DIN setup/hold, slave mode	1/2	T_{DCC}/T_{CCD}	5.0 / 0	ns, min
	DIN setup/hold, master mode	1/2	T_{DSCK}/T_{CKDS}	5.0 / 0	ns, min
	DOUT	3	T_{CCO}	12.0	ns, max
	High time	4	T_{CCH}	5.0	ns, min
	Low time	5	T_{CCL}	5.0	ns, min
	Maximum Frequency		F_{CC}	66	MHz, max
	Frequency Tolerance, master mode with respect to nominal			+45% -30%	



Note 1: If none of the Virtex FPGAs have been selected to drive DONE, an external pull-up resistor of 330 Ω should be added to the common DONE line. (For Spartan-XL devices, add a 4.7K Ω pull-up resistor.) This pull-up is not needed if the DriveDONE attribute is set. If used, DriveDONE should be selected only for the last device in the configuration chain.

xcv_12_050103

Figure 12: Master/Slave Serial Mode Circuit Diagram



X5379_a

Figure 13: Slave-Serial Mode Programming Switching Characteristics

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device⁽¹⁾ from 0 V. The current is highest at the fastest suggested ramp rate (0 V to nominal voltage in 2 ms) and is lowest at the slowest allowed ramp rate (0 V to nominal voltage in 50 ms). For more details on power supply requirements, see Application Note XAPP158 on www.xilinx.com.

Product	Description ⁽²⁾	Current Requirement ^(1,3)
Virtex Family, Commercial Grade	Minimum required current supply	500 mA
Virtex Family, Industrial Grade	Minimum required current supply	2 A

Notes:

- Ramp rate used for this specification is from 0 - 2.7 VDC. Peak current occurs on or near the internal power-on reset threshold of 1.0V and lasts for less than 3 ms.
- Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
- Larger currents can result if ramp rates are forced to be faster.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed output currents over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} for each standard with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTL ⁽¹⁾	-0.5	0.8	2.0	5.5	0.4	2.4	24	-24
LVC MOS2	-0.5	.7	1.7	5.5	0.4	1.9	12	-12
PCI, 3.3 V	-0.5	44% V_{CCINT}	60% V_{CCINT}	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI, 5.0 V	-0.5	0.8	2.0	5.5	0.55	2.4	Note 2	Note 2
GTL	-0.5	$V_{REF} - 0.05$	$V_{REF} + 0.05$	3.6	0.4	n/a	40	n/a
GTL+	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.6	n/a	36	n/a
HSTL I ⁽³⁾	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	8	-8
HSTL III	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	24	-8
HSTL IV	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	48	-8
SSTL3 I	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.6$	$V_{REF} + 0.6$	8	-8
SSTL3 II	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.8$	$V_{REF} + 0.8$	16	-16
SSTL2 I	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.61$	$V_{REF} + 0.61$	7.6	-7.6
SSTL2 II	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.80$	$V_{REF} + 0.80$	15.2	-15.2
CTT	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
AGP	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Notes:

- V_{OL} and V_{OH} for lower drive currents are sample tested.
- Tested according to the relevant specifications.
- DC input and output levels for HSTL18 (HSTL I/O standard with V_{CCO} of 1.8 V) are provided in an HSTL white paper on www.xilinx.com.

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Clock CLK to Pad delay with OBUFT enabled (non-3-state)	T_{IOCKP}	1.0	2.9	3.2	3.5	ns, max
Clock CLK to Pad high-impedance (synchronous) ⁽¹⁾	T_{IOCKHZ}	1.1	2.3	2.5	2.9	ns, max
Clock CLK to valid data on Pad delay, plus enable delay for OBUFT	T_{IOCKON}	1.5	3.4	3.7	4.1	ns, max
Setup and Hold Times before/after Clock CLK⁽²⁾		Setup Time / Hold Time				
O input	T_{IOOCK}/T_{IOCKO}	0.51 / 0	1.1 / 0	1.2 / 0	1.3 / 0	ns, min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$	0.37 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
SR input (OFF)	$T_{IOSRCKO}/T_{IOCKOSR}$	0.52 / 0	1.1 / 0	1.2 / 0	1.4 / 0	ns, min
3-State Setup Times, T input	T_{IOTCK}/T_{IOCKT}	0.34 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$	0.41 / 0	0.9 / 0	0.9 / 0	1.1 / 0	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$	0.49 / 0	1.0 / 0	1.1 / 0	1.3 / 0	ns, min
Set/Reset Delays						
SR input to Pad (asynchronous)	T_{IOSRP}	1.6	3.8	4.1	4.6	ns, max
SR input to Pad high-impedance (asynchronous) ⁽¹⁾	T_{IOSRHZ}	1.6	3.1	3.4	3.9	ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}	2.0	4.2	4.6	5.1	ns, max
GSR to Pad	T_{IOGSRQ}	4.9	9.7	10.9	12.5	ns, max

Notes:

1. 3-state turn-off delays should not be adjusted.
2. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Description	Symbol	Standard ⁽¹⁾	Speed Grade				Unit s
			Min	-6	-5	-4	
Output Delay Adjustments							
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T _{OLVTTL_S2}	LVTTL, Slow, 2 mA	4.2	14.7	15.8	17.0	ns
	T _{OLVTTL_S4}	4 mA	2.5	7.5	8.0	8.6	ns
	T _{OLVTTL_S6}	6 mA	1.8	4.8	5.1	5.6	ns
	T _{OLVTTL_S8}	8 mA	1.2	3.0	3.3	3.5	ns
	T _{OLVTTL_S12}	12 mA	1.0	1.9	2.1	2.2	ns
	T _{OLVTTL_S16}	16 mA	0.9	1.7	1.9	2.0	ns
	T _{OLVTTL_S24}	24 mA	0.8	1.3	1.4	1.6	ns
	T _{OLVTTL_F2}	LVTTL, Fast, 2mA	1.9	13.1	14.0	15.1	ns
	T _{OLVTTL_F4}	4 mA	0.7	5.3	5.7	6.1	ns
	T _{OLVTTL_F6}	6 mA	0.2	3.1	3.3	3.6	ns
	T _{OLVTTL_F8}	8 mA	0.1	1.0	1.1	1.2	ns
	T _{OLVTTL_F12}	12 mA	0	0	0	0	ns
	T _{OLVTTL_F16}	16 mA	−0.10	−0.05	−0.05	−0.05	ns
	T _{OLVTTL_F24}	24 mA	−0.10	−0.20	−0.21	−0.23	ns
	T _{OLVCMOS2}	LVC MOS2	0.10	0.10	0.11	0.12	ns
	T _{OPCI33_3}	PCI, 33 MHz, 3.3 V	0.50	2.3	2.5	2.7	ns
	T _{OPCI33_5}	PCI, 33 MHz, 5.0 V	0.40	2.8	3.0	3.3	ns
	T _{OPCI66_3}	PCI, 66 MHz, 3.3 V	0.10	−0.40	−0.42	−0.46	ns
	T _{OGTL}	GTL	0.6	0.50	0.54	0.6	ns
	T _{OGTLP}	GTL+	0.7	0.8	0.9	1.0	ns
	T _{OHSTL_I}	HSTL I	0.10	−0.50	−0.53	−0.5	ns
	T _{OHSTL_III}	HSTL III	−0.10	−0.9	−0.9	−1.0	ns
	T _{OHSTL_IV}	HSTL IV	−0.20	−1.0	−1.0	−1.1	ns
	T _{OSSTL2_I}	SSTL2 I	−0.10	−0.50	−0.53	−0.5	ns
	T _{OSSTL2_II}	SSTL2 II	−0.20	−0.9	−0.9	−1.0	ns
	T _{OSSTL3_I}	SSTL3 I	−0.20	−0.50	−0.53	−0.5	ns
	T _{OSSTL3_II}	SSTL3 II	−0.30	−1.0	−1.0	−1.1	ns
	T _{OCTT}	CTT	0	−0.6	−0.6	−0.6	ns
	T _{OAGP}	AGP	0	−0.9	−0.9	−1.0	ns

Notes:

- Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTTL. For other I/O standards and different loads, see [Table 2](#) and [Table 3](#).

I/O Standard Global Clock Input Adjustments

Description	Symbol	Standard ⁽¹⁾	Speed Grade				Units
			Min	-6	-5	-4	
Data Input Delay Adjustments							
Standard-specific global clock input delay adjustments	T _{GPLVTTL}	LVTTL	0	0	0	0	ns, max
	T _{GPLVCMOS2}	LVC MOS2	−0.02	−0.04	−0.04	−0.05	ns, max
	T _{GP PCI33_3}	PCI, 33 MHz, 3.3 V	−0.05	−0.11	−0.12	−0.14	ns, max
	T _{GP PCI33_5}	PCI, 33 MHz, 5.0 V	0.13	0.25	0.28	0.33	ns, max
	T _{GP PCI66_3}	PCI, 66 MHz, 3.3 V	−0.05	−0.11	−0.12	−0.14	ns, max
	T _{GPGTL}	GTL	0.7	0.8	0.9	0.9	ns, max
	T _{GPGTLP}	GTL+	0.7	0.8	0.8	0.8	ns, max
	T _{GPHSTL}	HSTL	0.7	0.7	0.7	0.7	ns, max
	T _{GPSSTL2}	SSTL2	0.6	0.52	0.51	0.50	ns, max
	T _{GPSSTL3}	SSTL3	0.6	0.6	0.55	0.54	ns, max
	T _{GPCTT}	CTT	0.7	0.7	0.7	0.7	ns, max
	T _{GPAGP}	AGP	0.6	0.54	0.53	0.52	ns, max

Notes:

1. Input timing for GPLVTTL is measured at 1.4 V. For other I/O standards, see [Table 3](#).

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Combinatorial Delays						
4-input function: F/G inputs to X/Y outputs	T _{ILO}	0.29	0.6	0.7	0.8	ns, max
5-input function: F/G inputs to F5 output	T _{IF5}	0.32	0.7	0.8	0.9	ns, max
5-input function: F/G inputs to X output	T _{IF5X}	0.36	0.8	0.8	1.0	ns, max
6-input function: F/G inputs to Y output via F6 MUX	T _{IF6Y}	0.44	0.9	1.0	1.2	ns, max
6-input function: F5IN input to Y output	T _{F5INY}	0.17	0.32	0.36	0.42	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T _{IFNCTL}	0.31	0.7	0.7	0.8	ns, max
BY input to YB output	T _{BYYB}	0.27	0.53	0.6	0.7	ns, max
Sequential Delays						
FF Clock CLK to XQ/YQ outputs	T _{CKO}	0.54	1.1	1.2	1.4	ns, max
Latch Clock CLK to XQ/YQ outputs	T _{CKLO}	0.6	1.2	1.4	1.6	ns, max
Setup and Hold Times before/after Clock CLK ⁽¹⁾	Setup Time / Hold Time					
4-input function: F/G Inputs	T _{ICK} /T _{CKI}	0.6 / 0	1.2 / 0	1.4 / 0	1.5 / 0	ns, min
5-input function: F/G inputs	T _{IF5CK} /T _{CKIF5}	0.7 / 0	1.3 / 0	1.5 / 0	1.7 / 0	ns, min
6-input function: F5IN input	T _{F5INCK} /T _{CKF5IN}	0.46 / 0	1.0 / 0	1.1 / 0	1.2 / 0	ns, min
6-input function: F/G inputs via F6 MUX	T _{IF6CK} /T _{CKIF6}	0.8 / 0	1.5 / 0	1.7 / 0	1.9 / 0	ns, min
BX/BY inputs	T _{DICK} /T _{CKDI}	0.30 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
CE input	T _{CECK} /T _{CKCE}	0.37 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
SR/BY inputs (synchronous)	T _{RCK} T _{CKR}	0.33 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T _{CH}	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low	T _{CL}	0.8	1.5	1.7	2.0	ns, min
Set/Reset						
Minimum Pulse Width, SR/BY inputs	T _{RPW}	1.3	2.5	2.8	3.3	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T _{RQ}	0.54	1.1	1.3	1.4	ns, max
Delay from GSR to XQ/YQ outputs	T _{IOGSRQ}	4.9	9.7	10.9	12.5	ns, max
Toggle Frequency (MHz) (for export control)	F _{TOG} (MHz)	625	333	294	250	MHz

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Virtex Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL

Description	Symbol	Device	Speed Grade				Units
			Min	-6	-5	-4	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, <i>with</i> DLL. For data <i>output</i> with different standards, adjust delays with the values shown in Output Delay Adjustments.	T _{ICKOFDLL}	XCV50	1.0	3.1	3.3	3.6	ns, max
		XCV100	1.0	3.1	3.3	3.6	ns, max
		XCV150	1.0	3.1	3.3	3.6	ns, max
		XCV200	1.0	3.1	3.3	3.6	ns, max
		XCV300	1.0	3.1	3.3	3.6	ns, max
		XCV400	1.0	3.1	3.3	3.6	ns, max
		XCV600	1.0	3.1	3.3	3.6	ns, max
		XCV800	1.0	3.1	3.3	3.6	ns, max
		XCV1000	1.0	3.1	3.3	3.6	ns, max

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see [Table 2](#) and [Table 3](#).
3. DLL output jitter is already included in the timing calculation.

Global Clock Input-to-Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL

Description	Symbol	Device	Speed Grade				Units
			Min	-6	-5	-4	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, <i>without</i> DLL. For data <i>output</i> with different standards, adjust delays with the values shown in Input and Output Delay Adjustments. For I/O standards requiring V _{REF} such as GTL, GTL+, SSTL, HSTL, CTT, and AGO, an additional 600 ps must be added.	T _{ICKOF}	XCV50	1.5	4.6	5.1	5.7	ns, max
		XCV100	1.5	4.6	5.1	5.7	ns, max
		XCV150	1.5	4.7	5.2	5.8	ns, max
		XCV200	1.5	4.7	5.2	5.8	ns, max
		XCV300	1.5	4.7	5.2	5.9	ns, max
		XCV400	1.5	4.8	5.3	6.0	ns, max
		XCV600	1.6	4.9	5.4	6.0	ns, max
		XCV800	1.6	4.9	5.5	6.2	ns, max
		XCV1000	1.7	5.0	5.6	6.3	ns, max

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see [Table 2](#) and [Table 3](#).

Minimum Clock-to-Out for Virtex Devices

I/O Standard	With DLL	Without DLL									
	All Devices	V50	V100	V150	V200	V300	V400	V600	V800	V1000	Units
*LVTTTL_S2	5.2	6.0	6.0	6.0	6.0	6.1	6.1	6.1	6.1	6.1	ns
*LVTTTL_S4	3.5	4.3	4.3	4.3	4.3	4.4	4.4	4.4	4.4	4.4	ns
*LVTTTL_S6	2.8	3.6	3.6	3.6	3.6	3.7	3.7	3.7	3.7	3.7	ns
*LVTTTL_S8	2.2	3.1	3.1	3.1	3.1	3.1	3.1	3.2	3.2	3.2	ns
*LVTTTL_S12	2.0	2.9	2.9	2.9	2.9	2.9	2.9	3.0	3.0	3.0	ns
*LVTTTL_S16	1.9	2.8	2.8	2.8	2.8	2.8	2.8	2.9	2.9	2.9	ns
*LVTTTL_S24	1.8	2.6	2.6	2.7	2.7	2.7	2.7	2.7	2.7	2.8	ns
*LVTTTL_F2	2.9	3.8	3.8	3.8	3.8	3.8	3.8	3.9	3.9	3.9	ns
*LVTTTL_F4	1.7	2.6	2.6	2.6	2.6	2.6	2.6	2.7	2.7	2.7	ns
*LVTTTL_F6	1.2	2.0	2.0	2.0	2.1	2.1	2.1	2.1	2.1	2.2	ns
*LVTTTL_F8	1.1	1.9	1.9	1.9	1.9	2.0	2.0	2.0	2.0	2.0	ns
*LVTTTL_F12	1.0	1.8	1.8	1.8	1.8	1.9	1.9	1.9	1.9	1.9	ns
*LVTTTL_F16	0.9	1.7	1.8	1.8	1.8	1.8	1.8	1.8	1.9	1.9	ns
*LVTTTL_F24	0.9	1.7	1.7	1.7	1.8	1.8	1.8	1.8	1.8	1.9	ns
LVCMS2	1.1	1.9	1.9	1.9	2.0	2.0	2.0	2.0	2.0	2.1	ns
PCI33_3	1.5	2.4	2.4	2.4	2.4	2.4	2.4	2.5	2.5	2.5	ns
PCI33_5	1.4	2.2	2.2	2.3	2.3	2.3	2.3	2.3	2.3	2.4	ns
PCI66_3	1.1	1.9	1.9	2.0	2.0	2.0	2.0	2.0	2.1	2.1	ns
GTL	1.6	2.5	2.5	2.5	2.5	2.5	2.5	2.6	2.6	2.6	ns
GTL+	1.7	2.5	2.5	2.6	2.6	2.6	2.6	2.6	2.6	2.7	ns
HSTL I	1.1	1.9	1.9	1.9	1.9	2.0	2.0	2.0	2.0	2.0	ns
HSTL III	0.9	1.7	1.7	1.8	1.8	1.8	1.8	1.8	1.8	1.9	ns
HSTL IV	0.8	1.6	1.6	1.6	1.7	1.7	1.7	1.7	1.7	1.8	ns
SSTL2 I	0.9	1.7	1.7	1.7	1.7	1.8	1.8	1.8	1.8	1.8	ns
SSTL2 II	0.8	1.6	1.6	1.6	1.6	1.7	1.7	1.7	1.7	1.7	ns
SSTL3 I	0.8	1.6	1.7	1.7	1.7	1.7	1.7	1.7	1.8	1.8	ns
SSTL3 II	0.7	1.5	1.5	1.6	1.6	1.6	1.6	1.6	1.6	1.7	ns
CTT	1.0	1.8	1.8	1.8	1.9	1.9	1.9	1.9	1.9	2.0	ns
AGP	1.0	1.8	1.8	1.9	1.9	1.9	1.9	1.9	1.9	2.0	ns

*S = Slow Slew Rate, F = Fast Slew Rate

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Input and output timing is measured at 1.4 V for LVTTTL. For other I/O standards, see Table 3. In all cases, an 8 pF external capacitive load is used.

DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Description	Symbol	Speed Grade						Units
		-6		-5		-4		
		Min	Max	Min	Max	Min	Max	
Input Clock Frequency (CLKDLLHF)	FCLKINHF	60	200	60	180	60	180	MHz
Input Clock Frequency (CLKDLL)	FCLKINLF	25	100	25	90	25	90	MHz
Input Clock Pulse Width (CLKDLLHF)	T _{DLLPWHF}	2.0	-	2.4	-	2.4	-	ns
Input Clock Pulse Width (CLKDLL)	T _{DLLPWLF}	2.5	-	3.0		3.0	-	ns

Notes:

1. All specifications correspond to Commercial Operating Temperatures (0°C to +85°C).

DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

Description	Symbol	F _{CLKIN}	CLKDLLHF		CLKDLL		Units
			Min	Max	Min	Max	
Input Clock Period Tolerance	T _{IPTOL}		-	1.0	-	1.0	ns
Input Clock Jitter Tolerance (Cycle to Cycle)	T _{IJTCC}		-	± 150	-	± 300	ps
Time Required for DLL to Acquire Lock	T _{LOCK}	> 60 MHz	-	20	-	20	μs
		50 - 60 MHz	-	-	-	25	μs
		40 - 50 MHz	-	-	-	50	μs
		30 - 40 MHz	-	-	-	90	μs
		25 - 30 MHz	-	-	-	120	μs
Output Jitter (cycle-to-cycle) for any DLL Clock Output ⁽¹⁾	T _{OJTCC}			± 60		± 60	ps
Phase Offset between CLKIN and CLKO ⁽²⁾	T _{PHIO}			± 100		± 100	ps
Phase Offset between Clock Outputs on the DLL ⁽³⁾	T _{PHOO}			± 140		± 140	ps
Maximum Phase Difference between CLKIN and CLKO ⁽⁴⁾	T _{PHIOM}			± 160		± 160	ps
Maximum Phase Difference between Clock Outputs on the DLL ⁽⁵⁾	T _{PHOOM}			± 200		± 200	ps

Notes:

1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* Output Jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN and CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of Output Jitter and Phase Offset between any two DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).
6. All specifications correspond to Commercial Operating Temperatures (0°C to +85°C).

Table 2: Virtex Pinout Tables (Chip-Scale and QFP Packages) (Continued)

Pin Name	Device	CS144	TQ144	PQ/HQ240
V_{CCO}	All	Banks 0 and 1: A2, A13, D7 Banks 2 and 3: B12, G11, M13 Banks 4 and 5: N1, N7, N13 Banks 6 and 7: B2, G2, M2	No I/O Banks in this package: 1, 17, 37, 55, 73, 92, 109, 128	No I/O Banks in this package: 15, 30, 44, 61, 76, 90, 105, 121, 136, 150, 165, 180, 197, 212, 226, 240
V_{REF} Bank 0 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	C4, D6	5, 13	218, 232
	XCV100/150	... + B4	... + 7	... + 229
	XCV200/300	N/A	N/A	... + 236
	XCV400	N/A	N/A	... + 215
	XCV600	N/A	N/A	... + 230
	XCV800	N/A	N/A	... + 222
V_{REF} Bank 1 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	A10, B8	22, 30	191, 205
	XCV100/150	... + D9	... + 28	... + 194
	XCV200/300	N/A	N/A	... + 187
	XCV400	N/A	N/A	... + 208
	XCV600	N/A	N/A	... + 193
	XCV800	N/A	N/A	... + 201
V_{REF} Bank 2 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	D11, F10	42, 50	157, 171
	XCV100/150	... + D13	... + 44	... + 168
	XCV200/300	N/A	N/A	... + 175
	XCV400	N/A	N/A	... + 154
	XCV600	N/A	N/A	... + 169
	XCV800	N/A	N/A	... + 161

Table 3: Virtex Pinout Tables (BGA) (Continued)

Pin Name	Device	BG256	BG352	BG432	BG560
V_{REF} Bank 7 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	G3, H1	N/A	N/A	N/A
	XCV100/150	... + D1	D26, G26, L26	N/A	N/A
	XCV200/300	... + B2	... + E24	F28, F31, J30, N30	N/A
	XCV400	N/A	N/A	... + R31	E31, G31, K31, P31, T31
	XCV600	N/A	N/A	... + J28	... + H32
	XCV800	N/A	N/A	... + M28	... + L33
	XCV1000	N/A	N/A	N/A	... + D31
GND	All	C3, C18, D4, D5, D9, D10, D11, D12, D16, D17, E4, E17, J4, J17, K4, K17, L4, L17, M4, M17, T4, T17, U4, U5, U9, U10, U11, U12, U16, U17, V3, V18	A1, A2, A5, A8, A14, A19, A22, A25, A26, B1, B26, E1, E26, H1, H26, N1, P26, W1, W26, AB1, AB26, AE1, AE26, AF1, AF2, AF5, AF8, AF13, AF19, AF22, AF25, AF26	A2, A3, A7, A9, A14, A18, A23, A25, A29, A30, B1, B2, B30, B31, C1, C31, D16, G1, G31, J1, J31, P1, P31, T4, T28, V1, V31, AC1, AC31, AE1, AE31, AH16, AJ1, AJ31, AK1, AK2, AK30, AK31, AL2, AL3, AL7, AL9, AL14, AL18, AL23, AL25, AL29, AL30	A1, A7, A12, A14, A18, A20, A24, A29, A32, A33, B1, B6, B9, B15, B23, B27, B31, C2, E1, F32, G2, G33, J32, K1, L2, M33, P1, P33, R32, T1, V33, W2, Y1, Y33, AB1, AC32, AD33, AE2, AG1, AG32, AH2, AJ33, AL32, AM3, AM7, AM11, AM19, AM25, AM28, AM33, AN1, AN2, AN5, AN10, AN14, AN16, AN20, AN22, AN27, AN33
GND ⁽¹⁾	All	J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12	N/A	N/A	N/A
No Connect	All	N/A	N/A	N/A	C31, AC2, AK4, AL3

Notes:

1. 16 extra balls (grounded) at package center.

Table 4: Virtex Pinout Tables (Fine-Pitch BGA)

Pin Name	Device	FG256	FG456	FG676	FG680
GCK0	All	N8	W12	AA14	AW19
GCK1	All	R8	Y11	AB13	AU22
GCK2	All	C9	A11	C13	D21
GCK3	All	B8	C11	E13	A20
M0	All	N3	AB2	AD4	AT37
M1	All	P2	U5	W7	AU38
M2	All	R3	Y4	AB6	AT35
CCLK	All	D15	B22	D24	E4
PROGRAM	All	P15	W20	AA22	AT5
DONE	All	R14	Y19	AB21	AU5
INIT	All	N15	V19	Y21	AU2
BUSY/DOUT	All	C15	C21	E23	E3
D0/DIN	All	D14	D20	F22	C2
D1	All	E16	H22	K24	P4
D2	All	F15	H20	K22	P3
D3	All	G16	K20	M22	R1
D4	All	J16	N22	R24	AD3
D5	All	M16	R21	U23	AG2
D6	All	N16	T22	V24	AH1
D7	All	N14	Y21	AB23	AR4
WRITE	All	C13	A20	C22	B4
CS	All	B13	C19	E21	D5
TDI	All	A15	B20	D22	B3
TDO	All	B14	A21	C23	C4
TMS	All	D3	D3	F5	E36
TCK	All	C4	C4	E6	C36
DXN	All	R4	Y5	AB7	AV37
DXP	All	P4	V6	Y8	AU35

Table 4: Virtex Pinout Tables (Fine-Pitch BGA) (Continued)

Pin Name	Device	FG256	FG456	FG676	FG680
V_{REF} Bank 1 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	B9, C11	N/A	N/A	N/A
	XCV100/150	... + E11	A18, B13, E14	N/A	N/A
	XCV200/300	... + A14	... + A19	N/A	N/A
	XCV400	N/A	N/A	A14, C20, C21, D15, G16	N/A
	XCV600	N/A	N/A	... + B19	B6, B8, B18, D11, D13, D17
	XCV800	N/A	N/A	... + A17	... + B14
	XCV1000	N/A	N/A	N/A	... + B5
V_{REF} Bank 2 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	F13, H13	N/A	N/A	N/A
	XCV100/150	... + F14	F21, H18, K21	N/A	N/A
	XCV200/300	... + E13	... + D22	N/A	N/A
	XCV400	N/A	N/A	F24, H23, K20, M23, M26	N/A
	XCV600	N/A	N/A	... + G26	G1, H4, J1, L2, V5, W3
	XCV800	N/A	N/A	... + K25	... + N1
	XCV1000	N/A	N/A	N/A	... + D2
V_{REF} Bank 3 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	K16, L14	N/A	N/A	N/A
	XCV100/150	... + L13	N21, R19, U21	N/A	N/A
	XCV200/300	... + M13	... + U20	N/A	N/A
	XCV400	N/A	N/A	R23, R25, U21, W22, W23	N/A
	XCV600	N/A	N/A	... + W26	AC1, AJ2, AK3, AL4, AR1, Y1
	XCV800	N/A	N/A	... + U25	... + AF3
	XCV1000	N/A	N/A	N/A	... + AP4

Table 4: Virtex Pinout Tables (Fine-Pitch BGA) (Continued)

Pin Name	Device	FG256	FG456	FG676	FG680
V_{REF} Bank 4 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	P9, T12	N/A	N/A	N/A
	XCV100/150	... + T11	AA13, AB16, AB19	N/A	N/A
	XCV200/300	... + R13	... + AB20	N/A	N/A
	XCV400	N/A	N/A	AC15, AD18, AD21, AD22, AF15	N/A
	XCV600	N/A	N/A	... + AF20	AT19, AU7, AU17, AV8, AV10, AW11
	XCV800	N/A	N/A	... + AF17	... + AV14
	XCV1000	N/A	N/A	N/A	... + AU6
V_{REF} Bank 5 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	T4, P8	N/A	N/A	N/A
	XCV100/150	... + R5	W8, Y10, AA5	N/A	N/A
	XCV200/300	... + T2	... + Y6	N/A	N/A
	XCV400	N/A	N/A	AA10, AB8, AB12, AC7, AF12	N/A
	XCV600	N/A	N/A	... + AF8	AT27, AU29, AU31, AV35, AW21, AW23
	XCV800	N/A	N/A	... + AE10	... + AT25
	XCV1000	N/A	N/A	N/A	... + AV36
V_{REF} Bank 6 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	J3, N1	N/A	N/A	N/A
	XCV100/150	... + M1	N2, R4, T3	N/A	N/A
	XCV200/300	... + N2	... + Y1	N/A	N/A
	XCV400	N/A	N/A	AB3, R1, R4, U6, V5	N/A
	XCV600	N/A	N/A	... + Y1	AB35, AD37, AH39, AK39, AM39, AN36
	XCV800	N/A	N/A	... + U2	... + AE39
	XCV1000	N/A	N/A	N/A	... + AT39

Table 4: Virtex Pinout Tables (Fine-Pitch BGA) (Continued)

Pin Name	Device	FG256	FG456	FG676	FG680
V_{REF} Bank 7 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	C1, H3	N/A	N/A	N/A
	XCV100/150	... + D1	E2, H4, K3	N/A	N/A
	XCV200/300	... + B1	... + D2	N/A	N/A
	XCV400	N/A	N/A	F4, G4, K6, M2, M5	N/A
	XCV600	N/A	N/A	... + H1	E38, G38, L36, N36, U36, U38
	XCV800	N/A	N/A	... + K1	... + N38
	XCV1000	N/A	N/A	N/A	... + F36
GND	All	A1, A16, B2, B15, F6, F7, F10, F11, G6, G7, G8, G9, G10, G11, H7, H8, H9, H10, J7, J8, J9, J10, K6, K7, K8, K9, K10, K11, L6, L7, L10, L11, R2, R15, T1, T16	A1, A22, B2, B21, C3, C20, J9, J10, J11, J12, J13, J14, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N9, N10, N11, N12, N13, N14, P9, P10, P11, P12, P13, P14, Y3, Y20, AA2, AA21, AB1, AB22	A1, A26, B2, B9, B14, B18, B25, C3, C24, D4, D23, E5, E22, J2, J25, K10, K11, K12, K13, K14, K15, K16, K17, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N2, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, P25, R10, R11, R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17, V2, V25, AB5, AB22, AC4, AC23, AD3, AD24, AE2, AE9, AE13, AE18, AE25, AF1, AF26	A1, A2, A3, A37, A38, A39, AA5, AA35, AH4, AH5, AH35, AH36, AR5, AR12, AR19, AR20, AR21, AR28, AR35, AT4, AT12, AT20, AT28, AT36, AU1, AU3, AU20, AU37, AU39, AV1, AV2, AV38, AV39, AW1, AW2, AW3, AW37, AW38, AW39, B1, B2, B38, B39, C1, C3, C20, C37, C39, D4, D12, D20, D28, D36, E5, E12, E19, E20, E21, E28, E35, M4, M5, M35, M36, W5, W35, Y3, Y4, Y5, Y35, Y36, Y37

Pinout Diagrams

The following diagrams, **CS144 Pin Function Diagram**, page 17 through **FG680 Pin Function Diagram**, page 27, illustrate the locations of special-purpose pins on Virtex FPGAs. Table 5 lists the symbols used in these diagrams. The diagrams also show I/O-bank boundaries.

Table 5: Pinout Diagram Symbols

Symbol	Pin Function
*	General I/O
*	Device-dependent general I/O, n/c on smaller devices
V	V _{CCINT}
v	Device-dependent V _{CCINT} , n/c on smaller devices
O	V _{CCO}
R	V _{REF}
r	Device-dependent V _{REF} , remains I/O on smaller devices
G	Ground
Ø, 1, 2, 3	Global Clocks

Table 5: Pinout Diagram Symbols (Continued)

Symbol	Pin Function
⑩, ①, ②	M0, M1, M2
⑩, ①, ②, ③, ④, ⑤, ⑥, ⑦	D0/DIN, D1, D2, D3, D4, D5, D6, D7
B	DOUT/BUSY
D	DONE
P	PROGRAM
I	INIT
K	CCLK
W	WRITE
S	CS
T	Boundary-scan Test Access Port
+	Temperature diode, anode
–	Temperature diode, cathode
n	No connect

CS144 Pin Function Diagram

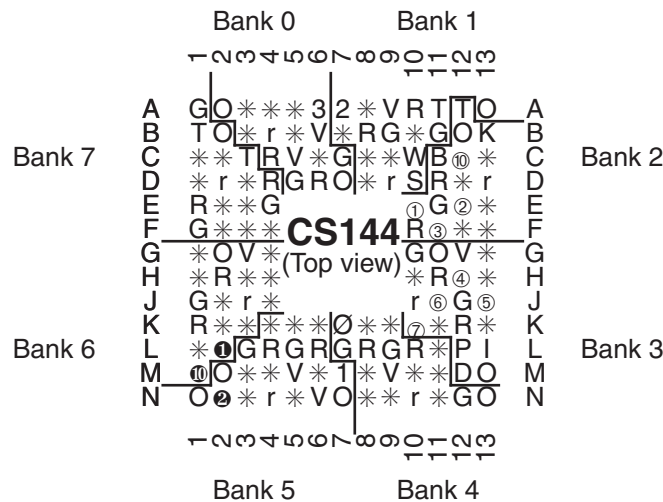
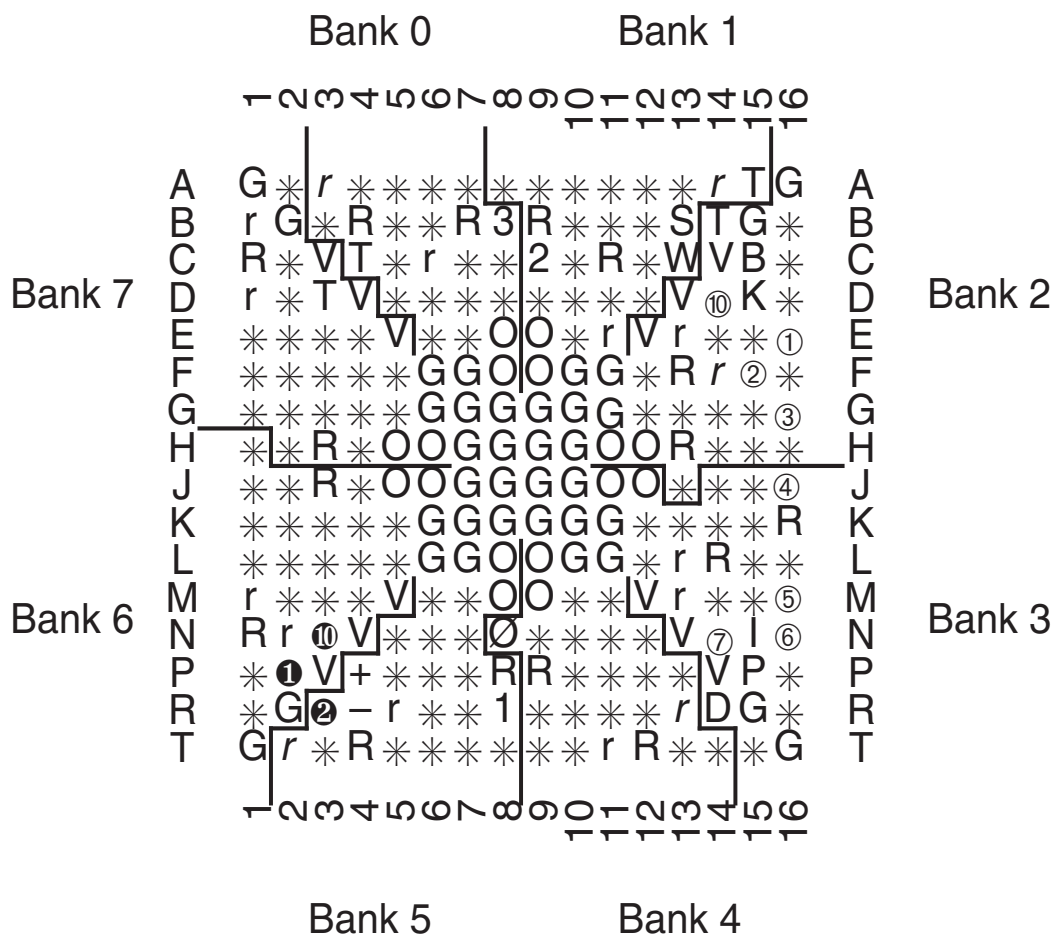


Figure 1: CS144 Pin Function Diagram

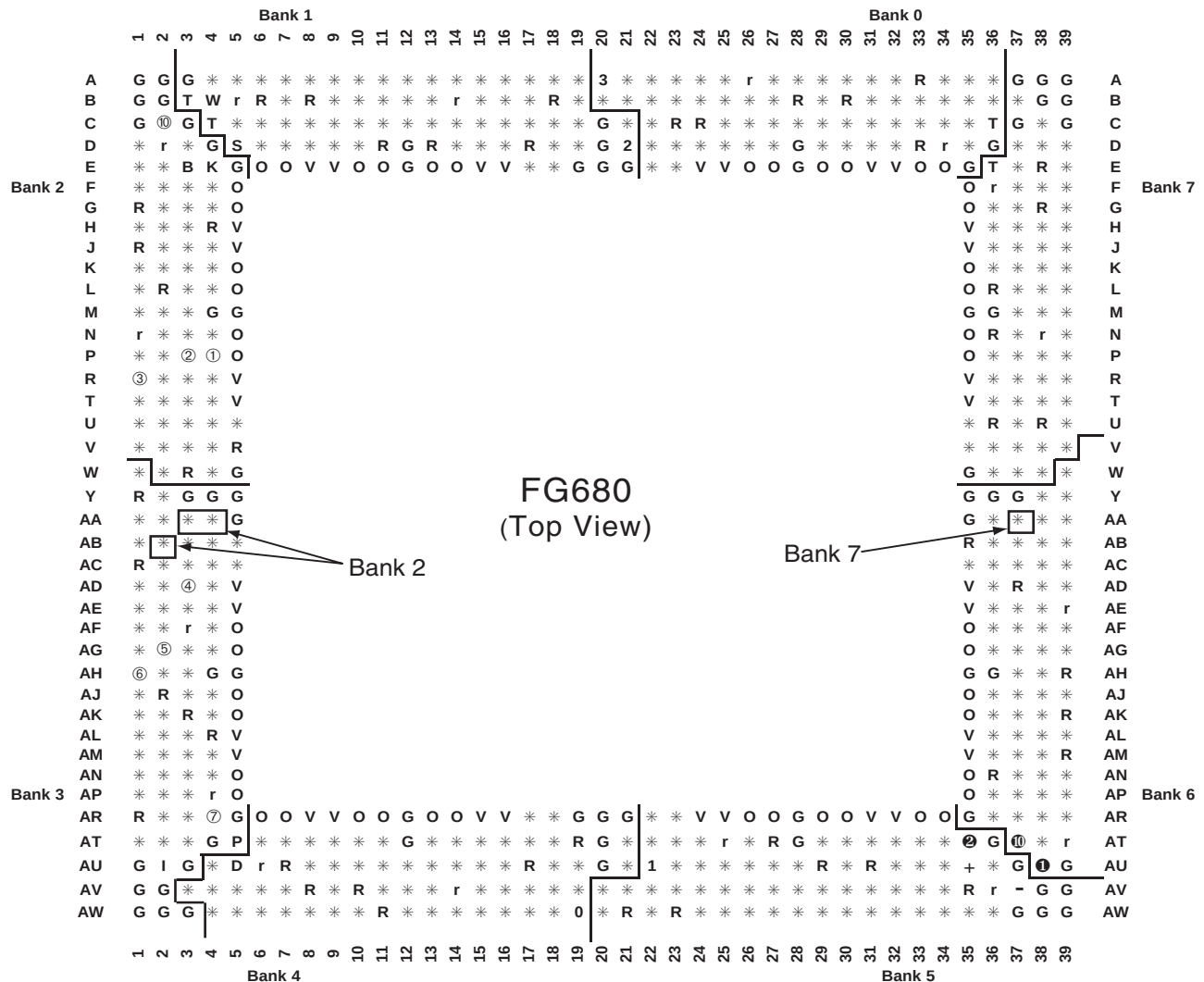
FG256 Pin Function Diagram



FG256 (Top view)

Figure 8: FG256 Pin Function Diagram

FG680 Pin Function Diagram



Note: AA3, AA4, and AB2 are in Bank 2

Note: AA37 is in Bank 7

fg680_12a

Figure 11: FG680 Pin Function Diagram