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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	1536
Number of Logic Elements/Cells	6912
Total RAM Bits	65536
Number of I/O	312
Number of Gates	322970
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xcv300-4fg456i">https://www.e-xfl.com/product-detail/xilinx/xcv300-4fg456i</a>

## General Purpose Routing

Most Virtex signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy. The general routing resources are located in horizontal and vertical routing channels associated with the rows and columns CLBs. The general-purpose routing resources are listed below.

- Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.
- 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.
- 12 buffered Hex lines route GRM signals to another GRMs six-blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines can be driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are uni-directional.

- 12 Longlines are buffered, bidirectional wires that distribute signals across the device quickly and efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

## I/O Routing

Virtex devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.

## Dedicated Routing

Some classes of signal require dedicated routing resources to maximize performance. In the Virtex architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple busses within a row, as shown in [Figure 8](#).
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.

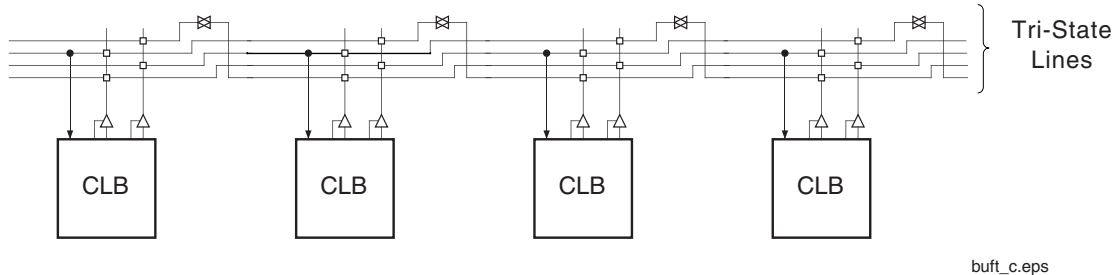


Figure 8: BUFT Connections to Dedicated Horizontal Bus Lines

## Global Routing

Global Routing resources distribute clocks and other signals with very high fanout throughout the device. Virtex devices include two tiers of global routing resources referred to as primary global and secondary local clock routing resources.

- The primary global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The primary global nets can only be driven by global buffers. There are four global buffers, one for each global net.

- The secondary local clock routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These secondary resources are more flexible than the primary resources since they are not restricted to routing only to clock pins.

## Clock Distribution

Virtex provides high-speed, low-skew clock distribution through the primary global routing resources described above. A typical clock distribution net is shown in [Figure 9](#).

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four primary global nets that in turn drive any clock pin.

ers with a common user interface regardless of their choice of entry and verification tools. The XDM software simplifies the selection of implementation options with pull-down menus and on-line help.

Application programs ranging from schematic capture to Placement and Routing (PAR) can be accessed through the XDM software. The program command sequence is generated prior to execution, and stored for documentation.

Several advanced software features facilitate Virtex design. RPMs, for example, are schematic-based macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the Xilinx FPGA Foundation development system provides interfaces to the following synthesis design environments.

- Synopsys (FPGA Compiler, FPGA Express)
- Exemplar (Spectrum)
- Synplicity (Synplify)

For schematic design entry, the Xilinx FPGA Foundation and alliance development system provides interfaces to the following schematic-capture design environments.

- Mentor Graphics V8 (Design Architect, QuickSim II)
- Viewlogic Systems (Viewdraw)

Third-party vendors support many other environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Virtex FPGAs supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The “soft macro” portion of the library contains detailed descriptions of common logic functions, but does not contain any partitioning or placement information. The performance of these macros depends, therefore, on the partitioning and placement obtained during implementation.

RPMs, on the other hand, do contain predetermined partitioning and placement information that permits optimal implementation of these functions. Users can create their own library of soft macros or RPMs based on the macros and primitives in the standard library.

The design environment supports hierarchical design entry, with high-level schematics that comprise major functional blocks, while lower-level schematics define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical

design, thus allowing the most convenient entry method to be used for each portion of the design.

## Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF net list for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floor planning.

The implementation software incorporates Timing Wizard® timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered on a schematic in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

## Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the net list for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the TRACE® static timing analyzer.

For in-circuit debugging, the development system includes a download and readback cable. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

## Configuration

Virtex devices are configured by loading configuration data into the internal configuration memory. Some of the pins used for this are dedicated configuration pins, while others can be re-used as general purpose inputs and outputs once configuration is complete.

The following are dedicated pins:

- Mode pins (M2, M1, M0)
- Configuration clock pin (CCLK)
- $\overline{\text{PROGRAM}}$  pin
- DONE pin
- Boundary-scan pins (TDI, TDO, TMS, TCK)

Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or it can be generated externally and provided to the FPGA as an input. The  $\overline{\text{PROGRAM}}$  pin must be pulled High prior to reconfiguration.

Note that some configuration pins can act as outputs. For correct operation, these pins can require a  $V_{\text{CCO}}$  of 3.3 V to permit LVTTTL operation. All the pins affected are in banks 2 or 3. The configuration pins needed for SelectMap (CS, Write) are located in bank 1.

Table 7: Configuration Codes

Configuration Mode	M2	M1	M0	CCLK Direction	Data Width	Serial D <sub>out</sub>	Configuration Pull-ups
Master-serial mode	0	0	0	Out	1	Yes	No
Boundary-scan mode	1	0	1	N/A	1	No	No
SelectMAP mode	1	1	0	In	8	No	No
Slave-serial mode	1	1	1	In	1	Yes	No
Master-serial mode	1	0	0	Out	1	Yes	Yes
Boundary-scan mode	0	0	1	N/A	1	No	Yes
SelectMAP mode	0	1	0	In	8	No	Yes
Slave-serial mode	0	1	1	In	1	Yes	Yes

### Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other source of serial configuration data. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

For more information on serial PROMs, see the PROM data sheet at:

<http://www.xilinx.com/bvdocs/publications/ds026.pdf>.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin. The data on the DOUT pin changes on the rising edge of CCLK.

The change of DOUT on the rising edge of CCLK differs from previous families, but does not cause a problem for

After Virtex devices are configured, unused IOBs function as 3-state OBUFTs with weak pull downs. For a more detailed description than that given below, see the XAPP138, Virtex Configuration and Readback.

## Configuration Modes

Virtex supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- SelectMAP mode
- Boundary-scan mode

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in Table 7.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected. However, it is recommended to drive the configuration mode pins externally.

mixed configuration chains. This change was made to improve serial configuration rates for Virtex-only chains.

Figure 12 shows a full master/slave system. A Virtex device in slave-serial mode should be connected as shown in the third device from the left.

Slave-serial mode is selected by applying <111> or <011> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave-serial the default mode if the pins are left unconnected. However, it is recommended to drive the configuration mode pins externally. Figure 13 shows slave-serial mode programming switching characteristics.

Table 8 provides more detail about the characteristics shown in Figure 13. Configuration must be delayed until the  $\overline{\text{INIT}}$  pins of all daisy-chained FPGAs are High.

## Master-Serial Mode

In master-serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM that feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge.

The interface is identical to slave-serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration. Switching to a lower frequency is prohibited.

The CCLK frequency is set using the ConfigRate option in the bitstream generation software. The maximum CCLK frequency that can be selected is 60 MHz. When selecting a CCLK frequency, ensure that the serial PROM and any

daisy-chained FPGAs are fast enough to support the clock rate.

On power-up, the CCLK frequency is 2.5 MHz. This frequency is used until the ConfigRate bits have been loaded when the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz.

Figure 12 shows a full master/slave system. In this system, the left-most device operates in master-serial mode. The remaining devices operate in slave-serial mode. The SPROM RESET pin is driven by INIT, and the CE input is driven by DONE. There is the potential for contention on the DONE pin, depending on the start-up sequence options chosen.

Figure 14 shows the timing of master-serial configuration. Master-serial mode is selected by a <000> or <100> on the mode pins (M2, M1, M0). Table 8 shows the timing information for Figure 14.

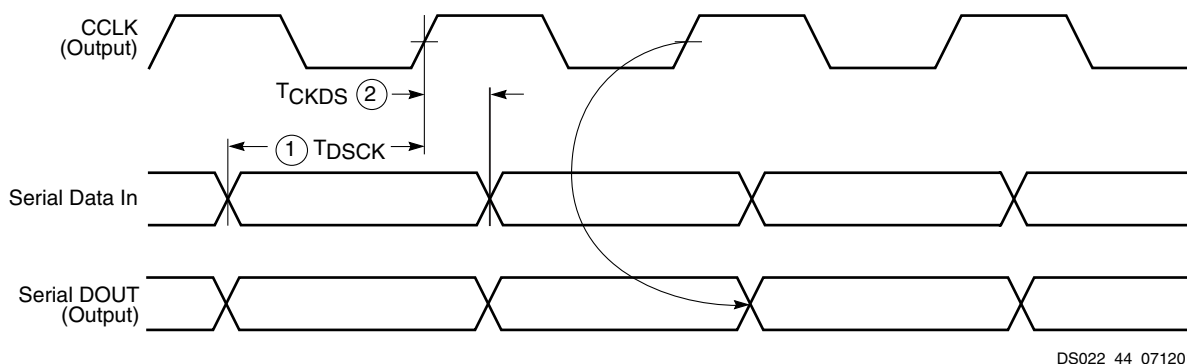


Figure 14: Master-Serial Mode Programming Switching Characteristics

At power-up,  $V_{CC}$  must rise from 1.0 V to  $V_{CC}$  min in less than 50 ms, otherwise delay configuration by pulling PROGRAM Low until  $V_{CC}$  is valid.

The sequence of operations necessary to configure a Virtex FPGA serially appears in Figure 15.

## SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the FPGA with a BUSY flag controlling the flow of data.

An external data source provides a byte stream, CCLK, a Chip Select ( $\overline{CS}$ ) signal and a Write signal ( $\overline{WRITE}$ ). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

Data can also be read using the SelectMAP mode. If  $\overline{WRITE}$  is not asserted, configuration data is read out of the FPGA as part of a readback operation.

In the SelectMAP mode, multiple Virtex devices can be chained in parallel. DATA pins (D7:D0), CCLK,  $\overline{WRITE}$ ,  $\overline{BUSY}$ ,  $\overline{PROGRAM}$ ,  $\overline{DONE}$ , and  $\overline{INIT}$  can be connected in parallel between all the FPGAs. Note that the data is organized with the MSB of each byte on pin D0 and the LSB of each byte on D7. The  $\overline{CS}$  pins are kept separate, insuring that each FPGA can be selected individually.  $\overline{WRITE}$  should be Low before loading the first bitstream and returned High after the last device has been programmed. Use  $\overline{CS}$  to select the appropriate FPGA for loading the bitstream and sending the configuration data. At the end of the bitstream, deselect the loaded device and select the next target FPGA by setting its  $\overline{CS}$  pin High. A free-running oscillator or other externally generated signal can be used for CCLK. The  $\overline{BUSY}$  signal can be ignored for frequencies below 50 MHz. For details about frequencies above 50 MHz, see XAPP138, Virtex Configuration and Readback. Once all the devices have been programmed, the  $\overline{DONE}$  pin goes High.





## Virtex™ 2.5 V Field Programmable Gate Arrays

DS003-3 (v4.0) March 1, 2013

Production Product Specification

### Virtex Electrical Characteristics

#### Definition of Terms

Electrical and switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

**Advance:** These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

**Preliminary:** These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

**Production:** These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. Contact the factory for design considerations requiring more detailed information.

**Table 1** correlates the current status of each Virtex device with a corresponding speed file designation.

**Table 1: Virtex Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XCV50			–6, –5, –4
XCV100			–6, –5, –4
XCV150			–6, –5, –4
XCV200			–6, –5, –4
XCV300			–6, –5, –4
XCV400			–6, –5, –4
XCV600			–6, –5, –4
XCV800			–6, –5, –4
XCV1000			–6, –5, –4

All specifications are subject to change without notice.

## Virtex DC Characteristics

### Absolute Maximum Ratings

Symbol	Description <sup>(1)</sup>			Units
$V_{CCINT}$	Supply voltage relative to GND <sup>(2)</sup>		–0.5 to 3.0	V
$V_{CCO}$	Supply voltage relative to GND <sup>(2)</sup>		–0.5 to 4.0	V
$V_{REF}$	Input Reference Voltage		–0.5 to 3.6	V
$V_{IN}$	Input voltage relative to GND <sup>(3)</sup>	Using $V_{REF}$	–0.5 to 3.6	V
		Internal threshold	–0.5 to 5.5	V
$V_{TS}$	Voltage applied to 3-state output		–0.5 to 5.5	V
$V_{CC}$	Longest Supply Voltage Rise Time from 1V-2.375V		50	ms
$T_{STG}$	Storage temperature (ambient)		–65 to +150	°C
$T_J$	Junction temperature <sup>(4)</sup>	Plastic Packages	+125	°C

#### Notes:

- Stresses beyond those listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time can affect device reliability.
- Power supplies can turn on in any order.
- For protracted periods (e.g., longer than a day),  $V_{IN}$  should not exceed  $V_{CCO}$  by more than 3.6 V.
- For soldering guidelines and thermal considerations, see the "Device Packaging" information on [www.xilinx.com](http://www.xilinx.com).

### Recommended Operating Conditions

Symbol	Description		Min	Max	Units
$V_{CCINT}^{(1)}$	Input Supply voltage relative to GND, $T_J = 0\text{ °C to }+85\text{ °C}$	Commercial	2.5 – 5%	2.5 + 5%	V
	Input Supply voltage relative to GND, $T_J = -40\text{ °C to }+100\text{ °C}$	Industrial	2.5 – 5%	2.5 + 5%	V
$V_{CCO}^{(4)}$	Supply voltage relative to GND, $T_J = 0\text{ °C to }+85\text{ °C}$	Commercial	1.4	3.6	V
	Supply voltage relative to GND, $T_J = -40\text{ °C to }+100\text{ °C}$	Industrial	1.4	3.6	V
$T_{IN}$	Input signal transition time			250	ns

#### Notes:

- Correct operation is guaranteed with a minimum  $V_{CCINT}$  of 2.375 V (Nominal  $V_{CCINT}$  –5%). Below the minimum value, all delay parameters increase by 3% for each 50-mV reduction in  $V_{CCINT}$  below the specified range.
- At junction temperatures above those listed as Operating Conditions, delay parameters do increase. Please refer to the TRCE report.
- Input and output measurement threshold is ~50% of  $V_{CC}$ .
- Min and Max values for  $V_{CCO}$  are I/O Standard dependant.

### DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Device	Min	Max	Units
$V_{DRINT}$	Data Retention $V_{CCINT}$ Voltage (below which configuration data can be lost)	All	2.0		V
$V_{DRIO}$	Data Retention $V_{CCO}$ Voltage (below which configuration data can be lost)	All	1.2		V
$I_{CCINTQ}$	Quiescent $V_{CCINT}$ supply current <sup>(1,3)</sup>	XCV50		50	mA
		XCV100		50	mA
		XCV150		50	mA
		XCV200		75	mA
		XCV300		75	mA
		XCV400		75	mA
		XCV600		100	mA
		XCV800		100	mA
		XCV1000		100	mA
$I_{CCOQ}$	Quiescent $V_{CCO}$ supply current <sup>(1)</sup>	XCV50		2	mA
		XCV100		2	mA
		XCV150		2	mA
		XCV200		2	mA
		XCV300		2	mA
		XCV400		2	mA
		XCV600		2	mA
		XCV800		2	mA
		XCV1000		2	mA
$I_{REF}$	$V_{REF}$ current per $V_{REF}$ pin	All		20	$\mu$ A
$I_L$	Input or output leakage current	All	-10	+10	$\mu$ A
$C_{IN}$	Input capacitance (sample tested)	BGA, PQ, HQ, packages		8	pF
$I_{RPU}$	Pad pull-up (when selected) @ $V_{in} = 0$ V, $V_{CCO} = 3.3$ V (sample tested)	All	Note (2)	0.25	mA
$I_{RPD}$	Pad pull-down (when selected) @ $V_{in} = 3.6$ V (sample tested)		Note (2)	0.15	mA

#### Notes:

1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.
3. Multiply  $I_{CCINTQ}$  limit by two for industrial grade.



### Virtex Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation net list. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Virtex devices unless otherwise noted.

### IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTTL levels. For other standards, adjust the delays with the values shown in , page 6.

Description	Device	Symbol	Speed Grade				Units
			Min	-6	-5	-4	
Propagation Delays							
Pad to I output, no delay	All	T <sub>IOPI</sub>	0.39	0.8	0.9	1.0	ns, max
Pad to I output, with delay	XCV50	T <sub>IOPID</sub>	0.8	1.5	1.7	1.9	ns, max
	XCV100		0.8	1.5	1.7	1.9	ns, max
	XCV150		0.8	1.5	1.7	1.9	ns, max
	XCV200		0.8	1.5	1.7	1.9	ns, max
	XCV300		0.8	1.5	1.7	1.9	ns, max
	XCV400		0.9	1.8	2.0	2.3	ns, max
	XCV600		0.9	1.8	2.0	2.3	ns, max
	XCV800		1.1	2.1	2.4	2.7	ns, max
	XCV1000		1.1	2.1	2.4	2.7	ns, max
Pad to output IQ via transparent latch, no delay	All	T <sub>IOPLI</sub>	0.8	1.6	1.8	2.0	ns, max
Pad to output IQ via transparent latch, with delay	XCV50	T <sub>IOPLID</sub>	1.9	3.7	4.2	4.8	ns, max
	XCV100		1.9	3.7	4.2	4.8	ns, max
	XCV150		2.0	3.9	4.3	4.9	ns, max
	XCV200		2.0	4.0	4.4	5.1	ns, max
	XCV300		2.0	4.0	4.4	5.1	ns, max
	XCV400		2.1	4.1	4.6	5.3	ns, max
	XCV600		2.1	4.2	4.7	5.4	ns, max
	XCV800		2.2	4.4	4.9	5.6	ns, max
	XCV1000		2.3	4.5	5.1	5.8	ns, max
Sequential Delays							
Clock CLK	All						
Minimum Pulse Width, High		T <sub>CH</sub>	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low		T <sub>CL</sub>	0.8	1.5	1.7	2.0	ns, min
Clock CLK to output IQ		T <sub>IOCKIQ</sub>	0.2	0.7	0.7	0.8	ns, max

### IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Description	Symbol	Standard <sup>(1)</sup>	Speed Grade				Unit s
			Min	-6	-5	-4	
Output Delay Adjustments							
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T <sub>OLVTTTL_S2</sub>	LVTTL, Slow, 2 mA	4.2	14.7	15.8	17.0	ns
	T <sub>OLVTTTL_S4</sub>	4 mA	2.5	7.5	8.0	8.6	ns
	T <sub>OLVTTTL_S6</sub>	6 mA	1.8	4.8	5.1	5.6	ns
	T <sub>OLVTTTL_S8</sub>	8 mA	1.2	3.0	3.3	3.5	ns
	T <sub>OLVTTTL_S12</sub>	12 mA	1.0	1.9	2.1	2.2	ns
	T <sub>OLVTTTL_S16</sub>	16 mA	0.9	1.7	1.9	2.0	ns
	T <sub>OLVTTTL_S24</sub>	24 mA	0.8	1.3	1.4	1.6	ns
	T <sub>OLVTTTL_F2</sub>	LVTTL, Fast, 2mA	1.9	13.1	14.0	15.1	ns
	T <sub>OLVTTTL_F4</sub>	4 mA	0.7	5.3	5.7	6.1	ns
	T <sub>OLVTTTL_F6</sub>	6 mA	0.2	3.1	3.3	3.6	ns
	T <sub>OLVTTTL_F8</sub>	8 mA	0.1	1.0	1.1	1.2	ns
	T <sub>OLVTTTL_F12</sub>	12 mA	0	0	0	0	ns
	T <sub>OLVTTTL_F16</sub>	16 mA	−0.10	−0.05	−0.05	−0.05	ns
	T <sub>OLVTTTL_F24</sub>	24 mA	−0.10	−0.20	−0.21	−0.23	ns
	T <sub>OLVCMOS2</sub>	LVC MOS2	0.10	0.10	0.11	0.12	ns
	T <sub>OPCI33_3</sub>	PCI, 33 MHz, 3.3 V	0.50	2.3	2.5	2.7	ns
	T <sub>OPCI33_5</sub>	PCI, 33 MHz, 5.0 V	0.40	2.8	3.0	3.3	ns
	T <sub>OPCI66_3</sub>	PCI, 66 MHz, 3.3 V	0.10	−0.40	−0.42	−0.46	ns
	T <sub>OGTL</sub>	GTL	0.6	0.50	0.54	0.6	ns
	T <sub>OGTLP</sub>	GTL+	0.7	0.8	0.9	1.0	ns
	T <sub>OHSTL_I</sub>	HSTL I	0.10	−0.50	−0.53	−0.5	ns
	T <sub>OHSTL_III</sub>	HSTL III	−0.10	−0.9	−0.9	−1.0	ns
	T <sub>OHSTL_IV</sub>	HSTL IV	−0.20	−1.0	−1.0	−1.1	ns
	T <sub>OSSTL2_I</sub>	SSTL2 I	−0.10	−0.50	−0.53	−0.5	ns
	T <sub>OSSTL2_II</sub>	SSTL2 II	−0.20	−0.9	−0.9	−1.0	ns
	T <sub>OSSTL3_I</sub>	SSTL3 I	−0.20	−0.50	−0.53	−0.5	ns
	T <sub>OSSTL3_II</sub>	SSTL3 II	−0.30	−1.0	−1.0	−1.1	ns
	T <sub>OCTT</sub>	CTT	0	−0.6	−0.6	−0.6	ns
	T <sub>OAGP</sub>	AGP	0	−0.9	−0.9	−1.0	ns

#### Notes:

- Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTTL. For other I/O standards and different loads, see [Table 2](#) and [Table 3](#).

## CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Combinatorial Delays						
4-input function: F/G inputs to X/Y outputs	T <sub>ILO</sub>	0.29	0.6	0.7	0.8	ns, max
5-input function: F/G inputs to F5 output	T <sub>IF5</sub>	0.32	0.7	0.8	0.9	ns, max
5-input function: F/G inputs to X output	T <sub>IF5X</sub>	0.36	0.8	0.8	1.0	ns, max
6-input function: F/G inputs to Y output via F6 MUX	T <sub>IF6Y</sub>	0.44	0.9	1.0	1.2	ns, max
6-input function: F5IN input to Y output	T <sub>F5INY</sub>	0.17	0.32	0.36	0.42	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T <sub>IFNCTL</sub>	0.31	0.7	0.7	0.8	ns, max
BY input to YB output	T <sub>BYYB</sub>	0.27	0.53	0.6	0.7	ns, max
Sequential Delays						
FF Clock CLK to XQ/YQ outputs	T <sub>CKO</sub>	0.54	1.1	1.2	1.4	ns, max
Latch Clock CLK to XQ/YQ outputs	T <sub>CKLO</sub>	0.6	1.2	1.4	1.6	ns, max
Setup and Hold Times before/after Clock CLK <sup>(1)</sup>	Setup Time / Hold Time					
4-input function: F/G Inputs	T <sub>ICK</sub> /T <sub>CKI</sub>	0.6 / 0	1.2 / 0	1.4 / 0	1.5 / 0	ns, min
5-input function: F/G inputs	T <sub>IF5CK</sub> /T <sub>CKIF5</sub>	0.7 / 0	1.3 / 0	1.5 / 0	1.7 / 0	ns, min
6-input function: F5IN input	T <sub>F5INCK</sub> /T <sub>CKF5IN</sub>	0.46 / 0	1.0 / 0	1.1 / 0	1.2 / 0	ns, min
6-input function: F/G inputs via F6 MUX	T <sub>IF6CK</sub> /T <sub>CKIF6</sub>	0.8 / 0	1.5 / 0	1.7 / 0	1.9 / 0	ns, min
BX/BY inputs	T <sub>DICK</sub> /T <sub>CKDI</sub>	0.30 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
CE input	T <sub>CECK</sub> /T <sub>CKCE</sub>	0.37 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
SR/BY inputs (synchronous)	T <sub>RCK</sub> T <sub>CKR</sub>	0.33 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T <sub>CH</sub>	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low	T <sub>CL</sub>	0.8	1.5	1.7	2.0	ns, min
Set/Reset						
Minimum Pulse Width, SR/BY inputs	T <sub>RPW</sub>	1.3	2.5	2.8	3.3	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T <sub>RQ</sub>	0.54	1.1	1.3	1.4	ns, max
Delay from GSR to XQ/YQ outputs	T <sub>IOGSRQ</sub>	4.9	9.7	10.9	12.5	ns, max
Toggle Frequency (MHz) (for export control)	F <sub>TOG</sub> (MHz)	625	333	294	250	MHz

### Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

## Global Clock Set-Up and Hold for LVTTL Standard, *without* DLL

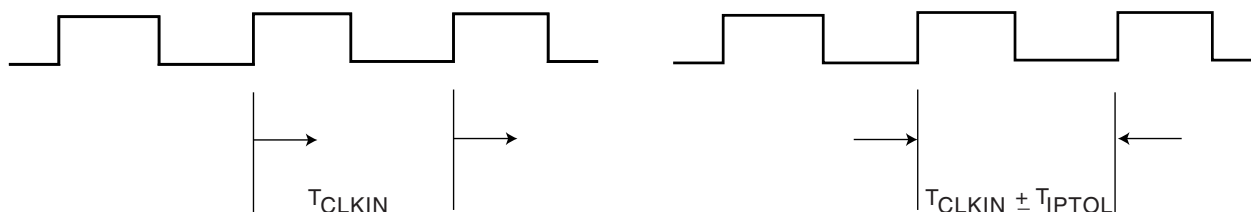
Description	Symbol	Device	Speed Grade				Units
			Min	-6	-5	-4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. <sup>(2)</sup> For data input with different standards, adjust the setup time delay by the values shown in Input Delay Adjustments.							
Full Delay Global Clock and IFF, without DLL	T <sub>PSFD</sub> /T <sub>PHFD</sub>	XCV50	0.6 / 0	2.3 / 0	2.6 / 0	2.9 / 0	ns, min
		XCV100	0.6 / 0	2.3 / 0	2.6 / 0	3.0 / 0	ns, min
		XCV150	0.6 / 0	2.4 / 0	2.7 / 0	3.1 / 0	ns, min
		XCV200	0.7 / 0	2.5 / 0	2.8 / 0	3.2 / 0	ns, min
		XCV300	0.7 / 0	2.5 / 0	2.8 / 0	3.2 / 0	ns, min
		XCV400	0.7 / 0	2.6 / 0	2.9 / 0	3.3 / 0	ns, min
		XCV600	0.7 / 0	2.6 / 0	2.9 / 0	3.3 / 0	ns, min
		XCV800	0.7 / 0	2.7 / 0	3.1 / 0	3.5 / 0	ns, min
		XCV1000	0.7 / 0	2.8 / 0	3.1 / 0	3.6 / 0	ns, min

IFF = Input Flip-Flop or Latch

**Notes: Notes:**

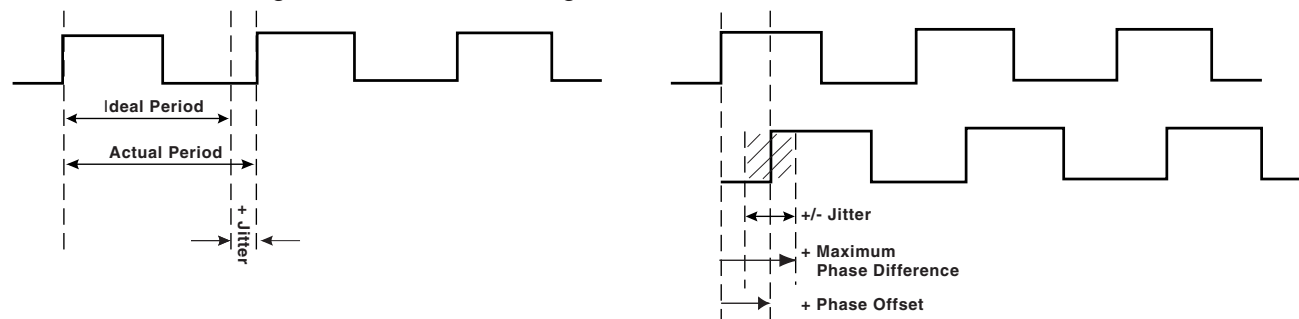
1. Set-up time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
2. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

**Period Tolerance:** the allowed input clock period change in nanoseconds.



**Output Jitter:** the difference between an ideal reference clock edge and the actual design.

**Phase Offset and Maximum Phase Difference**



ds003\_20c\_110399

Figure 1: Frequency Tolerance and Clock Jitter

## Revision History

Date	Version	Revision
11/98	1.0	Initial Xilinx release.
01/99	1.2	Updated package drawings and specs.
02/99	1.3	Update of package drawings, updated specifications.
05/99	1.4	Addition of package drawings and specifications.
05/99	1.5	Replaced FG 676 & FG680 package drawings.
07/99	1.6	Changed Boundary Scan Information and changed Figure 11, Boundary Scan Bit Sequence. Updated IOB Input & Output delays. Added Capacitance info for different I/O Standards. Added 5 V tolerant information. Added DLL Parameters and waveforms and new Pin-to-pin Input and Output Parameter tables for Global Clock Input to Output and Setup and Hold. Changed Configuration Information including Figures 12, 14, 17 & 19. Added device-dependent listings for quiescent currents ICCINTQ and ICCOQ. Updated IOB Input and Output Delays based on default standard of LVTTTL, 12 mA, Fast Slew Rate. Added IOB Input Switching Characteristics Standard Adjustments.
09/99	1.7	Speed grade update to preliminary status, Power-on specification and Clock-to-Out Minimums additions, "0" hold time listing explanation, quiescent current listing update, and Figure 6 ADDRA input label correction. Added T <sub>IJITCC</sub> parameter, changed T <sub>OJIT</sub> to T <sub>OPHASE</sub> .
01/00	1.8	Update to speed.txt file 1.96. Corrections for CRs 111036, 111137, 112697, 115479, 117153, 117154, and 117612. Modified notes for Recommended Operating Conditions (voltage and temperature). Changed Bank information for V <sub>CCO</sub> in CS144 package on p.43.

Date	Version	Revision
01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
03/00	2.0	New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration.
05/00	2.1	Modified "Pins not listed..." statement. Speed grade update to Final status.
05/00	2.2	Modified Table 18.
09/00	2.3	<ul style="list-style-type: none"> <li>Added XCV400 values to table under <b>Minimum Clock-to-Out for Virtex Devices</b>.</li> <li>Corrected Units column in table under <b>IOB Input Switching Characteristics</b>.</li> <li>Added values to table under <b>CLB SelectRAM Switching Characteristics</b>.</li> </ul>
10/00	2.4	<ul style="list-style-type: none"> <li>Corrected Pinout information for devices in the BG256, BG432, and BG560 packages in Table 18.</li> <li>Corrected <b>BG256 Pin Function Diagram</b>.</li> </ul>
04/02/01	2.5	<ul style="list-style-type: none"> <li>Revised minimums for <b>Global Clock Set-Up and Hold for LVTTTL Standard, with DLL</b>.</li> <li>Converted file to modularized format. See the <b>Virtex Data Sheet</b> section.</li> </ul>
04/19/01	2.6	<ul style="list-style-type: none"> <li>Clarified TIOCKP and TIOCKON <b>IOB Output Switching Characteristics</b> descriptors.</li> </ul>
07/19/01	2.7	<ul style="list-style-type: none"> <li>Under <b>Absolute Maximum Ratings</b>, changed (<math>T_{SOL}</math>) to 220 °C.</li> </ul>
07/26/01	2.8	<ul style="list-style-type: none"> <li>Removed <math>T_{SOL}</math> parameter and added footnote to <b>Absolute Maximum Ratings</b> table.</li> </ul>
10/29/01	2.9	<ul style="list-style-type: none"> <li>Updated the speed grade designations used in data sheets, and added <b>Table 1</b>, which shows the current speed grade designation for each device.</li> </ul>
02/01/02	3.0	<ul style="list-style-type: none"> <li>Added footnote to <b>DC Input and Output Levels</b> table.</li> </ul>
07/19/02	3.1	<ul style="list-style-type: none"> <li>Removed mention of MIL-M-38510/605 specification.</li> <li>Added link to xapp158 from the <b>Power-On Power Supply Requirements</b> section.</li> </ul>
09/10/02	3.2	<ul style="list-style-type: none"> <li>Added Clock CLK to <b>IOB Input Switching Characteristics</b> and <b>IOB Output Switching Characteristics</b>.</li> </ul>
03/01/13	4.0	The products listed in this data sheet are obsolete. See <a href="#">XCN10016</a> for further information.

## Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

- DS003-1, Virtex 2.5V FPGAs:  
Introduction and Ordering Information (Module 1)
- DS003-2, Virtex 2.5V FPGAs:  
Functional Description (Module 2)
- DS003-3, Virtex 2.5V FPGAs:  
DC and Switching Characteristics (Module 3)
- DS003-4, Virtex 2.5V FPGAs:  
Pinout Tables (Module 4)



## Virtex Pinout Information

### Pinout Tables

See [www.xilinx.com](http://www.xilinx.com) for updates or additional pinout information. For convenience, [Table 2](#), [Table 3](#) and [Table 4](#) list the locations of special-purpose and power-supply pins. Pins not listed are either user I/Os or not connected, depending on the device/package combination. See the Pinout Diagrams starting on [page 17](#) for any pins not listed for a particular part/package combination.

*Table 2: Virtex Pinout Tables (Chip-Scale and QFP Packages)*

Pin Name	Device	CS144	TQ144	PQ/HQ240
GCK0	All	K7	90	92
GCK1	All	M7	93	89
GCK2	All	A7	19	210
GCK3	All	A6	16	213
M0	All	M1	110	60
M1	All	L2	112	58
M2	All	N2	108	62
CCLK	All	B13	38	179
PROGRAM	All	L12	72	122
DONE	All	M12	74	120
INIT	All	L13	71	123
BUSY/DOUT	All	C11	39	178
D0/DIN	All	C12	40	177
D1	All	E10	45	167
D2	All	E12	47	163
D3	All	F11	51	156
D4	All	H12	59	145
D5	All	J13	63	138
D6	All	J11	65	134
D7	All	K10	70	124
WRITE	All	C10	32	185
CS	All	D10	33	184
TDI	All	A11	34	183
TDO	All	A12	36	181
TMS	All	B1	143	2
TCK	All	C3	2	239
V <sub>CCINT</sub>	All	A9, B6, C5, G3, G12, M5, M9, N6	10, 15, 25, 57, 84, 94, 99, 126	16, 32, 43, 77, 88, 104, 137, 148, 164, 198, 214, 225

Table 3: Virtex Pinout Tables (BGA) (Continued)

Pin Name	Device	BG256	BG352	BG432	BG560
<b>V<sub>CCINT</sub></b> <b>Notes:</b> <ul style="list-style-type: none"> <li>Superset includes all pins, including the ones in <b>bold</b> type. Subset excludes pins in <b>bold</b> type.</li> <li>In BG352, for XCV300 all the V<sub>CCINT</sub> pins in the superset must be connected. For XCV150/200, V<sub>CCINT</sub> pins in the subset must be connected, and pins in <b>bold</b> type can be left unconnected (these unconnected pins cannot be used as user I/O.)</li> <li>In BG432, for XCV400/600/800 all V<sub>CCINT</sub> pins in the superset must be connected. For XCV300, V<sub>CCINT</sub> pins in the subset must be connected, and pins in <b>bold</b> type can be left unconnected (these unconnected pins cannot be used as user I/O.)</li> <li>In BG560, for XCV800/1000 all V<sub>CCINT</sub> pins in the superset must be connected. For XCV400/600, V<sub>CCINT</sub> pins in the subset must be connected, and pins in <b>bold</b> type can be left unconnected (these unconnected pins cannot be used as user I/O.)</li> </ul>	XCV50/100	C10, D6, D15, F4, F17, L3, L18, R4, R17, U6, U15, V10	N/A	N/A	N/A
	XCV150/200/300	Same as above	A20, C14, D10, J24, K4, P2, P25, V24, W2, AC10, AE14, AE19, <b>B16, D12, L1, L25, R23, T1, AF11, AF16</b>	A10, A17, B23, C14, C19, K3, K29, N2, N29, T1, T29, W2, W31, AB2, AB30, AJ10, AJ16, AK13, AK19, AK22, <b>B26, C7, F1, F30, AE29, AF1, AH8, AH24</b>	N/A
	XCV400/600/800/1000	N/A	N/A	Same as above	A21, B14, B18, B28, C24, E9, E12, F2, H30, J1, K32, N1, N33, U5, U30, Y2, Y31, AD2, AD32, AG3, AG31, AK8, AK11, AK17, AK20, AL14, AL27, AN25, <b>B12, C22, M3, N29, AB2, AB32, AJ13, AL22</b>
V <sub>CCO</sub> , Bank 0	All	D7, D8	A17, B25, D19	A21, C29, D21	A22, A26, A30, B19, B32
V <sub>CCO</sub> , Bank 1	All	D13, D14	A10, D7, D13	A1, A11, D11	A10, A16, B13, C3, E5
V <sub>CCO</sub> , Bank 2	All	G17, H17	B2, H4, K1	C3, L1, L4	B2, D1, H1, M1, R2
V <sub>CCO</sub> , Bank 3	All	N17, P17	P4, U1, Y4	AA1, AA4, AJ3	V1, AA2, AD1, AK1, AL2
V <sub>CCO</sub> , Bank 4	All	U13, U14	AC8, AE2, AF10	AH11, AL1, AL11	AM2, AM15, AN4, AN8, AN12
V <sub>CCO</sub> , Bank 5	All	U7, U8	AC14, AC20, AF17	AH21, AJ29, AL21	AL31, AM21, AN18, AN24, AN30
V <sub>CCO</sub> , Bank 6	All	N4, P4	U26, W23, AE25	AA28, AA31, AL31	W32, AB33, AF33, AK33, AM32

Table 3: Virtex Pinout Tables (BGA) (Continued)

Pin Name	Device	BG256	BG352	BG432	BG560
<b>V<sub>REF</sub> Bank 3</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	M18, V20	N/A	N/A	N/A
	XCV100/150	... + R19	R4, V4, Y3	N/A	N/A
	XCV200/300	... + P18	... + AC2	V2, AB4, AD4, AF3	N/A
	XCV400	N/A	N/A	... + U2	V4, W5, AD3, AE5, AK2
	XCV600	N/A	N/A	... + AC3	... + AF1
	XCV800	N/A	N/A	... + Y3	... + AA4
	XCV1000	N/A	N/A	N/A	... + AH4
<b>V<sub>REF</sub> Bank 4</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	V12, Y18	N/A	N/A	N/A
	XCV100/150	... + W15	AC12, AE5, AE8,	N/A	N/A
	XCV200/300	... + V14	... + AE4	AJ7, AL4, AL8, AL13	N/A
	XCV400	N/A	N/A	... + AK15	AL7, AL10, AL16, AM4, AM14
	XCV600	N/A	N/A	... + AK8	... + AL9
	XCV800	N/A	N/A	... + AJ12	... + AK13
	XCV1000	N/A	N/A	N/A	... + AN3
<b>V<sub>REF</sub> Bank 5</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	V9, Y3	N/A	N/A	N/A
	XCV100/150	... + W6	AC15, AC18, AD20	N/A	N/A
	XCV200/300	... + V7	... + AE23	AJ18, AJ25, AK23, AK27	N/A
	XCV400	N/A	N/A	... + AJ17	AJ18, AJ25, AL20, AL24, AL29
	XCV600	N/A	N/A	... + AL24	... + AM26
	XCV800	N/A	N/A	... + AH19	... + AN23
	XCV1000	N/A	N/A	N/A	... + AK28
<b>V<sub>REF</sub> Bank 6</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	M2, R3	N/A	N/A	N/A
	XCV100/150	... + T1	R24, Y26, AA25,	N/A	N/A
	XCV200/300	... + T3	... + AD26	V28, AB28, AE30, AF28	N/A
	XCV400	N/A	N/A	... + U28	V29, Y32, AD31, AE29, AK32
	XCV600	N/A	N/A	... + AC28	... + AE31
	XCV800	N/A	N/A	... + Y30	... + AA30
	XCV1000	N/A	N/A	N/A	... + AH30

Table 4: Virtex Pinout Tables (Fine-Pitch BGA)

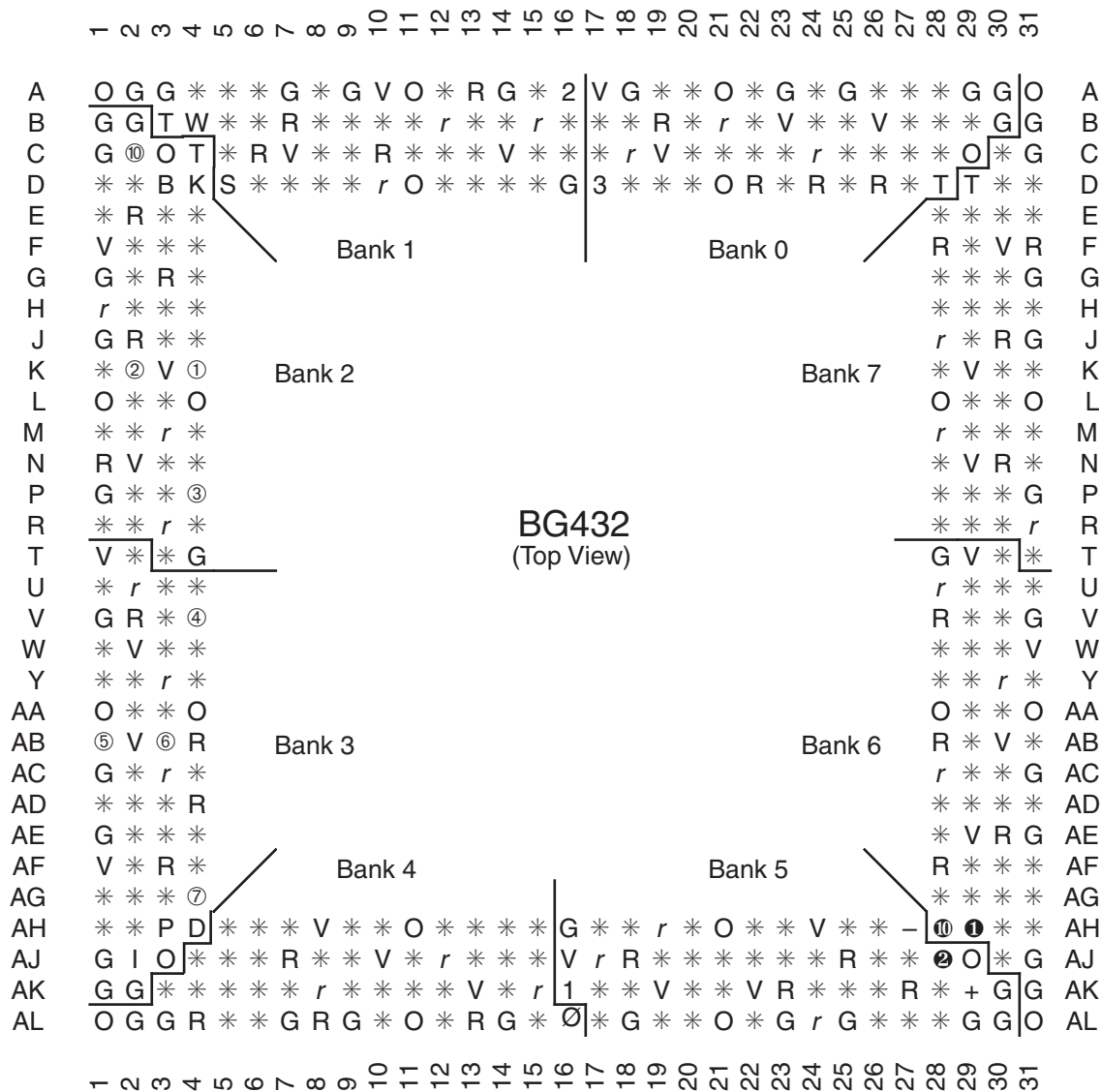
Pin Name	Device	FG256	FG456	FG676	FG680
GCK0	All	N8	W12	AA14	AW19
GCK1	All	R8	Y11	AB13	AU22
GCK2	All	C9	A11	C13	D21
GCK3	All	B8	C11	E13	A20
M0	All	N3	AB2	AD4	AT37
M1	All	P2	U5	W7	AU38
M2	All	R3	Y4	AB6	AT35
CCLK	All	D15	B22	D24	E4
PROGRAM	All	P15	W20	AA22	AT5
DONE	All	R14	Y19	AB21	AU5
INIT	All	N15	V19	Y21	AU2
BUSY/DOUT	All	C15	C21	E23	E3
D0/DIN	All	D14	D20	F22	C2
D1	All	E16	H22	K24	P4
D2	All	F15	H20	K22	P3
D3	All	G16	K20	M22	R1
D4	All	J16	N22	R24	AD3
D5	All	M16	R21	U23	AG2
D6	All	N16	T22	V24	AH1
D7	All	N14	Y21	AB23	AR4
WRITE	All	C13	A20	C22	B4
CS	All	B13	C19	E21	D5
TDI	All	A15	B20	D22	B3
TDO	All	B14	A21	C23	C4
TMS	All	D3	D3	F5	E36
TCK	All	C4	C4	E6	C36
DXN	All	R4	Y5	AB7	AV37
DXP	All	P4	V6	Y8	AU35







## BG432 Pin Function Diagram



DS003\_21\_100300

Figure 6: BG432 Pin Function Diagram