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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	2400
Number of Logic Elements/Cells	10800
Total RAM Bits	81920
Number of I/O	316
Number of Gates	468252
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	432-LBGA Exposed Pad, Metal
Supplier Device Package	432-MBGA (40x40)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xcv400-4bg432c">https://www.e-xfl.com/product-detail/xilinx/xcv400-4bg432c</a>

### Input Path

A buffer in the Virtex IOB input path routes the input signal either directly to internal logic or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signalling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage,  $V_{REF}$ . The need to supply  $V_{REF}$  imposes constraints on which standards can be used in close proximity to each other. See [I/O Banking, page 3](#).

There are optional pull-up and pull-down resistors at each user I/O input for use after configuration. Their value is in the range 50 k $\Omega$  – 100 k $\Omega$ .

### Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flop that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signalling standards. Each output buffer can source up to 24 mA and sink up to 48mA. Drive strength and slew rate controls minimize bus transients.

In most signalling standards, the output High voltage depends on an externally supplied  $V_{CCO}$  voltage. The need to supply  $V_{CCO}$  imposes constraints on which standards can be used in close proximity to each other. See [I/O Banking, page 3](#).

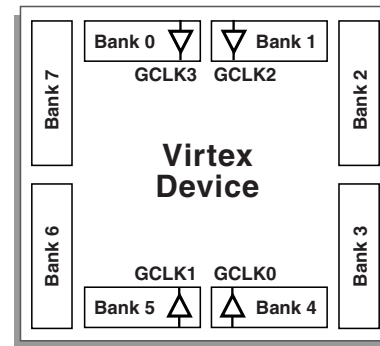
An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate  $V_{REF}$  voltage must be provided if the signalling standard requires one. The provision of this voltage must comply with the I/O banking rules.

### I/O Banking

Some of the I/O standards described above require  $V_{CCO}$  and/or  $V_{REF}$  voltages. These voltages externally and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks, as shown in [Figure 3](#). Each bank has multiple  $V_{CCO}$  pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.



X8778\_b

Figure 3: Virtex I/O Banks

Within a bank, output standards can be mixed only if they use the same  $V_{CCO}$ . Compatible standards are shown in [Table 2](#). GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on  $V_{CCO}$ .

Table 2: Compatible Output Standards

$V_{CCO}$	Compatible Standards
3.3 V	PCI, LVTTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+
2.5 V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+
1.5 V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage,  $V_{REF}$ . In this case, certain user-I/O pins are automatically configured as inputs for the  $V_{REF}$  voltage. Approximately one in six of the I/O pins in the bank assume this role.

The  $V_{REF}$  pins within a bank are interconnected internally and consequently only one  $V_{REF}$  voltage can be used within each bank. All  $V_{REF}$  pins in the bank, however, must be connected to the external voltage source for correct operation.

Within a bank, inputs that require  $V_{REF}$  can be mixed with those that do not. However, only one  $V_{REF}$  voltage can be used within a bank. Input buffers that use  $V_{REF}$  are not 5 V tolerant. LVTTTL, LVCMOS2, and PCI 33 MHz 5 V, are 5 V tolerant.

The  $V_{CCO}$  and  $V_{REF}$  pins for each bank appear in the device Pinout tables and diagrams. The diagrams also show the bank affiliation of each I/O.

Within a given package, the number of  $V_{REF}$  and  $V_{CCO}$  pins can vary depending on the size of device. In larger devices,

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is

selected either from these pads or from signals in the general purpose routing.

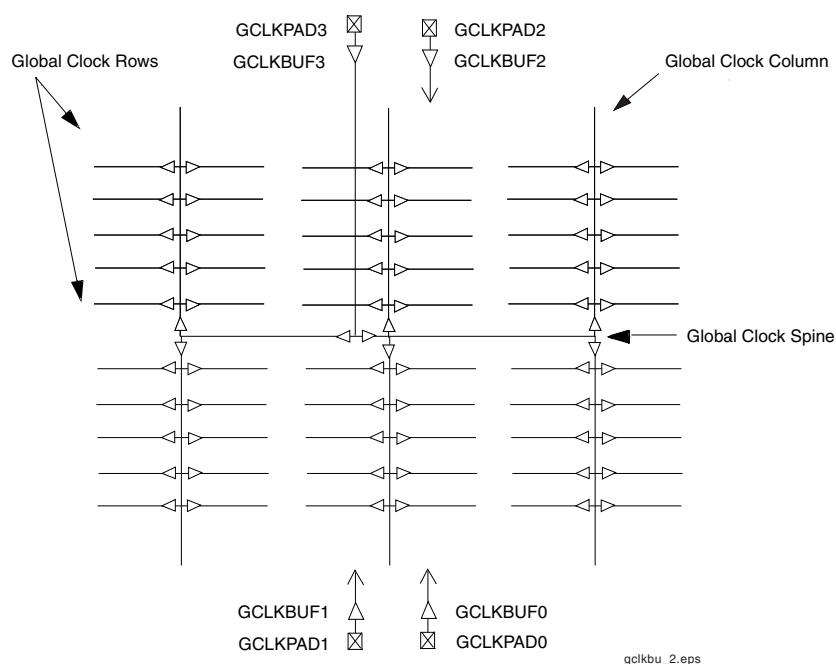


Figure 9: Global Clock Distribution Network

### Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Clock edges reach internal flip-flops one to four clock periods after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to de-skew a board level clock among multiple Virtex devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

See **DLL Timing Parameters**, page 21 of Module 3, for frequency range information.

### Boundary Scan

Virtex devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, and HIGHZ instructions. The TAP also supports two internal scan chains and configuration/readback of the device. The TAP uses dedicated package pins that always operate using LVTTTL. For TDO to operate using LVTTTL, the  $V_{CCO}$  for Bank 2 should be 3.3 V. Otherwise, TDO switches rail-to-rail between ground and  $V_{CCO}$ .

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including un-bonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections, provided the user design or application is turned off.

**Table 5** lists the boundary-scan instructions supported in Virtex FPGAs. Internal signals can be captured during EXTEST by connecting them to un-bonded or unused IOBs. They can also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Before the device is configured, all instructions except USER1 and USER2 are available. After configuration, all instructions are available. During configuration, it is recommended that those operations using the boundary-scan register (SAMPLE/PRELOAD, INTEST, EXTEST) not be performed.

ers with a common user interface regardless of their choice of entry and verification tools. The XDM software simplifies the selection of implementation options with pull-down menus and on-line help.

Application programs ranging from schematic capture to Placement and Routing (PAR) can be accessed through the XDM software. The program command sequence is generated prior to execution, and stored for documentation.

Several advanced software features facilitate Virtex design. RPMs, for example, are schematic-based macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the Xilinx FPGA Foundation development system provides interfaces to the following synthesis design environments.

- Synopsys (FPGA Compiler, FPGA Express)
- Exemplar (Spectrum)
- Synplicity (Synplify)

For schematic design entry, the Xilinx FPGA Foundation and alliance development system provides interfaces to the following schematic-capture design environments.

- Mentor Graphics V8 (Design Architect, QuickSim II)
- Viewlogic Systems (Viewdraw)

Third-party vendors support many other environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Virtex FPGAs supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The “soft macro” portion of the library contains detailed descriptions of common logic functions, but does not contain any partitioning or placement information. The performance of these macros depends, therefore, on the partitioning and placement obtained during implementation.

RPMs, on the other hand, do contain predetermined partitioning and placement information that permits optimal implementation of these functions. Users can create their own library of soft macros or RPMs based on the macros and primitives in the standard library.

The design environment supports hierarchical design entry, with high-level schematics that comprise major functional blocks, while lower-level schematics define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical

design, thus allowing the most convenient entry method to be used for each portion of the design.

## Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF net list for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floor planning.

The implementation software incorporates Timing Wizard® timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

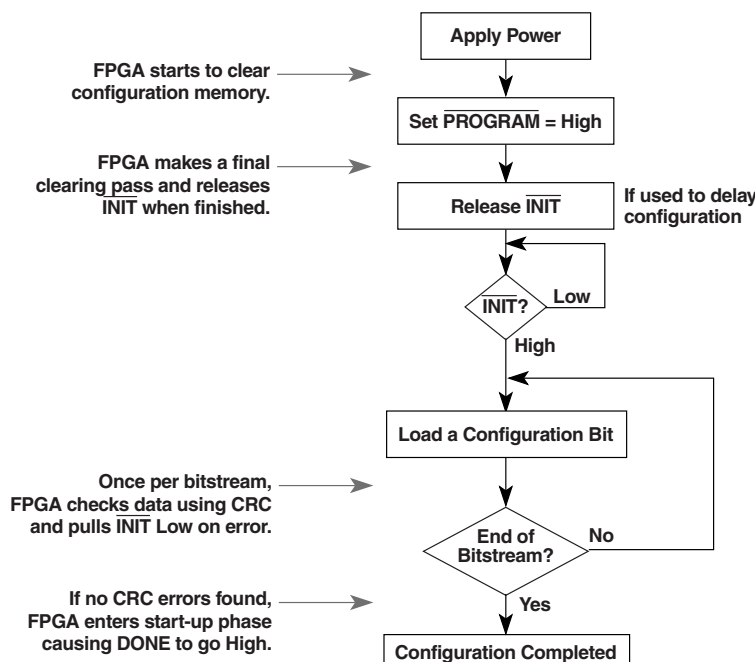
Timing requirements are entered on a schematic in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

## Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the net list for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the TRACE® static timing analyzer.

For in-circuit debugging, the development system includes a download and readback cable. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.



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Figure 15: Serial Configuration Flowchart

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained to permit high-speed 8-bit readback.

Retention of the SelectMAP port is selectable on a design-by-design basis when the bitstream is generated. If retention is selected, PROHIBIT constraints are required to prevent the SelectMAP-port pins from being used as user I/O.

Multiple Virtex FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, WRITE, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the CS pin of each device in turn and writing the appropriate data. see Table 9 for SelectMAP Write Timing Characteristics.

Table 9: SelectMAP Write Timing Characteristics

	Description		Symbol		Units
CCLK	D <sub>0-7</sub> Setup/Hold	1/2	T <sub>SMDCC</sub> /T <sub>SMCCD</sub>	5.0 / 1.7	ns, min
	$\overline{\text{CS}}$ Setup/Hold	3/4	T <sub>SMCSCC</sub> /T <sub>SMCCCS</sub>	7.0 / 1.7	ns, min
	$\overline{\text{WRITE}}$ Setup/Hold	5/6	T <sub>SMCCW</sub> /T <sub>SMWCC</sub>	7.0 / 1.7	ns, min
	BUSY Propagation Delay	7	T <sub>SMCKBY</sub>	12.0	ns, max
	Maximum Frequency		F <sub>CC</sub>	66	MHz, max
	Maximum Frequency with no handshake		F <sub>CCNH</sub>	50	MHz, max

### Write

Write operations send packets of configuration data into the FPGA. The sequence of operations for a multi-cycle write operation is shown below. Note that a configuration packet can be split into many such sequences. The packet does not have to complete within one assertion of  $\overline{\text{CS}}$ , illustrated in Figure 16.

1. Assert  $\overline{\text{WRITE}}$  and  $\overline{\text{CS}}$  Low. Note that when  $\overline{\text{CS}}$  is asserted on successive CCLKs,  $\overline{\text{WRITE}}$  must remain either asserted or de-asserted. Otherwise an abort will be initiated, as described below.
2. Drive data onto D[7:0]. Note that to avoid contention, the data source should not be enabled while  $\overline{\text{CS}}$  is Low and  $\overline{\text{WRITE}}$  is High. Similarly, while  $\overline{\text{WRITE}}$  is High, no more than one  $\overline{\text{CS}}$  should be asserted.





Figure 18: SelectMAP Write Abort Waveforms

## Boundary-Scan Mode

In the boundary-scan mode, configuration is done through the IEEE 1149.1 Test Access Port. Note that the **PROGRAM** pin must be pulled High prior to reconfiguration. A Low on the **PROGRAM** pin resets the TAP controller and no JTAG operations can be performed.

Configuration through the TAP uses the **CFG\_IN** instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port (when using TCK as a start-up clock).

1. Load the **CFG\_IN** instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the **JSTART** instruction into IR
6. Enter the SDR state
7. Clock TCK through the startup sequence
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode is selected by a <101> or 001> on the mode pins (M2, M1, M0). For details on TAP characteristics, refer to XAPP139.

## Configuration Sequence

The configuration of Virtex devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user, as described below. The configuration process can also be initiated by asserting **PROGRAM**.

The end of the memory-clearing phase is signalled by **INIT** going High, and the completion of the entire process is signalled by **DONE** going High.

The power-up timing of configuration signals is shown in Figure 19. The corresponding timing characteristics are listed in Table 10.

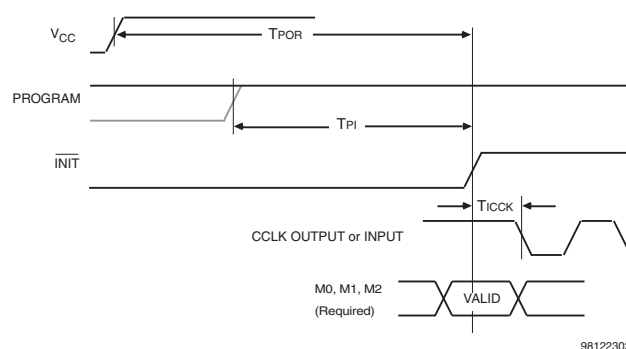


Figure 19: Power-Up Timing Configuration Signals

Table 10: Power-up Timing Characteristics

Description	Symbol	Value	Units
Power-on Reset	T <sub>POR</sub>	2.0	ms, max
Program Latency	T <sub>PL</sub>	100.0	μs, max
CCLK (output) Delay	T <sub>ICCK</sub>	0.5	μs, min
		4.0	μs, max
Program Pulse Width	T <sub>PROGRAM</sub>	300	ns, min

## Delaying Configuration

**INIT** can be held Low using an open-drain driver. An open-drain is required since **INIT** is a bidirectional open-drain pin that is held Low by the FPGA while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

## Start-Up Sequence

The default Start-up sequence is that one CCLK cycle after **DONE** goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed. In addition, the GTS, GSR, and GWE events can be made dependent on the **DONE** pins of multiple devices all going High, forcing the devices to start in synchronism. The sequence can also be paused at any stage until lock has been achieved on any or all DLLs.

Date	Version	Revision
01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
03/00	2.0	New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration.
05/00	2.1	Modified “Pins not listed...” statement. Speed grade update to Final status.
05/00	2.2	Modified Table 18.
09/00	2.3	<ul style="list-style-type: none"> <li>Added XCV400 values to table under <b>Minimum Clock-to-Out for Virtex Devices</b>.</li> <li>Corrected Units column in table under <b>IOB Input Switching Characteristics</b>.</li> <li>Added values to table under <b>CLB SelectRAM Switching Characteristics</b>.</li> </ul>
10/00	2.4	<ul style="list-style-type: none"> <li>Corrected Pinout information for devices in the BG256, BG432, and BG560 packages in Table 18.</li> <li>Corrected <b>BG256 Pin Function Diagram</b>.</li> </ul>
04/01	2.5	<ul style="list-style-type: none"> <li>Revised minimums for <b>Global Clock Set-Up and Hold for LVTTTL Standard, with DLL</b>.</li> <li>Updated SelectMAP Write Timing Characteristics values in <b>Table 9</b>.</li> <li>Converted file to modularized format. See the <b>Virtex Data Sheet</b> section.</li> </ul>
07/19/01	2.6	<ul style="list-style-type: none"> <li>Made minor edits to text under <b>Configuration</b>.</li> </ul>
07/19/02	2.7	<ul style="list-style-type: none"> <li>Made minor edit to <b>Figure 16</b> and <b>Figure 18</b>.</li> </ul>
09/10/02	2.8	<ul style="list-style-type: none"> <li>Added clarifications in the <b>Configuration</b>, <b>Boundary-Scan Mode</b>, and <b>Block SelectRAM</b> sections. Revised <b>Figure 17</b>.</li> </ul>
12/09/02	2.8.1	<ul style="list-style-type: none"> <li>Added clarification in the <b>Boundary Scan</b> section.</li> <li>Corrected number of buffered Hex lines listed in <b>General Purpose Routing</b> section.</li> </ul>
03/01/13	4.0	The products listed in this data sheet are obsolete. See <a href="#">XCN10016</a> for further information.

## Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

- DS003-1, Virtex 2.5V FPGAs:  
Introduction and Ordering Information (Module 1)
- DS003-2, Virtex 2.5V FPGAs:  
Functional Description (Module 2)
- DS003-3, Virtex 2.5V FPGAs:  
DC and Switching Characteristics (Module 3)
- DS003-4, Virtex 2.5V FPGAs:  
Pinout Tables (Module 4)



## Virtex™ 2.5 V Field Programmable Gate Arrays

DS003-3 (v4.0) March 1, 2013

Production Product Specification

### Virtex Electrical Characteristics

#### Definition of Terms

Electrical and switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

**Advance:** These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

**Preliminary:** These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

**Production:** These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. Contact the factory for design considerations requiring more detailed information.

**Table 1** correlates the current status of each Virtex device with a corresponding speed file designation.

**Table 1: Virtex Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XCV50			–6, –5, –4
XCV100			–6, –5, –4
XCV150			–6, –5, –4
XCV200			–6, –5, –4
XCV300			–6, –5, –4
XCV400			–6, –5, –4
XCV600			–6, –5, –4
XCV800			–6, –5, –4
XCV1000			–6, –5, –4

All specifications are subject to change without notice.



Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Clock CLK to Pad delay with OBUFT enabled (non-3-state)	$T_{IOCKP}$	1.0	2.9	3.2	3.5	ns, max
Clock CLK to Pad high-impedance (synchronous) <sup>(1)</sup>	$T_{IOCKHZ}$	1.1	2.3	2.5	2.9	ns, max
Clock CLK to valid data on Pad delay, plus enable delay for OBUFT	$T_{IOCKON}$	1.5	3.4	3.7	4.1	ns, max
<b>Setup and Hold Times before/after Clock CLK<sup>(2)</sup></b>		<b>Setup Time / Hold Time</b>				
O input	$T_{IOOCK}/T_{IOCKO}$	0.51 / 0	1.1 / 0	1.2 / 0	1.3 / 0	ns, min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$	0.37 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
SR input (OFF)	$T_{IOSRCKO}/T_{IOCKOSR}$	0.52 / 0	1.1 / 0	1.2 / 0	1.4 / 0	ns, min
3-State Setup Times, T input	$T_{IOTCK}/T_{IOCKT}$	0.34 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$	0.41 / 0	0.9 / 0	0.9 / 0	1.1 / 0	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$	0.49 / 0	1.0 / 0	1.1 / 0	1.3 / 0	ns, min
<b>Set/Reset Delays</b>						
SR input to Pad (asynchronous)	$T_{IOSRP}$	1.6	3.8	4.1	4.6	ns, max
SR input to Pad high-impedance (asynchronous) <sup>(1)</sup>	$T_{IOSRHZ}$	1.6	3.1	3.4	3.9	ns, max
SR input to valid data on Pad (asynchronous)	$T_{IOSRON}$	2.0	4.2	4.6	5.1	ns, max
GSR to Pad	$T_{IOGSRQ}$	4.9	9.7	10.9	12.5	ns, max

**Notes:**

1. 3-state turn-off delays should not be adjusted.
2. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

## I/O Standard Global Clock Input Adjustments

Description	Symbol	Standard <sup>(1)</sup>	Speed Grade				Units
			Min	-6	-5	-4	
Data Input Delay Adjustments							
Standard-specific global clock input delay adjustments	T <sub>GPLVTTL</sub>	LVTTL	0	0	0	0	ns, max
	T <sub>GPLVCMOS2</sub>	LVC MOS2	−0.02	−0.04	−0.04	−0.05	ns, max
	T <sub>GPPCI33_3</sub>	PCI, 33 MHz, 3.3 V	−0.05	−0.11	−0.12	−0.14	ns, max
	T <sub>GPPCI33_5</sub>	PCI, 33 MHz, 5.0 V	0.13	0.25	0.28	0.33	ns, max
	T <sub>GPPCI66_3</sub>	PCI, 66 MHz, 3.3 V	−0.05	−0.11	−0.12	−0.14	ns, max
	T <sub>GPGTL</sub>	GTL	0.7	0.8	0.9	0.9	ns, max
	T <sub>GPGTLP</sub>	GTL+	0.7	0.8	0.8	0.8	ns, max
	T <sub>GPHSTL</sub>	HSTL	0.7	0.7	0.7	0.7	ns, max
	T <sub>GPSSTL2</sub>	SSTL2	0.6	0.52	0.51	0.50	ns, max
	T <sub>GPSSTL3</sub>	SSTL3	0.6	0.6	0.55	0.54	ns, max
	T <sub>GPCTT</sub>	CTT	0.7	0.7	0.7	0.7	ns, max
	T <sub>GPAGP</sub>	AGP	0.6	0.54	0.53	0.52	ns, max

**Notes:**

1. Input timing for GPLVTTL is measured at 1.4 V. For other I/O standards, see [Table 3](#).

## CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Combinatorial Delays						
F operand inputs to X via XOR	T <sub>OPX</sub>	0.37	0.8	0.9	1.0	ns, max
F operand input to XB output	T <sub>OPXB</sub>	0.54	1.1	1.3	1.4	ns, max
F operand input to Y via XOR	T <sub>OPY</sub>	0.8	1.5	1.7	2.0	ns, max
F operand input to YB output	T <sub>OPYB</sub>	0.8	1.5	1.7	2.0	ns, max
F operand input to COUT output	T <sub>OPCYF</sub>	0.6	1.2	1.3	1.5	ns, max
G operand inputs to Y via XOR	T <sub>OPGY</sub>	0.46	1.0	1.1	1.2	ns, max
G operand input to YB output	T <sub>OPGYB</sub>	0.8	1.6	1.8	2.1	ns, max
G operand input to COUT output	T <sub>OPCYG</sub>	0.7	1.3	1.4	1.6	ns, max
BX initialization input to COUT	T <sub>BXCY</sub>	0.41	0.9	1.0	1.1	ns, max
CIN input to X output via XOR	T <sub>CINX</sub>	0.21	0.41	0.46	0.53	ns, max
CIN input to XB	T <sub>CINXB</sub>	0.02	0.04	0.05	0.06	ns, max
CIN input to Y via XOR	T <sub>CINY</sub>	0.23	0.46	0.52	0.6	ns, max
CIN input to YB	T <sub>CINYB</sub>	0.23	0.45	0.51	0.6	ns, max
CIN input to COUT output	T <sub>BYP</sub>	0.05	0.09	0.10	0.11	ns, max
Multiplier Operation						
F1/2 operand inputs to XB output via AND	T <sub>FANDXB</sub>	0.18	0.36	0.40	0.46	ns, max
F1/2 operand inputs to YB output via AND	T <sub>FANDYB</sub>	0.40	0.8	0.9	1.1	ns, max
F1/2 operand inputs to COUT output via AND	T <sub>FANDCY</sub>	0.22	0.43	0.48	0.6	ns, max
G1/2 operand inputs to YB output via AND	T <sub>GANDYB</sub>	0.25	0.50	0.6	0.7	ns, max
G1/2 operand inputs to COUT output via AND	T <sub>GANDCY</sub>	0.07	0.13	0.15	0.17	ns, max
Setup and Hold Times before/after Clock CLK <sup>(1)</sup>	Setup Time / Hold Time					
CIN input to FFX	T <sub>CCKX</sub> /T <sub>CKCX</sub>	0.50 / 0	1.0 / 0	1.2 / 0	1.3 / 0	ns, min
CIN input to FFY	T <sub>CCKY</sub> /T <sub>CKCY</sub>	0.53 / 0	1.1 / 0	1.2 / 0	1.4 / 0	ns, min

### Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Date	Version	Revision
01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
03/00	2.0	New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration.
05/00	2.1	Modified "Pins not listed..." statement. Speed grade update to Final status.
05/00	2.2	Modified Table 18.
09/00	2.3	<ul style="list-style-type: none"> <li>Added XCV400 values to table under <b>Minimum Clock-to-Out for Virtex Devices</b>.</li> <li>Corrected Units column in table under <b>IOB Input Switching Characteristics</b>.</li> <li>Added values to table under <b>CLB SelectRAM Switching Characteristics</b>.</li> </ul>
10/00	2.4	<ul style="list-style-type: none"> <li>Corrected Pinout information for devices in the BG256, BG432, and BG560 packages in Table 18.</li> <li>Corrected <b>BG256 Pin Function Diagram</b>.</li> </ul>
04/02/01	2.5	<ul style="list-style-type: none"> <li>Revised minimums for <b>Global Clock Set-Up and Hold for LVTTTL Standard, with DLL</b>.</li> <li>Converted file to modularized format. See the <b>Virtex Data Sheet</b> section.</li> </ul>
04/19/01	2.6	<ul style="list-style-type: none"> <li>Clarified TIOCKP and TIOCKON <b>IOB Output Switching Characteristics</b> descriptors.</li> </ul>
07/19/01	2.7	<ul style="list-style-type: none"> <li>Under <b>Absolute Maximum Ratings</b>, changed (<math>T_{SOL}</math>) to 220 °C.</li> </ul>
07/26/01	2.8	<ul style="list-style-type: none"> <li>Removed <math>T_{SOL}</math> parameter and added footnote to <b>Absolute Maximum Ratings</b> table.</li> </ul>
10/29/01	2.9	<ul style="list-style-type: none"> <li>Updated the speed grade designations used in data sheets, and added <b>Table 1</b>, which shows the current speed grade designation for each device.</li> </ul>
02/01/02	3.0	<ul style="list-style-type: none"> <li>Added footnote to <b>DC Input and Output Levels</b> table.</li> </ul>
07/19/02	3.1	<ul style="list-style-type: none"> <li>Removed mention of MIL-M-38510/605 specification.</li> <li>Added link to xapp158 from the <b>Power-On Power Supply Requirements</b> section.</li> </ul>
09/10/02	3.2	<ul style="list-style-type: none"> <li>Added Clock CLK to <b>IOB Input Switching Characteristics</b> and <b>IOB Output Switching Characteristics</b>.</li> </ul>
03/01/13	4.0	The products listed in this data sheet are obsolete. See <a href="#">XCN10016</a> for further information.

## Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

- DS003-1, Virtex 2.5V FPGAs:  
Introduction and Ordering Information (Module 1)
- DS003-2, Virtex 2.5V FPGAs:  
Functional Description (Module 2)
- DS003-3, Virtex 2.5V FPGAs:  
DC and Switching Characteristics (Module 3)
- DS003-4, Virtex 2.5V FPGAs:  
Pinout Tables (Module 4)

Table 3: Virtex Pinout Tables (BGA) (Continued)

Pin Name	Device	BG256	BG352	BG432	BG560
<b>V<sub>CCINT</sub></b> <b>Notes:</b> <ul style="list-style-type: none"> <li>Superset includes all pins, including the ones in <b>bold</b> type. Subset excludes pins in <b>bold</b> type.</li> <li>In BG352, for XCV300 all the V<sub>CCINT</sub> pins in the superset must be connected. For XCV150/200, V<sub>CCINT</sub> pins in the subset must be connected, and pins in <b>bold</b> type can be left unconnected (these unconnected pins cannot be used as user I/O.)</li> <li>In BG432, for XCV400/600/800 all V<sub>CCINT</sub> pins in the superset must be connected. For XCV300, V<sub>CCINT</sub> pins in the subset must be connected, and pins in <b>bold</b> type can be left unconnected (these unconnected pins cannot be used as user I/O.)</li> <li>In BG560, for XCV800/1000 all V<sub>CCINT</sub> pins in the superset must be connected. For XCV400/600, V<sub>CCINT</sub> pins in the subset must be connected, and pins in <b>bold</b> type can be left unconnected (these unconnected pins cannot be used as user I/O.)</li> </ul>	XCV50/100	C10, D6, D15, F4, F17, L3, L18, R4, R17, U6, U15, V10	N/A	N/A	N/A
	XCV150/200/300	Same as above	A20, C14, D10, J24, K4, P2, P25, V24, W2, AC10, AE14, AE19, <b>B16, D12, L1, L25, R23, T1, AF11, AF16</b>	A10, A17, B23, C14, C19, K3, K29, N2, N29, T1, T29, W2, W31, AB2, AB30, AJ10, AJ16, AK13, AK19, AK22, <b>B26, C7, F1, F30, AE29, AF1, AH8, AH24</b>	N/A
	XCV400/600/800/1000	N/A	N/A	Same as above	A21, B14, B18, B28, C24, E9, E12, F2, H30, J1, K32, N1, N33, U5, U30, Y2, Y31, AD2, AD32, AG3, AG31, AK8, AK11, AK17, AK20, AL14, AL27, AN25, <b>B12, C22, M3, N29, AB2, AB32, AJ13, AL22</b>
V <sub>CCO</sub> , Bank 0	All	D7, D8	A17, B25, D19	A21, C29, D21	A22, A26, A30, B19, B32
V <sub>CCO</sub> , Bank 1	All	D13, D14	A10, D7, D13	A1, A11, D11	A10, A16, B13, C3, E5
V <sub>CCO</sub> , Bank 2	All	G17, H17	B2, H4, K1	C3, L1, L4	B2, D1, H1, M1, R2
V <sub>CCO</sub> , Bank 3	All	N17, P17	P4, U1, Y4	AA1, AA4, AJ3	V1, AA2, AD1, AK1, AL2
V <sub>CCO</sub> , Bank 4	All	U13, U14	AC8, AE2, AF10	AH11, AL1, AL11	AM2, AM15, AN4, AN8, AN12
V <sub>CCO</sub> , Bank 5	All	U7, U8	AC14, AC20, AF17	AH21, AJ29, AL21	AL31, AM21, AN18, AN24, AN30
V <sub>CCO</sub> , Bank 6	All	N4, P4	U26, W23, AE25	AA28, AA31, AL31	W32, AB33, AF33, AK33, AM32

*Table 3: Virtex Pinout Tables (BGA) (Continued)*

Pin Name	Device	BG256	BG352	BG432	BG560
V <sub>CCO</sub> , Bank 7	All	G4, H4	G23, K26, N23	A31, L28, L31	C32, D33, K33, N32, T33
V <sub>REF</sub> Bank 0 (VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	A8, B4	N/A	N/A	N/A
	XCV100/150	... + A4	A16, C19, C21	N/A	N/A
	XCV200/300	... + A2	... + D21	B19, D22, D24, D26	N/A
	XCV400	N/A	N/A	... + C18	A19, D20, D26, E23, E27
	XCV600	N/A	N/A	... + C24	... + E24
	XCV800	N/A	N/A	... + B21	... + E21
	XCV1000	N/A	N/A	N/A	... + D29
V <sub>REF</sub> Bank 1 (VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	A17, B12	N/A	N/A	N/A
	XCV100/150	... + B15	B6, C9, C12	N/A	N/A
	XCV200/300	... + B17	... + D6	A13, B7, C6, C10	N/A
	XCV400	N/A	N/A	... + B15	A6, D7, D11, D16, E15
	XCV600	N/A	N/A	... + D10	... + D10
	XCV800	N/A	N/A	... + B12	... + D13
	XCV1000	N/A	N/A	N/A	... + E7
V <sub>REF</sub> Bank 2 (VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	C20, J18	N/A	N/A	N/A
	XCV100/150	... + F19	E2, H2, M4	N/A	N/A
	XCV200/300	... + G18	... + D2	E2, G3, J2, N1	N/A
	XCV400	N/A	N/A	... + R3	G5, H4, L5, P4, R1
	XCV600	N/A	N/A	... + H1	... + K5
	XCV800	N/A	N/A	... + M3	... + N5
	XCV1000	N/A	N/A	N/A	... + B3



Table 3: Virtex Pinout Tables (BGA) (Continued)

Pin Name	Device	BG256	BG352	BG432	BG560
<b>V<sub>REF</sub> Bank 7</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	G3, H1	N/A	N/A	N/A
	XCV100/150	... + D1	D26, G26, L26	N/A	N/A
	XCV200/300	... + B2	... + E24	F28, F31, J30, N30	N/A
	XCV400	N/A	N/A	... + R31	E31, G31, K31, P31, T31
	XCV600	N/A	N/A	... + J28	... + H32
	XCV800	N/A	N/A	... + M28	... + L33
	XCV1000	N/A	N/A	N/A	... + D31
GND	All	C3, C18, D4, D5, D9, D10, D11, D12, D16, D17, E4, E17, J4, J17, K4, K17, L4, L17, M4, M17, T4, T17, U4, U5, U9, U10, U11, U12, U16, U17, V3, V18	A1, A2, A5, A8, A14, A19, A22, A25, A26, B1, B26, E1, E26, H1, H26, N1, P26, W1, W26, AB1, AB26, AE1, AE26, AF1, AF2, AF5, AF8, AF13, AF19, AF22, AF25, AF26	A2, A3, A7, A9, A14, A18, A23, A25, A29, A30, B1, B2, B30, B31, C1, C31, D16, G1, G31, J1, J31, P1, P31, T4, T28, V1, V31, AC1, AC31, AE1, AE31, AH16, AJ1, AJ31, AK1, AK2, AK30, AK31, AL2, AL3, AL7, AL9, AL14, AL18, AL23, AL25, AL29, AL30	A1, A7, A12, A14, A18, A20, A24, A29, A32, A33, B1, B6, B9, B15, B23, B27, B31, C2, E1, F32, G2, G33, J32, K1, L2, M33, P1, P33, R32, T1, V33, W2, Y1, Y33, AB1, AC32, AD33, AE2, AG1, AG32, AH2, AJ33, AL32, AM3, AM7, AM11, AM19, AM25, AM28, AM33, AN1, AN2, AN5, AN10, AN14, AN16, AN20, AN22, AN27, AN33
GND <sup>(1)</sup>	All	J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12	N/A	N/A	N/A
No Connect	All	N/A	N/A	N/A	C31, AC2, AK4, AL3

**Notes:**

1. 16 extra balls (grounded) at package center.

Table 4: Virtex Pinout Tables (Fine-Pitch BGA)

Pin Name	Device	FG256	FG456	FG676	FG680
GCK0	All	N8	W12	AA14	AW19
GCK1	All	R8	Y11	AB13	AU22
GCK2	All	C9	A11	C13	D21
GCK3	All	B8	C11	E13	A20
M0	All	N3	AB2	AD4	AT37
M1	All	P2	U5	W7	AU38
M2	All	R3	Y4	AB6	AT35
CCLK	All	D15	B22	D24	E4
PROGRAM	All	P15	W20	AA22	AT5
DONE	All	R14	Y19	AB21	AU5
INIT	All	N15	V19	Y21	AU2
BUSY/DOUT	All	C15	C21	E23	E3
D0/DIN	All	D14	D20	F22	C2
D1	All	E16	H22	K24	P4
D2	All	F15	H20	K22	P3
D3	All	G16	K20	M22	R1
D4	All	J16	N22	R24	AD3
D5	All	M16	R21	U23	AG2
D6	All	N16	T22	V24	AH1
D7	All	N14	Y21	AB23	AR4
WRITE	All	C13	A20	C22	B4
CS	All	B13	C19	E21	D5
TDI	All	A15	B20	D22	B3
TDO	All	B14	A21	C23	C4
TMS	All	D3	D3	F5	E36
TCK	All	C4	C4	E6	C36
DXN	All	R4	Y5	AB7	AV37
DXP	All	P4	V6	Y8	AU35

## Pinout Diagrams

The following diagrams, **CS144 Pin Function Diagram**, page 17 through **FG680 Pin Function Diagram**, page 27, illustrate the locations of special-purpose pins on Virtex FPGAs. Table 5 lists the symbols used in these diagrams. The diagrams also show I/O-bank boundaries.

Table 5: Pinout Diagram Symbols

Symbol	Pin Function
*	General I/O
*	Device-dependent general I/O, n/c on smaller devices
V	V <sub>CCINT</sub>
v	Device-dependent V <sub>CCINT</sub> , n/c on smaller devices
O	V <sub>CCO</sub>
R	V <sub>REF</sub>
r	Device-dependent V <sub>REF</sub> , remains I/O on smaller devices
G	Ground
Ø, 1, 2, 3	Global Clocks

Table 5: Pinout Diagram Symbols (Continued)

Symbol	Pin Function
⑩, ①, ②	M0, M1, M2
⑩, ①, ②, ③, ④, ⑤, ⑥, ⑦	D0/DIN, D1, D2, D3, D4, D5, D6, D7
B	DOUT/BUSY
D	DONE
P	PROGRAM
I	INIT
K	CCLK
W	WRITE
S	CS
T	Boundary-scan Test Access Port
+	Temperature diode, anode
–	Temperature diode, cathode
n	No connect

## CS144 Pin Function Diagram

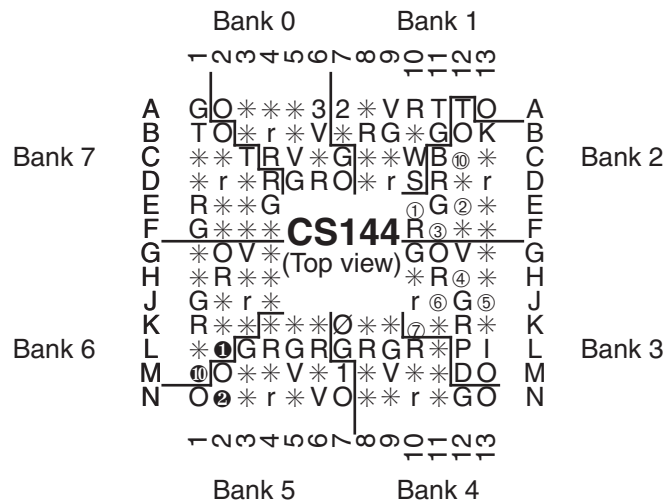
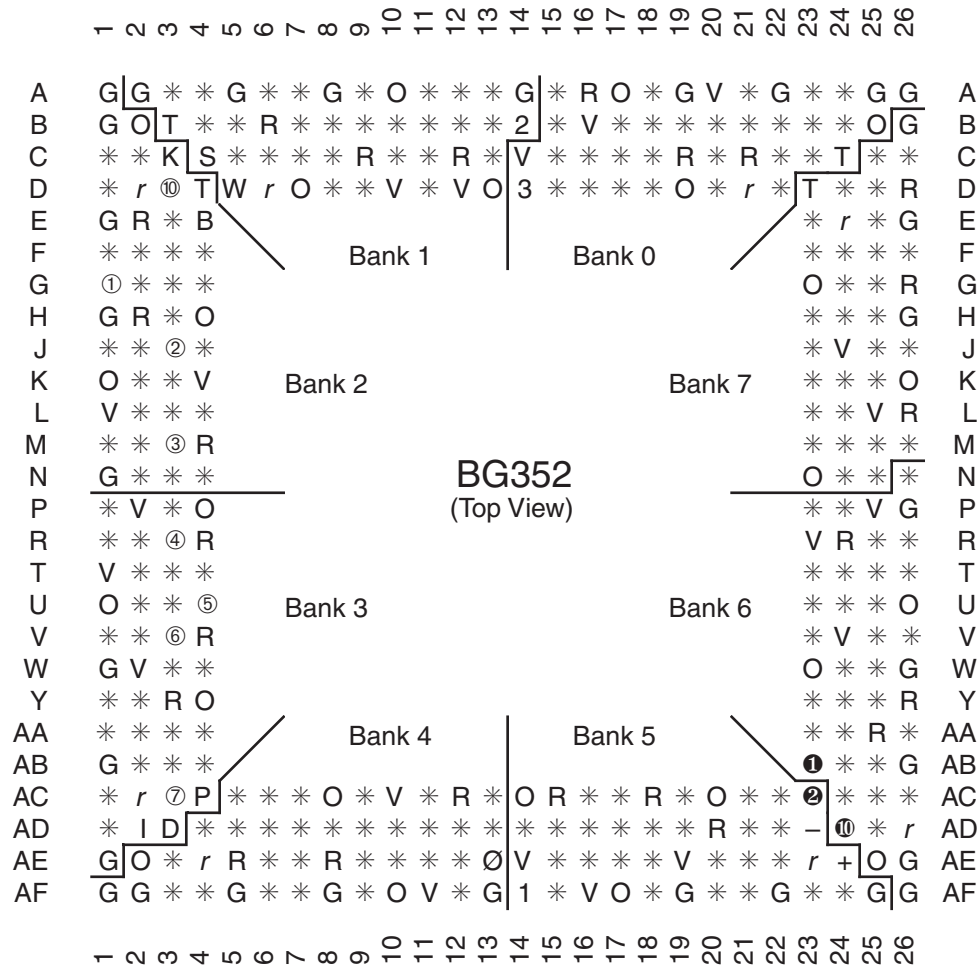


Figure 1: CS144 Pin Function Diagram

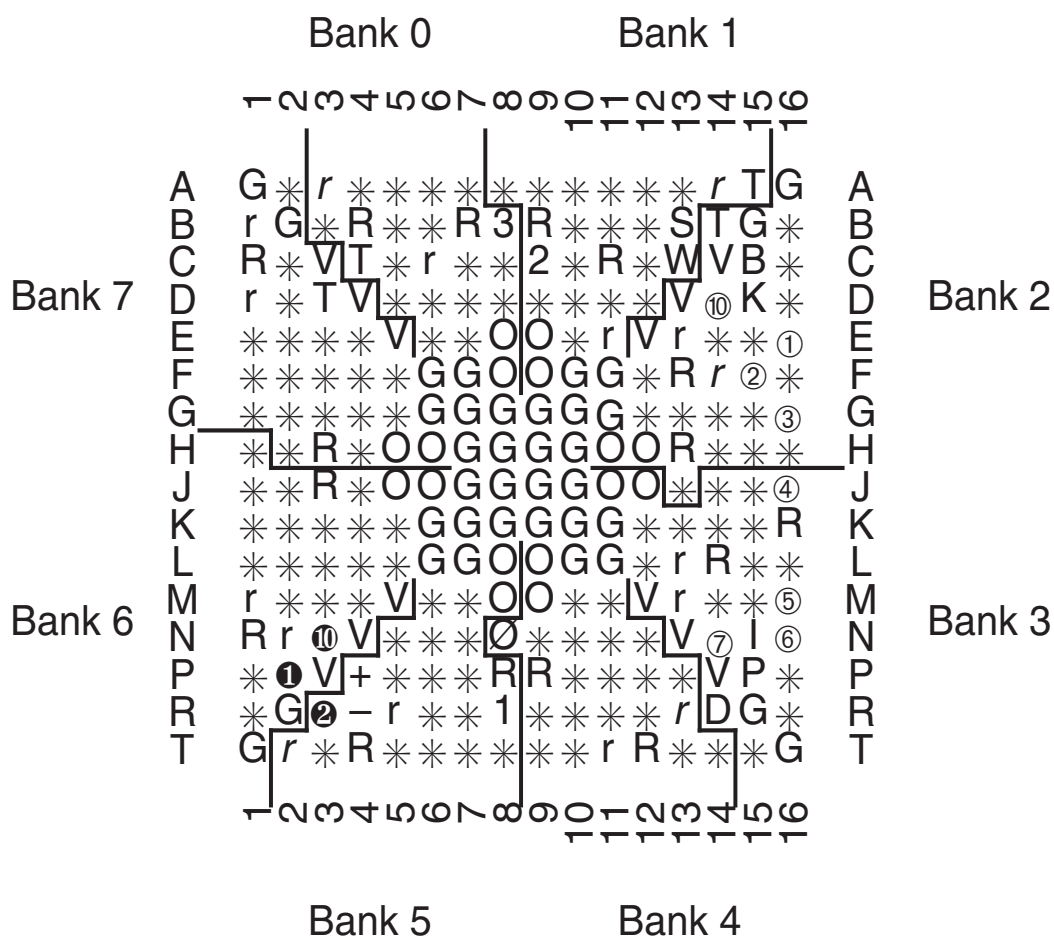
## BG352 Pin Function Diagram



DS003\_19\_100600

Figure 5: BG352 Pin Function Diagram

## FG256 Pin Function Diagram

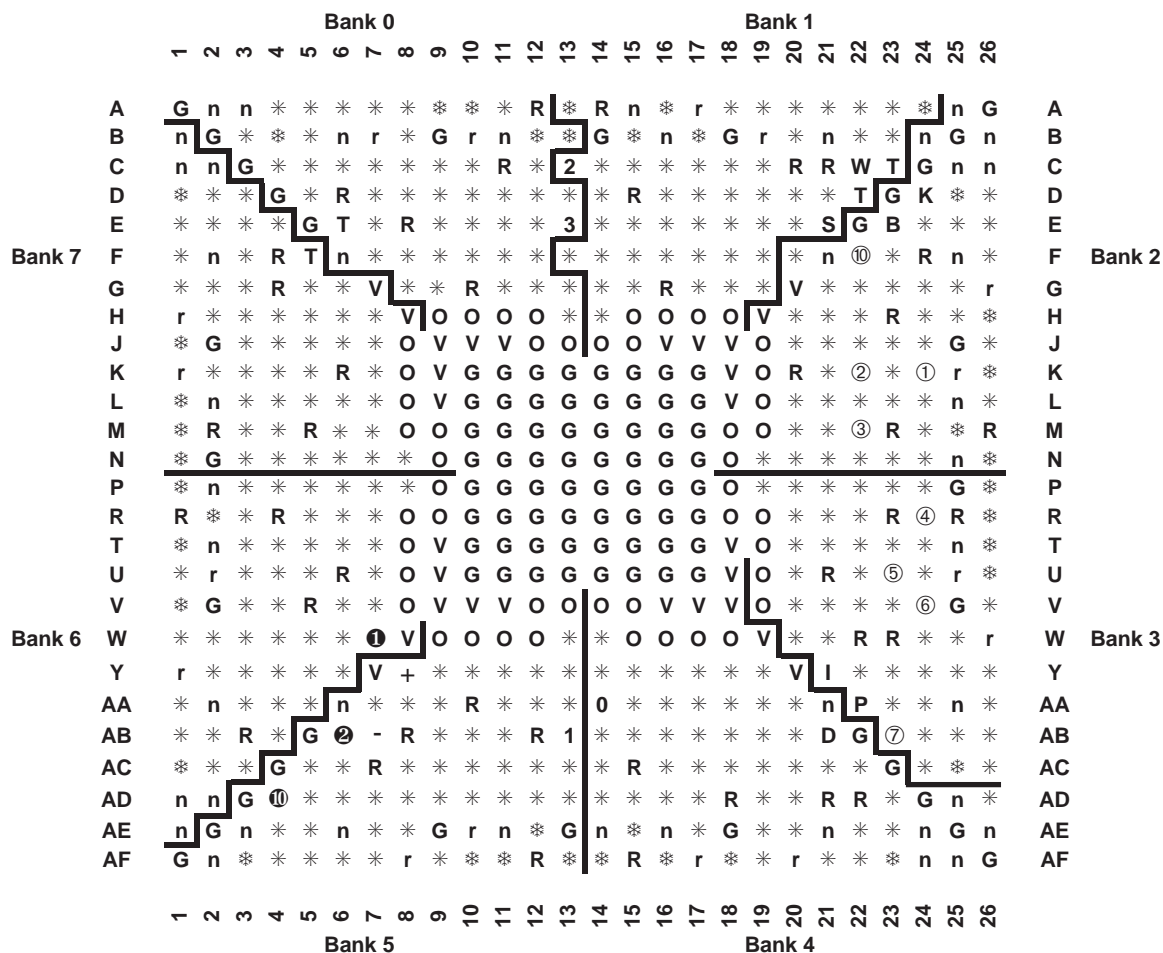


## FG256

(Top view)

Figure 8: FG256 Pin Function Diagram

## FG676 Pin Function Diagram



**FG676**  
(Top view)

fg676a

Figure 10: FG676 Pin Function Diagram

**Notes:**

Packages FG456 and FG676 are layout compatible.



