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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	2400
Number of Logic Elements/Cells	10800
Total RAM Bits	81920
Number of I/O	404
Number of Gates	468252
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	560-LBGA Exposed Pad, Metal
Supplier Device Package	560-MBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv400-4bg560i

Virtex Device/Package Combinations and Maximum I/O

Table 3: Virtex Family Maximum User I/O by Device/Package (Excluding Dedicated Clock Pins)

Package	XCV50	XCV100	XCV150	XCV200	XCV300	XCV400	XCV600	XCV800	XCV1000
CS144	94	94							
TQ144	98	98							
PQ240	166	166	166	166	166				
HQ240						166	166	166	
BG256	180	180	180	180					
BG352			260	260	260				
BG432					316	316	316	316	
BG560						404	404	404	404
FG256	176	176	176	176					
FG456			260	284	312				
FG676						404	444	444	
FG680							512	512	512

Virtex Ordering Information



Figure 1: Virtex Ordering Information

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is

selected either from these pads or from signals in the general purpose routing.

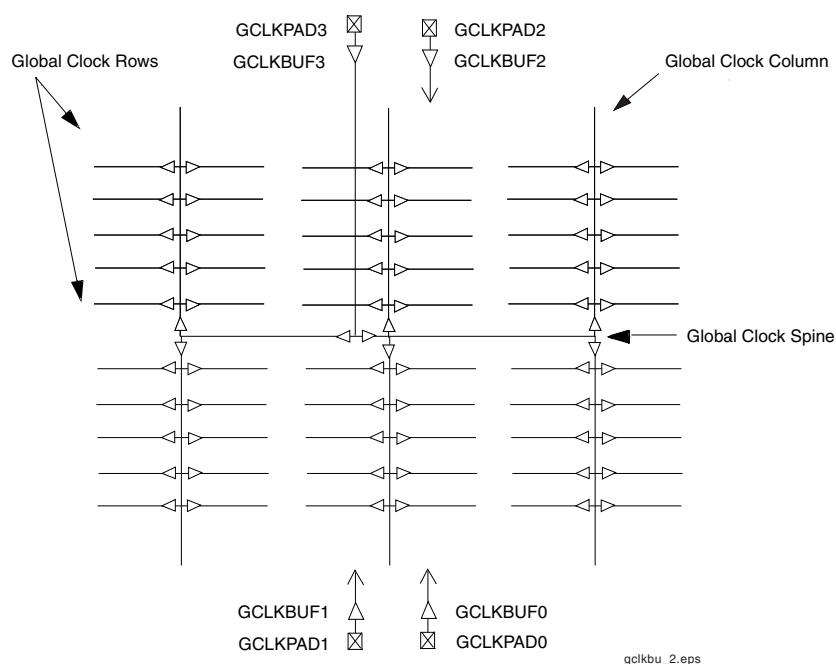


Figure 9: Global Clock Distribution Network

Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Clock edges reach internal flip-flops one to four clock periods after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to de-skew a board level clock among multiple Virtex devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

See **DLL Timing Parameters**, page 21 of Module 3, for frequency range information.

Boundary Scan

Virtex devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, and HIGHZ instructions. The TAP also supports two internal scan chains and configuration/readback of the device. The TAP uses dedicated package pins that always operate using LVTTTL. For TDO to operate using LVTTTL, the V_{CCO} for Bank 2 should be 3.3 V. Otherwise, TDO switches rail-to-rail between ground and V_{CCO} .

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including un-bonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections, provided the user design or application is turned off.

Table 5 lists the boundary-scan instructions supported in Virtex FPGAs. Internal signals can be captured during EXTEST by connecting them to un-bonded or unused IOBs. They can also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Before the device is configured, all instructions except USER1 and USER2 are available. After configuration, all instructions are available. During configuration, it is recommended that those operations using the boundary-scan register (SAMPLE/PRELOAD, INTEST, EXTEST) not be performed.

Configuration

Virtex devices are configured by loading configuration data into the internal configuration memory. Some of the pins used for this are dedicated configuration pins, while others can be re-used as general purpose inputs and outputs once configuration is complete.

The following are dedicated pins:

- Mode pins (M2, M1, M0)
- Configuration clock pin (CCLK)
- $\overline{\text{PROGRAM}}$ pin
- DONE pin
- Boundary-scan pins (TDI, TDO, TMS, TCK)

Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or it can be generated externally and provided to the FPGA as an input. The $\overline{\text{PROGRAM}}$ pin must be pulled High prior to reconfiguration.

Note that some configuration pins can act as outputs. For correct operation, these pins can require a V_{CCO} of 3.3 V to permit LVTTTL operation. All the pins affected are in banks 2 or 3. The configuration pins needed for SelectMap (CS, Write) are located in bank 1.

Table 7: Configuration Codes

Configuration Mode	M2	M1	M0	CCLK Direction	Data Width	Serial D _{out}	Configuration Pull-ups
Master-serial mode	0	0	0	Out	1	Yes	No
Boundary-scan mode	1	0	1	N/A	1	No	No
SelectMAP mode	1	1	0	In	8	No	No
Slave-serial mode	1	1	1	In	1	Yes	No
Master-serial mode	1	0	0	Out	1	Yes	Yes
Boundary-scan mode	0	0	1	N/A	1	No	Yes
SelectMAP mode	0	1	0	In	8	No	Yes
Slave-serial mode	0	1	1	In	1	Yes	Yes

Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other source of serial configuration data. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

For more information on serial PROMs, see the PROM data sheet at:

<http://www.xilinx.com/bvdocs/publications/ds026.pdf>.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin. The data on the DOUT pin changes on the rising edge of CCLK.

The change of DOUT on the rising edge of CCLK differs from previous families, but does not cause a problem for

After Virtex devices are configured, unused IOBs function as 3-state OBUFTs with weak pull downs. For a more detailed description than that given below, see the XAPP138, Virtex Configuration and Readback.

Configuration Modes

Virtex supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- SelectMAP mode
- Boundary-scan mode

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in Table 7.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected. However, it is recommended to drive the configuration mode pins externally.

mixed configuration chains. This change was made to improve serial configuration rates for Virtex-only chains.

Figure 12 shows a full master/slave system. A Virtex device in slave-serial mode should be connected as shown in the third device from the left.

Slave-serial mode is selected by applying <111> or <011> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave-serial the default mode if the pins are left unconnected. However, it is recommended to drive the configuration mode pins externally. Figure 13 shows slave-serial mode programming switching characteristics.

Table 8 provides more detail about the characteristics shown in Figure 13. Configuration must be delayed until the $\overline{\text{INIT}}$ pins of all daisy-chained FPGAs are High.



Virtex™ 2.5 V Field Programmable Gate Arrays

DS003-3 (v4.0) March 1, 2013

Production Product Specification

Virtex Electrical Characteristics

Definition of Terms

Electrical and switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. Contact the factory for design considerations requiring more detailed information.

Table 1 correlates the current status of each Virtex device with a corresponding speed file designation.

Table 1: Virtex Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XCV50			–6, –5, –4
XCV100			–6, –5, –4
XCV150			–6, –5, –4
XCV200			–6, –5, –4
XCV300			–6, –5, –4
XCV400			–6, –5, –4
XCV600			–6, –5, –4
XCV800			–6, –5, –4
XCV1000			–6, –5, –4

All specifications are subject to change without notice.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device⁽¹⁾ from 0 V. The current is highest at the fastest suggested ramp rate (0 V to nominal voltage in 2 ms) and is lowest at the slowest allowed ramp rate (0 V to nominal voltage in 50 ms). For more details on power supply requirements, see Application Note XAPP158 on www.xilinx.com.

Product	Description ⁽²⁾	Current Requirement ^(1,3)
Virtex Family, Commercial Grade	Minimum required current supply	500 mA
Virtex Family, Industrial Grade	Minimum required current supply	2 A

Notes:

- Ramp rate used for this specification is from 0 - 2.7 VDC. Peak current occurs on or near the internal power-on reset threshold of 1.0V and lasts for less than 3 ms.
- Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
- Larger currents can result if ramp rates are forced to be faster.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed output currents over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} for each standard with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTL ⁽¹⁾	-0.5	0.8	2.0	5.5	0.4	2.4	24	-24
LVC MOS2	-0.5	.7	1.7	5.5	0.4	1.9	12	-12
PCI, 3.3 V	-0.5	44% V_{CCINT}	60% V_{CCINT}	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI, 5.0 V	-0.5	0.8	2.0	5.5	0.55	2.4	Note 2	Note 2
GTL	-0.5	$V_{REF} - 0.05$	$V_{REF} + 0.05$	3.6	0.4	n/a	40	n/a
GTL+	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.6	n/a	36	n/a
HSTL I ⁽³⁾	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	8	-8
HSTL III	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	24	-8
HSTL IV	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	48	-8
SSTL3 I	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.6$	$V_{REF} + 0.6$	8	-8
SSTL3 II	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.8$	$V_{REF} + 0.8$	16	-16
SSTL2 I	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.61$	$V_{REF} + 0.61$	7.6	-7.6
SSTL2 II	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.80$	$V_{REF} + 0.80$	15.2	-15.2
CTT	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
AGP	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Notes:

- V_{OL} and V_{OH} for lower drive currents are sample tested.
- Tested according to the relevant specifications.
- DC input and output levels for HSTL18 (HSTL I/O standard with V_{CCO} of 1.8 V) are provided in an HSTL white paper on www.xilinx.com.

IOB Input Switching Characteristics Standard Adjustments

Description	Symbol	Standard ⁽¹⁾	Speed Grade				Units
			Min	-6	-5	-4	
Data Input Delay Adjustments							
Standard-specific data input delay adjustments	T _{ILVTTL}	LVTTL	0	0	0	0	ns
	T _{ILVCMOS2}	LVC MOS2	−0.02	−0.04	−0.04	−0.05	ns
	T _{IPCI33_3}	PCI, 33 MHz, 3.3 V	−0.05	−0.11	−0.12	−0.14	ns
	T _{IPCI33_5}	PCI, 33 MHz, 5.0 V	0.13	0.25	0.28	0.33	ns
	T _{IPCI66_3}	PCI, 66 MHz, 3.3 V	−0.05	−0.11	−0.12	−0.14	ns
	T _{IGTL}	GTL	0.10	0.20	0.23	0.26	ns
	T _{IGTLP}	GTL+	0.06	0.11	0.12	0.14	ns
	T _{IHSTL}	HSTL	0.02	0.03	0.03	0.04	ns
	T _{ISSTL2}	SSTL2	−0.04	−0.08	−0.09	−0.10	ns
	T _{ISSTL3}	SSTL3	−0.02	−0.04	−0.05	−0.06	ns
	T _{ICTT}	CTT	0.01	0.02	0.02	0.02	ns
	T _{IAGP}	AGP	−0.03	−0.06	−0.07	−0.08	ns

Notes:

- Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see [Table 3](#).

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in [IOB Output Switching Characteristics Standard Adjustments, page 9](#).

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Propagation Delays						
O input to Pad	T _{IOOP}	1.2	2.9	3.2	3.5	ns, max
O input to Pad via transparent latch	T _{IOOLP}	1.4	3.4	3.7	4.0	ns, max
3-State Delays						
T input to Pad high-impedance ⁽¹⁾	T _{IOTHZ}	1.0	2.0	2.2	2.4	ns, max
T input to valid data on Pad	T _{IOTON}	1.4	3.1	3.3	3.7	ns, max
T input to Pad high-impedance via transparent latch ⁽¹⁾	T _{IOTLPHZ}	1.2	2.4	2.6	3.0	ns, max
T input to valid data on Pad via transparent latch	T _{IOTLPON}	1.6	3.5	3.8	4.2	ns, max
GTS to Pad high impedance ⁽¹⁾	T _{GTS}	2.5	4.9	5.5	6.3	ns, max
Sequential Delays						
Clock CLK						
Minimum Pulse Width, High	T _{CH}	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low	T _{CL}	0.8	1.5	1.7	2.0	ns, min

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Description	Symbol	Standard ⁽¹⁾	Speed Grade				Unit s
			Min	-6	-5	-4	
Output Delay Adjustments							
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T _{OLVTTTL_S2}	LVTTL, Slow, 2 mA	4.2	14.7	15.8	17.0	ns
	T _{OLVTTTL_S4}	4 mA	2.5	7.5	8.0	8.6	ns
	T _{OLVTTTL_S6}	6 mA	1.8	4.8	5.1	5.6	ns
	T _{OLVTTTL_S8}	8 mA	1.2	3.0	3.3	3.5	ns
	T _{OLVTTTL_S12}	12 mA	1.0	1.9	2.1	2.2	ns
	T _{OLVTTTL_S16}	16 mA	0.9	1.7	1.9	2.0	ns
	T _{OLVTTTL_S24}	24 mA	0.8	1.3	1.4	1.6	ns
	T _{OLVTTTL_F2}	LVTTL, Fast, 2mA	1.9	13.1	14.0	15.1	ns
	T _{OLVTTTL_F4}	4 mA	0.7	5.3	5.7	6.1	ns
	T _{OLVTTTL_F6}	6 mA	0.2	3.1	3.3	3.6	ns
	T _{OLVTTTL_F8}	8 mA	0.1	1.0	1.1	1.2	ns
	T _{OLVTTTL_F12}	12 mA	0	0	0	0	ns
	T _{OLVTTTL_F16}	16 mA	−0.10	−0.05	−0.05	−0.05	ns
	T _{OLVTTTL_F24}	24 mA	−0.10	−0.20	−0.21	−0.23	ns
	T _{OLVCMOS2}	LVC MOS2	0.10	0.10	0.11	0.12	ns
	T _{OPCI33_3}	PCI, 33 MHz, 3.3 V	0.50	2.3	2.5	2.7	ns
	T _{OPCI33_5}	PCI, 33 MHz, 5.0 V	0.40	2.8	3.0	3.3	ns
	T _{OPCI66_3}	PCI, 66 MHz, 3.3 V	0.10	−0.40	−0.42	−0.46	ns
	T _{OGTL}	GTL	0.6	0.50	0.54	0.6	ns
	T _{OGTLP}	GTL+	0.7	0.8	0.9	1.0	ns
	T _{OHSTL_I}	HSTL I	0.10	−0.50	−0.53	−0.5	ns
	T _{OHSTL_III}	HSTL III	−0.10	−0.9	−0.9	−1.0	ns
	T _{OHSTL_IV}	HSTL IV	−0.20	−1.0	−1.0	−1.1	ns
	T _{OSSTL2_I}	SSTL2 I	−0.10	−0.50	−0.53	−0.5	ns
	T _{OSSTL2_II}	SSTL2 II	−0.20	−0.9	−0.9	−1.0	ns
	T _{OSSTL3_I}	SSTL3 I	−0.20	−0.50	−0.53	−0.5	ns
	T _{OSSTL3_II}	SSTL3 II	−0.30	−1.0	−1.0	−1.1	ns
	T _{OCTT}	CTT	0	−0.6	−0.6	−0.6	ns
	T _{OAGP}	AGP	0	−0.9	−0.9	−1.0	ns

Notes:

- Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTTL. For other I/O standards and different loads, see [Table 2](#) and [Table 3](#).

Clock Distribution Guidelines

Description	Device	Symbol	Speed Grade			Units
			-6	-5	-4	
Global Clock Skew ⁽¹⁾						
Global Clock Skew between IOB Flip-flops	XCV50	T _{GSKEWIOB}	0.10	0.12	0.14	ns, max
	XCV100		0.12	0.13	0.15	ns, max
	XCV150		0.12	0.13	0.15	ns, max
	XCV200		0.13	0.14	0.16	ns, max
	XCV300		0.14	0.16	0.18	ns, max
	XCV400		0.13	0.13	0.14	ns, max
	XCV600		0.14	0.15	0.17	ns, max
	XCV800		0.16	0.17	0.20	ns, max
	XCV1000		0.20	0.23	0.25	ns, max

Notes:

- These clock-skew delays are provided for guidance only. They reflect the delays encountered in a typical design under worst-case conditions. Precise values for a particular design are provided by the timing analyzer.

Clock Distribution Switching Characteristics

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
GCLK IOB and Buffer						
Global Clock PAD to output.	T _{GPIO}	0.33	0.7	0.8	0.9	ns, max
Global Clock Buffer I input to O output	T _{GIO}	0.34	0.7	0.8	0.9	ns, max

Block RAM Switching Characteristics

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Sequential Delays						
Clock CLK to DOUT output	T _{BCKO}	1.7	3.4	3.8	4.3	ns, max
Setup and Hold Times before/after Clock CLK ⁽¹⁾	Setup Time / Hold Time					
ADDR inputs	T _{BACK} /T _{BCKA}	0.6 / 0	1.2 / 0	1.3 / 0	1.5 / 0	ns, min
DIN inputs	T _{BDCK} /T _{BCKD}	0.6 / 0	1.2 / 0	1.3 / 0	1.5 / 0	ns, min
EN input	T _{BECK} /T _{BCKE}	1.3 / 0	2.6 / 0	3.0 / 0	3.4 / 0	ns, min
RST input	T _{BRCK} /T _{BCKR}	1.3 / 0	2.5 / 0	2.7 / 0	3.2 / 0	ns, min
WEN input	T _{BWCK} /T _{BCKW}	1.2 / 0	2.3 / 0	2.6 / 0	3.0 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T _{BPWH}	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low	T _{BPWL}	0.8	1.5	1.7	2.0	ns, min
CLKA -> CLKB setup time for different ports	T _{BCCS}		3.0	3.5	4.0	ns, min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

TBUF Switching Characteristics

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Combinatorial Delays						
IN input to OUT output	T _{IO}	0	0	0	0	ns, max
TRI input to OUT output high-impedance	T _{OFF}	0.05	0.09	0.10	0.11	ns, max
TRI input to valid data on OUT output	T _{ON}	0.05	0.09	0.10	0.11	ns, max

JTAG Test Access Port Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
TMS and TDI Setup times before TCK	T_{TAPTCK}	4.0	4.0	4.0	ns, min
TMS and TDI Hold times after TCK	T_{TCKTAP}	2.0	2.0	2.0	ns, min
Output delay from clock TCK to output TDO	T_{TCKTDO}	11.0	11.0	11.0	ns, max
Maximum TCK clock frequency	F_{TCK}	33	33	33	MHz, max

Date	Version	Revision
01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
03/00	2.0	New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration.
05/00	2.1	Modified "Pins not listed..." statement. Speed grade update to Final status.
05/00	2.2	Modified Table 18.
09/00	2.3	<ul style="list-style-type: none"> Added XCV400 values to table under Minimum Clock-to-Out for Virtex Devices. Corrected Units column in table under IOB Input Switching Characteristics. Added values to table under CLB SelectRAM Switching Characteristics.
10/00	2.4	<ul style="list-style-type: none"> Corrected Pinout information for devices in the BG256, BG432, and BG560 packages in Table 18. Corrected BG256 Pin Function Diagram.
04/02/01	2.5	<ul style="list-style-type: none"> Revised minimums for Global Clock Set-Up and Hold for LVTTTL Standard, with DLL. Converted file to modularized format. See the Virtex Data Sheet section.
04/19/01	2.6	<ul style="list-style-type: none"> Clarified TIOCKP and TIOCKON IOB Output Switching Characteristics descriptors.
07/19/01	2.7	<ul style="list-style-type: none"> Under Absolute Maximum Ratings, changed (T_{SOL}) to 220 °C.
07/26/01	2.8	<ul style="list-style-type: none"> Removed T_{SOL} parameter and added footnote to Absolute Maximum Ratings table.
10/29/01	2.9	<ul style="list-style-type: none"> Updated the speed grade designations used in data sheets, and added Table 1, which shows the current speed grade designation for each device.
02/01/02	3.0	<ul style="list-style-type: none"> Added footnote to DC Input and Output Levels table.
07/19/02	3.1	<ul style="list-style-type: none"> Removed mention of MIL-M-38510/605 specification. Added link to xapp158 from the Power-On Power Supply Requirements section.
09/10/02	3.2	<ul style="list-style-type: none"> Added Clock CLK to IOB Input Switching Characteristics and IOB Output Switching Characteristics.
03/01/13	4.0	The products listed in this data sheet are obsolete. See XCN10016 for further information.

Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

- DS003-1, Virtex 2.5V FPGAs:
Introduction and Ordering Information (Module 1)
- DS003-2, Virtex 2.5V FPGAs:
Functional Description (Module 2)
- DS003-3, Virtex 2.5V FPGAs:
DC and Switching Characteristics (Module 3)
- DS003-4, Virtex 2.5V FPGAs:
Pinout Tables (Module 4)

Virtex Pinout Information

Pinout Tables

See www.xilinx.com for updates or additional pinout information. For convenience, [Table 2](#), [Table 3](#) and [Table 4](#) list the locations of special-purpose and power-supply pins. Pins not listed are either user I/Os or not connected, depending on the device/package combination. See the Pinout Diagrams starting on [page 17](#) for any pins not listed for a particular part/package combination.

Table 2: Virtex Pinout Tables (Chip-Scale and QFP Packages)

Pin Name	Device	CS144	TQ144	PQ/HQ240
GCK0	All	K7	90	92
GCK1	All	M7	93	89
GCK2	All	A7	19	210
GCK3	All	A6	16	213
M0	All	M1	110	60
M1	All	L2	112	58
M2	All	N2	108	62
CCLK	All	B13	38	179
PROGRAM	All	L12	72	122
DONE	All	M12	74	120
INIT	All	L13	71	123
BUSY/DOUT	All	C11	39	178
D0/DIN	All	C12	40	177
D1	All	E10	45	167
D2	All	E12	47	163
D3	All	F11	51	156
D4	All	H12	59	145
D5	All	J13	63	138
D6	All	J11	65	134
D7	All	K10	70	124
WRITE	All	C10	32	185
CS	All	D10	33	184
TDI	All	A11	34	183
TDO	All	A12	36	181
TMS	All	B1	143	2
TCK	All	C3	2	239
V _{CCINT}	All	A9, B6, C5, G3, G12, M5, M9, N6	10, 15, 25, 57, 84, 94, 99, 126	16, 32, 43, 77, 88, 104, 137, 148, 164, 198, 214, 225

Table 2: Virtex Pinout Tables (Chip-Scale and QFP Packages) (Continued)

Pin Name	Device	CS144	TQ144	PQ/HQ240
V_{CCO}	All	Banks 0 and 1: A2, A13, D7 Banks 2 and 3: B12, G11, M13 Banks 4 and 5: N1, N7, N13 Banks 6 and 7: B2, G2, M2	No I/O Banks in this package: 1, 17, 37, 55, 73, 92, 109, 128	No I/O Banks in this package: 15, 30, 44, 61, 76, 90, 105, 121, 136, 150, 165, 180, 197, 212, 226, 240
V_{REF} Bank 0 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	C4, D6	5, 13	218, 232
	XCV100/150	... + B4	... + 7	... + 229
	XCV200/300	N/A	N/A	... + 236
	XCV400	N/A	N/A	... + 215
	XCV600	N/A	N/A	... + 230
	XCV800	N/A	N/A	... + 222
V_{REF} Bank 1 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	A10, B8	22, 30	191, 205
	XCV100/150	... + D9	... + 28	... + 194
	XCV200/300	N/A	N/A	... + 187
	XCV400	N/A	N/A	... + 208
	XCV600	N/A	N/A	... + 193
	XCV800	N/A	N/A	... + 201
V_{REF} Bank 2 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XCV50	D11, F10	42, 50	157, 171
	XCV100/150	... + D13	... + 44	... + 168
	XCV200/300	N/A	N/A	... + 175
	XCV400	N/A	N/A	... + 154
	XCV600	N/A	N/A	... + 169
	XCV800	N/A	N/A	... + 161

Table 3: Virtex Pinout Tables (BGA) (Continued)

Pin Name	Device	BG256	BG352	BG432	BG560
V _{CCO} , Bank 7	All	G4, H4	G23, K26, N23	A31, L28, L31	C32, D33, K33, N32, T33
V _{REF} Bank 0 (VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all VREF pins are general I/O.	XCV50	A8, B4	N/A	N/A	N/A
	XCV100/150	... + A4	A16, C19, C21	N/A	N/A
	XCV200/300	... + A2	... + D21	B19, D22, D24, D26	N/A
	XCV400	N/A	N/A	... + C18	A19, D20, D26, E23, E27
	XCV600	N/A	N/A	... + C24	... + E24
	XCV800	N/A	N/A	... + B21	... + E21
	XCV1000	N/A	N/A	N/A	... + D29
V _{REF} Bank 1 (VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all VREF pins are general I/O.	XCV50	A17, B12	N/A	N/A	N/A
	XCV100/150	... + B15	B6, C9, C12	N/A	N/A
	XCV200/300	... + B17	... + D6	A13, B7, C6, C10	N/A
	XCV400	N/A	N/A	... + B15	A6, D7, D11, D16, E15
	XCV600	N/A	N/A	... + D10	... + D10
	XCV800	N/A	N/A	... + B12	... + D13
	XCV1000	N/A	N/A	N/A	... + E7
V _{REF} Bank 2 (VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all VREF pins are general I/O.	XCV50	C20, J18	N/A	N/A	N/A
	XCV100/150	... + F19	E2, H2, M4	N/A	N/A
	XCV200/300	... + G18	... + D2	E2, G3, J2, N1	N/A
	XCV400	N/A	N/A	... + R3	G5, H4, L5, P4, R1
	XCV600	N/A	N/A	... + H1	... + K5
	XCV800	N/A	N/A	... + M3	... + N5
	XCV1000	N/A	N/A	N/A	... + B3

Table 3: Virtex Pinout Tables (BGA) (Continued)

Pin Name	Device	BG256	BG352	BG432	BG560
V_{REF} Bank 3 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	M18, V20	N/A	N/A	N/A
	XCV100/150	... + R19	R4, V4, Y3	N/A	N/A
	XCV200/300	... + P18	... + AC2	V2, AB4, AD4, AF3	N/A
	XCV400	N/A	N/A	... + U2	V4, W5, AD3, AE5, AK2
	XCV600	N/A	N/A	... + AC3	... + AF1
	XCV800	N/A	N/A	... + Y3	... + AA4
	XCV1000	N/A	N/A	N/A	... + AH4
V_{REF} Bank 4 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	V12, Y18	N/A	N/A	N/A
	XCV100/150	... + W15	AC12, AE5, AE8,	N/A	N/A
	XCV200/300	... + V14	... + AE4	AJ7, AL4, AL8, AL13	N/A
	XCV400	N/A	N/A	... + AK15	AL7, AL10, AL16, AM4, AM14
	XCV600	N/A	N/A	... + AK8	... + AL9
	XCV800	N/A	N/A	... + AJ12	... + AK13
	XCV1000	N/A	N/A	N/A	... + AN3
V_{REF} Bank 5 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	V9, Y3	N/A	N/A	N/A
	XCV100/150	... + W6	AC15, AC18, AD20	N/A	N/A
	XCV200/300	... + V7	... + AE23	AJ18, AJ25, AK23, AK27	N/A
	XCV400	N/A	N/A	... + AJ17	AJ18, AJ25, AL20, AL24, AL29
	XCV600	N/A	N/A	... + AL24	... + AM26
	XCV800	N/A	N/A	... + AH19	... + AN23
	XCV1000	N/A	N/A	N/A	... + AK28
V_{REF} Bank 6 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	M2, R3	N/A	N/A	N/A
	XCV100/150	... + T1	R24, Y26, AA25,	N/A	N/A
	XCV200/300	... + T3	... + AD26	V28, AB28, AE30, AF28	N/A
	XCV400	N/A	N/A	... + U28	V29, Y32, AD31, AE29, AK32
	XCV600	N/A	N/A	... + AC28	... + AE31
	XCV800	N/A	N/A	... + Y30	... + AA30
	XCV1000	N/A	N/A	N/A	... + AH30

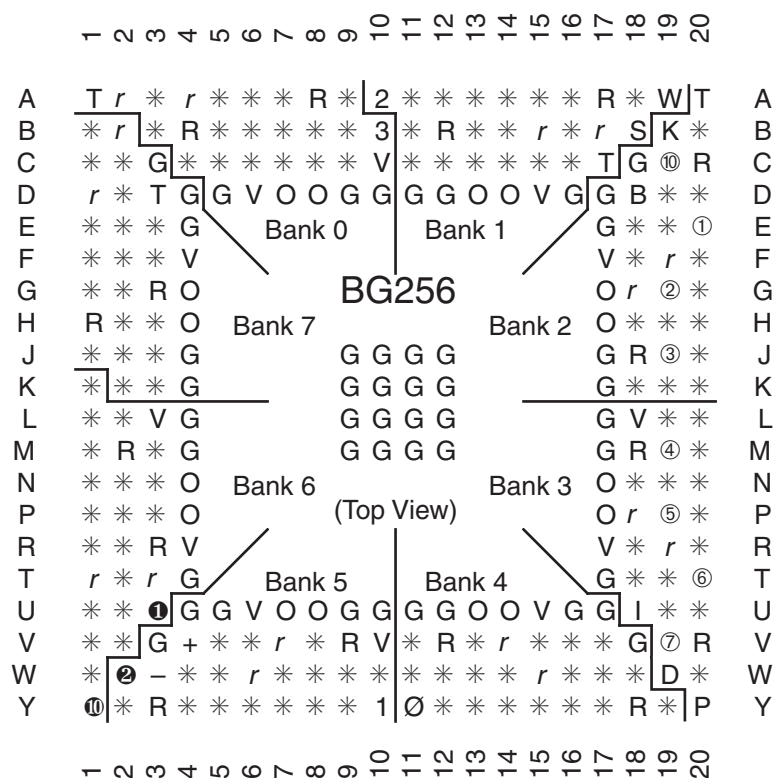
Table 4: Virtex Pinout Tables (Fine-Pitch BGA)

Pin Name	Device	FG256	FG456	FG676	FG680
GCK0	All	N8	W12	AA14	AW19
GCK1	All	R8	Y11	AB13	AU22
GCK2	All	C9	A11	C13	D21
GCK3	All	B8	C11	E13	A20
M0	All	N3	AB2	AD4	AT37
M1	All	P2	U5	W7	AU38
M2	All	R3	Y4	AB6	AT35
CCLK	All	D15	B22	D24	E4
PROGRAM	All	P15	W20	AA22	AT5
DONE	All	R14	Y19	AB21	AU5
INIT	All	N15	V19	Y21	AU2
BUSY/DOUT	All	C15	C21	E23	E3
D0/DIN	All	D14	D20	F22	C2
D1	All	E16	H22	K24	P4
D2	All	F15	H20	K22	P3
D3	All	G16	K20	M22	R1
D4	All	J16	N22	R24	AD3
D5	All	M16	R21	U23	AG2
D6	All	N16	T22	V24	AH1
D7	All	N14	Y21	AB23	AR4
WRITE	All	C13	A20	C22	B4
CS	All	B13	C19	E21	D5
TDI	All	A15	B20	D22	B3
TDO	All	B14	A21	C23	C4
TMS	All	D3	D3	F5	E36
TCK	All	C4	C4	E6	C36
DXN	All	R4	Y5	AB7	AV37
DXP	All	P4	V6	Y8	AU35

Table 4: Virtex Pinout Tables (Fine-Pitch BGA) (Continued)

Pin Name	Device	FG256	FG456	FG676	FG680
V _{CCINT}	All	C3, C14, D4, D13, E5, E12, M5, M12, N4, N13, P3, P14	E5, E18, F6, F17, G7, G8, G9, G14, G15, G16, H7, H16, J7, J16, P7, P16, R7, R16, T7, T8, T9, T14, T15, T16, U6, U17, V5, V18	G7, G20, H8, H19, J9, J10, J11, J16, J17, J18, K9, K18, L9, L18, T9, T18, U9, U18, V9, V10, V11, V16, V17, V18, W8, W19, Y7, Y20	AD5, AD35, AE5, AE35, AL5, AL35, AM5, AM35, AR8, AR9, AR15, AR16, AR24, AR25, AR31, AR32, E8, E9, E15, E16, E24, E25, E31, E32, H5, H35, J5, J35, R5, R35, T5, T35
V _{CCO} , Bank 0	All	E8, F8	F7, F8, F9, F10, G10, G11	H9, H10, H11, H12, J12, J13	E26, E27, E29, E30, E33, E34
V _{CCO} , Bank 1	All	E9, F9	F13, F14, F15, F16, G12, G13	H15, H16, H17, H18, J14, J15	E6, E7, E10, E11, E13, E14
V _{CCO} , Bank 2	All	H11, H12	G17, H17, J17, K16, K17, L16	J19, K19, L19, M18, M19, N18	F5, G5, K5, L5, N5, P5
V _{CCO} , Bank 3	All	J11, J12	M16, N16, N17, P17, R17, T17	P18, R18, R19, T19, U19, V19	AF5, AG5, AN5, AK5, AJ5, AP5
V _{CCO} , Bank 4	All	L9, M9	T12, T13, U13, U14, U15, U16,	V14, V15, W15, W16, W17, W18	AR6, AR7, AR10, AR11, AR13, AR14
V _{CCO} , Bank 5	All	L8, M8	T10, T11, U7, U8, U9, U10	V12, V13, W9, W10, W11, W12	AR26, AR27, AR29, AR30, AR33, AR34
V _{CCO} , Bank 6	All	J5, J6	M7, N6, N7, P6, R6, T6	P9, R8, R9, T8, U8, V8	AF35, AG35, AJ35, AK35, AN35, AP35
V _{CCO} , Bank 7	All	H5, H6	G6, H6, J6, K6, K7, L7	J8, K8, L8, M8, M9, N9	F35, G35, K35, L35, N35, P35
V _{REF} , Bank 0 (VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	B4, B7	N/A	N/A	N/A
	XCV100/150	... + C6	A9, C6, E8	N/A	N/A
	XCV200/300	... + A3	... + B4	N/A	N/A
	XCV400	N/A	N/A	A12, C11, D6, E8, G10	
	XCV600	N/A	N/A	... + B7	A33, B28, B30, C23, C24, D33
	XCV800	N/A	N/A	... + B10	... + A26
	XCV1000	N/A	N/A	N/A	... + D34

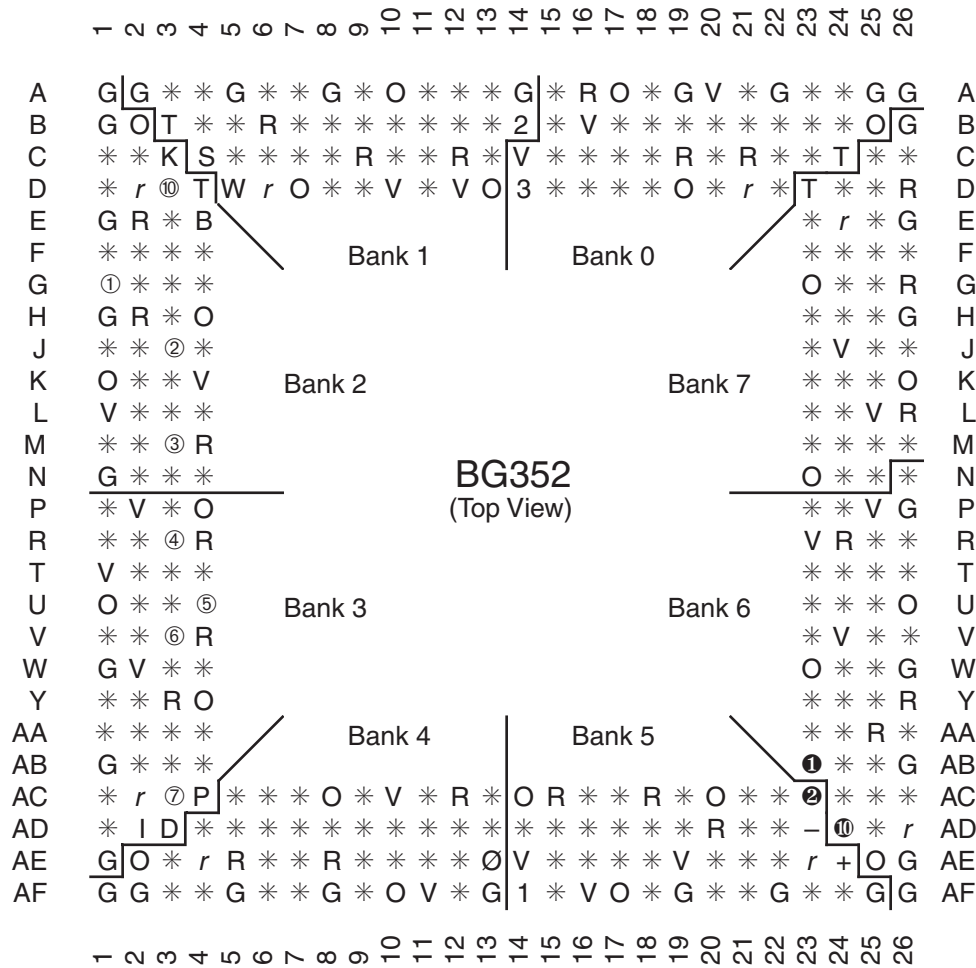
BG256 Pin Function Diagram



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Figure 4: BG256 Pin Function Diagram

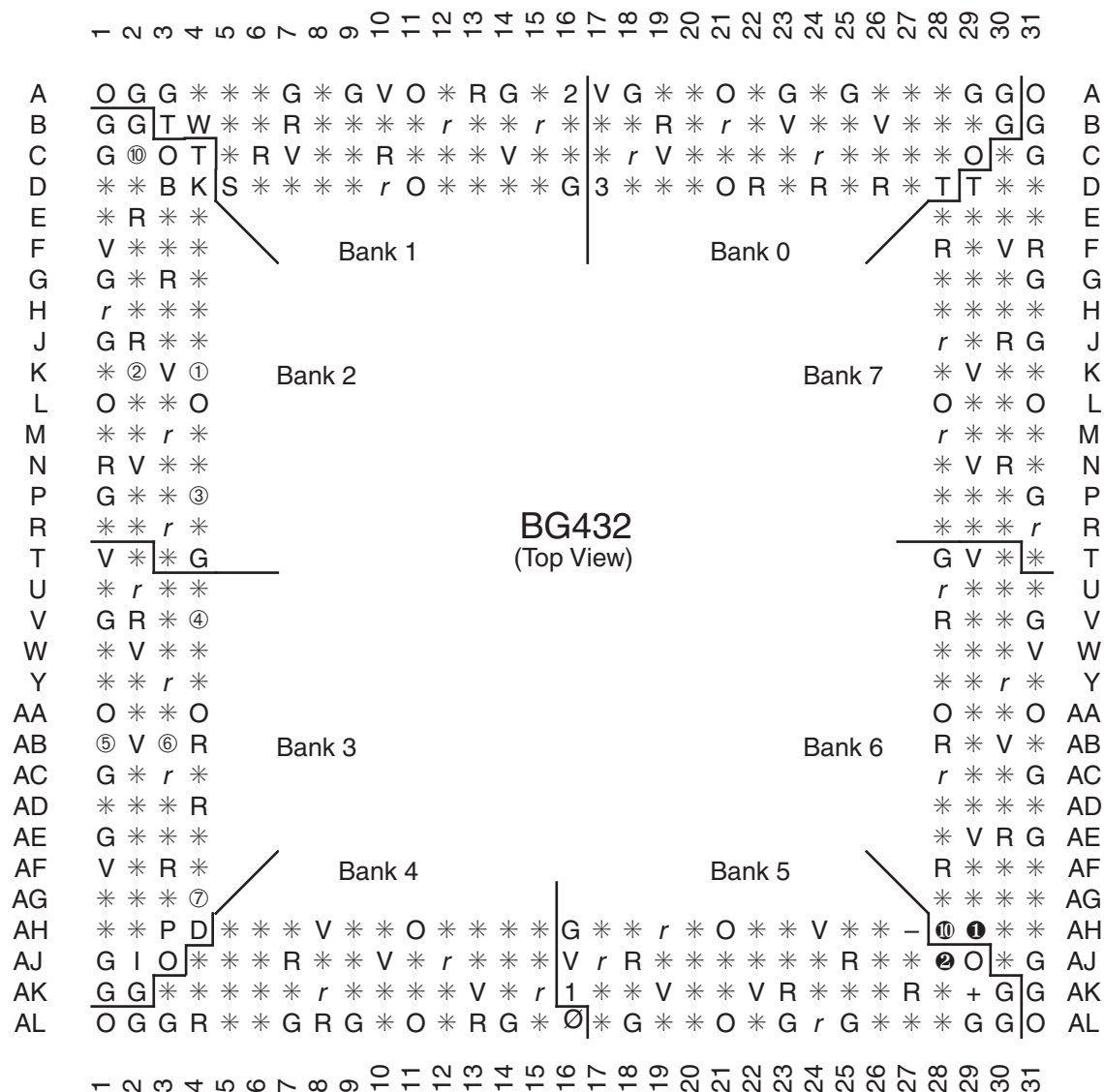
BG352 Pin Function Diagram



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Figure 5: BG352 Pin Function Diagram

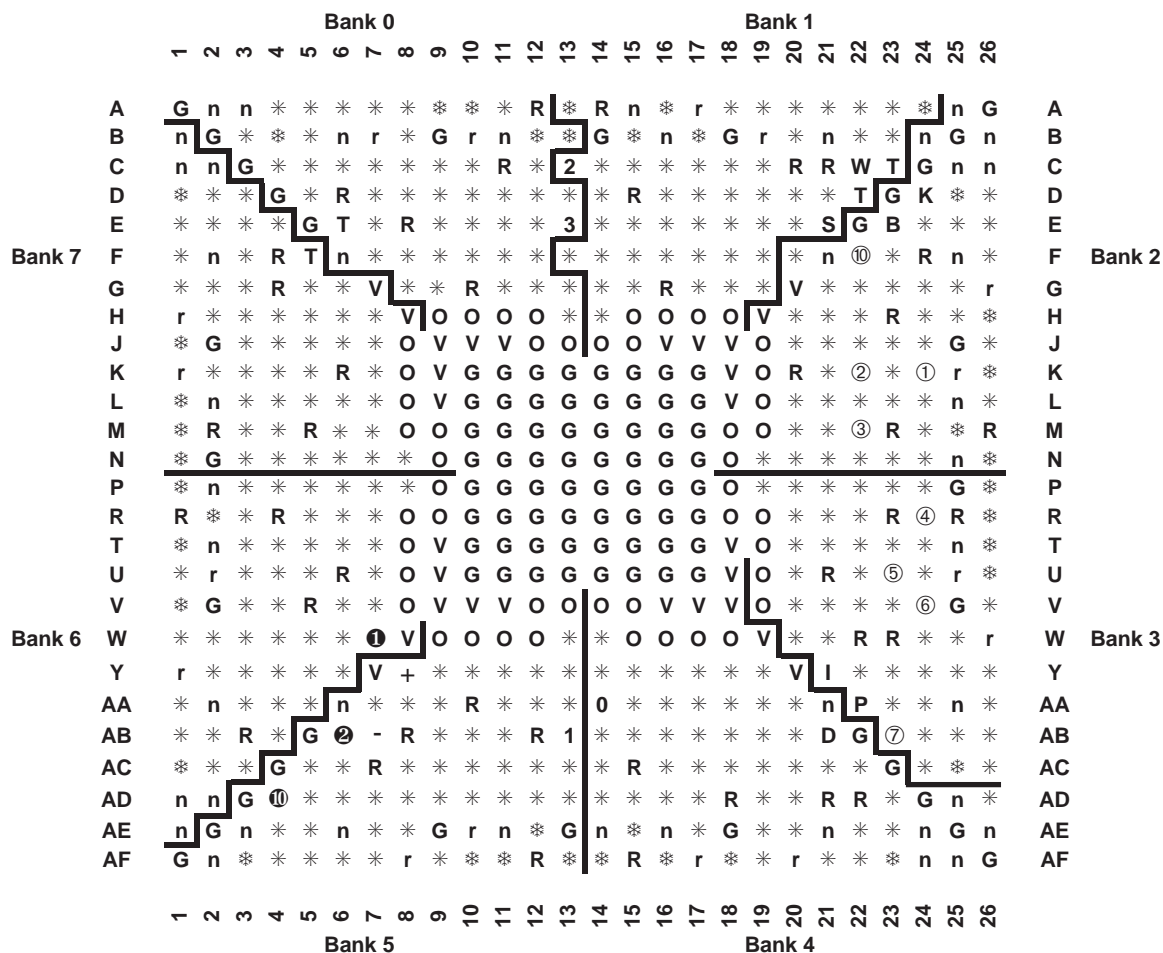
BG432 Pin Function Diagram



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Figure 6: BG432 Pin Function Diagram

FG676 Pin Function Diagram

FG676
(Top view)

fg676a

Figure 10: FG676 Pin Function Diagram

Notes:

Packages FG456 and FG676 are layout compatible.