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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	2400
Number of Logic Elements/Cells	10800
Total RAM Bits	81920
Number of I/O	166
Number of Gates	468252
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-PQFP (32x32)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xcv400-5hq240c">https://www.e-xfl.com/product-detail/xilinx/xcv400-5hq240c</a>

## Revision History

Date	Version	Revision
11/98	1.0	Initial Xilinx release.
01/99-02/99	1.2-1.3	Both versions updated package drawings and specs.
05/99	1.4	Addition of package drawings and specifications.
05/99	1.5	Replaced FG 676 & FG680 package drawings.
07/99	1.6	Changed Boundary Scan Information and changed Figure 11, Boundary Scan Bit Sequence. Updated IOB Input & Output delays. Added Capacitance info for different I/O Standards. Added 5 V tolerant information. Added DLL Parameters and waveforms and new Pin-to-pin Input and Output Parameter tables for Global Clock Input to Output and Setup and Hold. Changed Configuration Information including Figures 12, 14, 17 & 19. Added device-dependent listings for quiescent currents ICCINTQ and ICCOQ. Updated IOB Input and Output Delays based on default standard of LVTTTL, 12 mA, Fast Slew Rate. Added IOB Input Switching Characteristics Standard Adjustments.
09/99	1.7	Speed grade update to preliminary status, Power-on specification and Clock-to-Out Minimums additions, "0" hold time listing explanation, quiescent current listing update, and Figure 6 ADDRA input label correction. Added T <sub>IJITCC</sub> parameter, changed T <sub>OJIT</sub> to T <sub>OPHASE</sub> .
01/00	1.8	Update to speed.txt file 1.96. Corrections for CRs 111036, 111137, 112697, 115479, 117153, 117154, and 117612. Modified notes for Recommended Operating Conditions (voltage and temperature). Changed Bank information for V <sub>CCO</sub> in CS144 package on p.43.
01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
03/00	2.0	New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration.
05/00	2.1	Modified "Pins not listed..." statement. Speed grade update to Final status.
05/00	2.2	Modified Table 18.
09/00	2.3	<ul style="list-style-type: none"> <li>Added XCV400 values to table under <b>Minimum Clock-to-Out for Virtex Devices</b>.</li> <li>Corrected Units column in table under <b>IOB Input Switching Characteristics</b>.</li> <li>Added values to table under <b>CLB SelectRAM Switching Characteristics</b>.</li> </ul>
10/00	2.4	<ul style="list-style-type: none"> <li>Corrected Pinout information for devices in the BG256, BG432, and BG560 packages in Table 18.</li> <li>Corrected <b>BG256 Pin Function Diagram</b>.</li> </ul>
04/01	2.5	<ul style="list-style-type: none"> <li>Revised minimums for <b>Global Clock Set-Up and Hold for LVTTTL Standard, with DLL</b>.</li> <li>Converted file to modularized format. See <b>Virtex Data Sheet</b> section.</li> </ul>
03/13	4.0	The products listed in this data sheet are obsolete. See <a href="#">XCN10016</a> for further information.

## Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

- DS003-1, Virtex 2.5V FPGAs:  
Introduction and Ordering Information (Module 1)
- DS003-2, Virtex 2.5V FPGAs:  
Functional Description (Module 2)
- DS003-3, Virtex 2.5V FPGAs:  
DC and Switching Characteristics (Module 3)
- DS003-4, Virtex 2.5V FPGAs:  
Pinout Tables (Module 4)

more I/O pins convert to  $V_{REF}$  pins. Since these are always a superset of the  $V_{REF}$  pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary. All the  $V_{REF}$  pins for the largest device anticipated must be connected to the  $V_{REF}$  voltage, and not used for I/O.

In smaller devices, some  $V_{CCO}$  pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or can be connected to the  $V_{CCO}$  voltage to permit migration to a larger device if necessary.

In TQ144 and PQ/HQ240 packages, all  $V_{CCO}$  pins are bonded together internally, and consequently the same  $V_{CCO}$  voltage must be connected to all of them. In the CS144 package, bank pairs that share a side are interconnected internally, permitting four choices for  $V_{CCO}$ . In both cases, the  $V_{REF}$  pins remain internally connected as eight banks, and can be used as described previously.

## Configurable Logic Block

The basic building block of the Virtex CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and a storage element. The output from the function generator in each LC drives both the CLB output and the D input of the flip-flop. Each Virtex CLB contains four LCs, organized in two similar slices, as shown in Figure 4.

Figure 5 shows a more detailed view of a single slice.

In addition to the four basic LCs, the Virtex CLB contains logic that combines function generators to provide functions

of five or six inputs. Consequently, when estimating the number of system gates provided by a given device, each CLB counts as 4.5 LCs.

## Look-Up Tables

Virtex function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16x1-bit dual-port synchronous RAM.

The Virtex LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

## Storage Elements

The storage elements in the Virtex slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by the function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each Slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals can be configured to operate asynchronously. All of the control signals are independently invertible, and are shared by the two flip-flops within the slice.

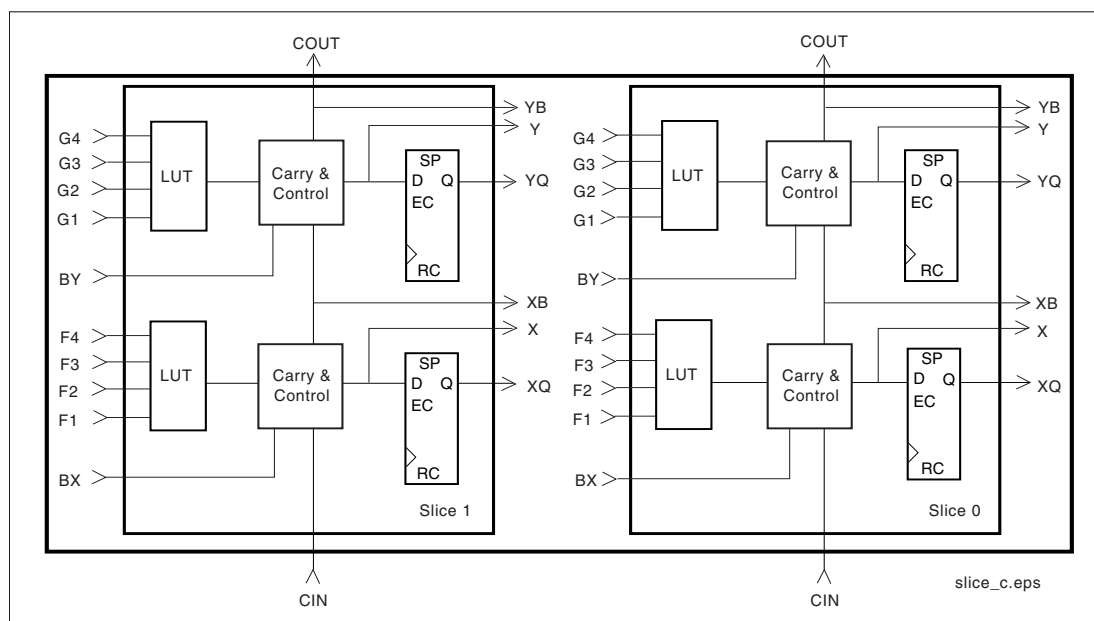


Figure 4: 2-Slice Virtex CLB

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is

selected either from these pads or from signals in the general purpose routing.

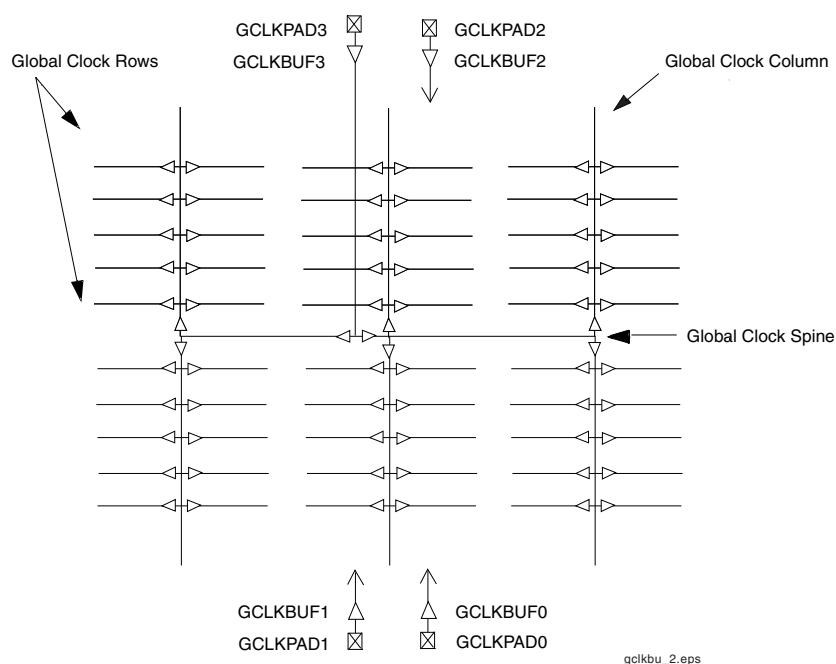


Figure 9: Global Clock Distribution Network

### Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Clock edges reach internal flip-flops one to four clock periods after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to de-skew a board level clock among multiple Virtex devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

See **DLL Timing Parameters**, page 21 of Module 3, for frequency range information.

### Boundary Scan

Virtex devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, and HIGHZ instructions. The TAP also supports two internal scan chains and configuration/readback of the device. The TAP uses dedicated package pins that always operate using LVTTTL. For TDO to operate using LVTTTL, the  $V_{CCO}$  for Bank 2 should be 3.3 V. Otherwise, TDO switches rail-to-rail between ground and  $V_{CCO}$ .

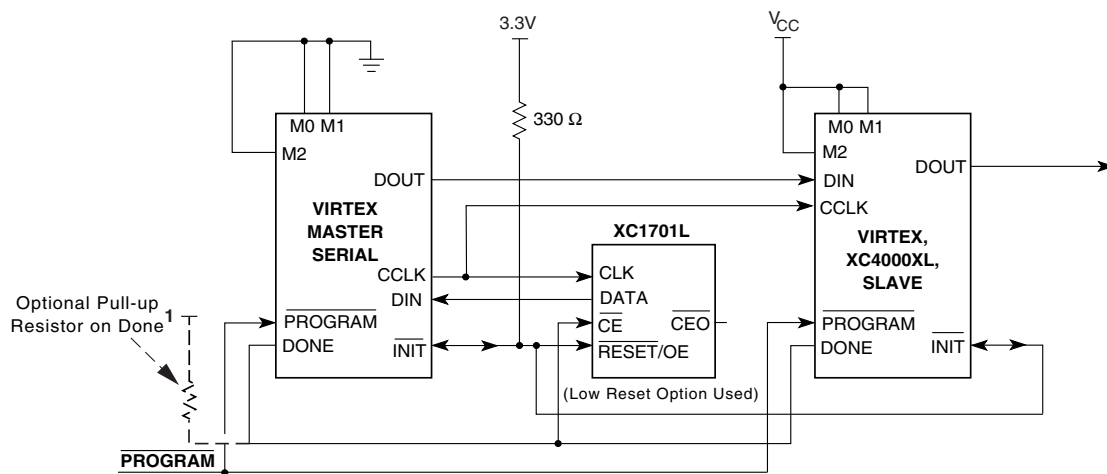
Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including un-bonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections, provided the user design or application is turned off.

**Table 5** lists the boundary-scan instructions supported in Virtex FPGAs. Internal signals can be captured during EXTEST by connecting them to un-bonded or unused IOBs. They can also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Before the device is configured, all instructions except USER1 and USER2 are available. After configuration, all instructions are available. During configuration, it is recommended that those operations using the boundary-scan register (SAMPLE/PRELOAD, INTEST, EXTEST) not be performed.

Table 8: Master/Slave Serial Mode Programming Switching

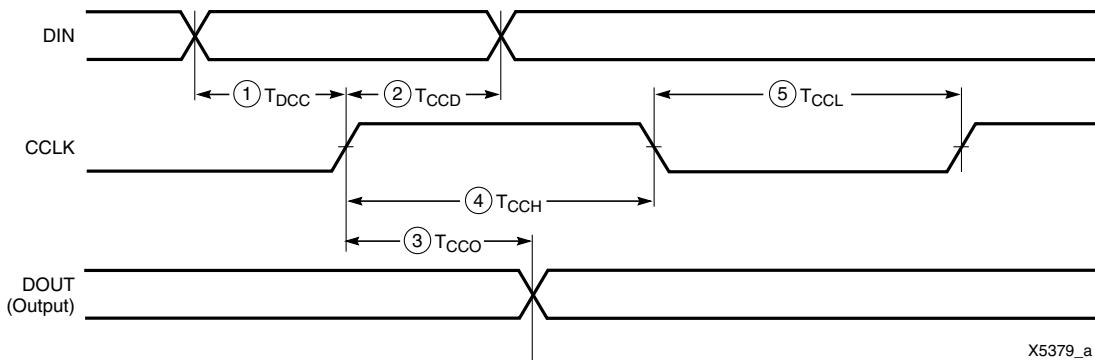
	Description	Figure References	Symbol	Values	Units
CCLK	DIN setup/hold, slave mode	1/2	$T_{DCC}/T_{CCD}$	5.0 / 0	ns, min
	DIN setup/hold, master mode	1/2	$T_{DSCK}/T_{CKDS}$	5.0 / 0	ns, min
	DOUT	3	$T_{CCO}$	12.0	ns, max
	High time	4	$T_{CCH}$	5.0	ns, min
	Low time	5	$T_{CCL}$	5.0	ns, min
	Maximum Frequency		$F_{CC}$	66	MHz, max
	Frequency Tolerance, master mode with respect to nominal			+45% -30%	



**Note 1:** If none of the Virtex FPGAs have been selected to drive DONE, an external pull-up resistor of 330  $\Omega$  should be added to the common DONE line. (For Spartan-XL devices, add a 4.7K  $\Omega$  pull-up resistor.) This pull-up is not needed if the DriveDONE attribute is set. If used, DriveDONE should be selected only for the last device in the configuration chain.

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Figure 12: Master/Slave Serial Mode Circuit Diagram



X5379\_a

Figure 13: Slave-Serial Mode Programming Switching Characteristics

## Master-Serial Mode

In master-serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM that feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge.

The interface is identical to slave-serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration. Switching to a lower frequency is prohibited.

The CCLK frequency is set using the ConfigRate option in the bitstream generation software. The maximum CCLK frequency that can be selected is 60 MHz. When selecting a CCLK frequency, ensure that the serial PROM and any

daisy-chained FPGAs are fast enough to support the clock rate.

On power-up, the CCLK frequency is 2.5 MHz. This frequency is used until the ConfigRate bits have been loaded when the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz.

Figure 12 shows a full master/slave system. In this system, the left-most device operates in master-serial mode. The remaining devices operate in slave-serial mode. The SPROM  $\overline{\text{RESET}}$  pin is driven by  $\overline{\text{INIT}}$ , and the  $\overline{\text{CE}}$  input is driven by DONE. There is the potential for contention on the DONE pin, depending on the start-up sequence options chosen.

Figure 14 shows the timing of master-serial configuration. Master-serial mode is selected by a <000> or <100> on the mode pins (M2, M1, M0). Table 8 shows the timing information for Figure 14.

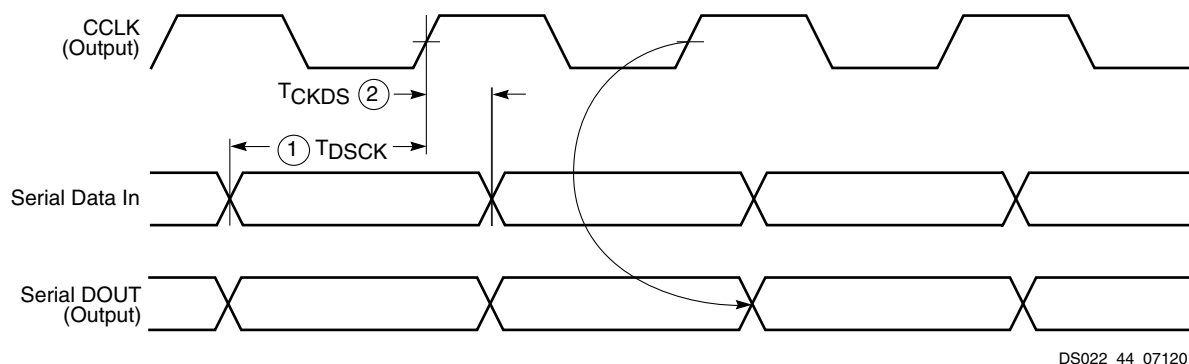


Figure 14: Master-Serial Mode Programming Switching Characteristics

At power-up,  $V_{CC}$  must rise from 1.0 V to  $V_{CC}$  min in less than 50 ms, otherwise delay configuration by pulling  $\overline{\text{PROGRAM}}$  Low until  $V_{CC}$  is valid.

The sequence of operations necessary to configure a Virtex FPGA serially appears in Figure 15.

## SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the FPGA with a  $\overline{\text{BUSY}}$  flag controlling the flow of data.

An external data source provides a byte stream, CCLK, a Chip Select ( $\overline{\text{CS}}$ ) signal and a Write signal ( $\overline{\text{WRITE}}$ ). If  $\overline{\text{BUSY}}$  is asserted (High) by the FPGA, the data must be held until  $\overline{\text{BUSY}}$  goes Low.

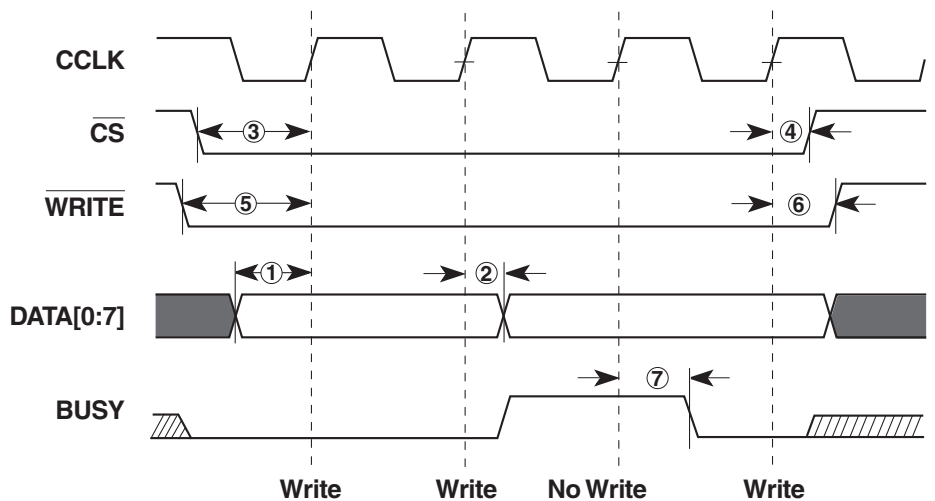
Data can also be read using the SelectMAP mode. If  $\overline{\text{WRITE}}$  is not asserted, configuration data is read out of the FPGA as part of a readback operation.

In the SelectMAP mode, multiple Virtex devices can be chained in parallel. DATA pins (D7:D0), CCLK,  $\overline{\text{WRITE}}$ ,  $\overline{\text{BUSY}}$ ,  $\overline{\text{PROGRAM}}$ , DONE, and  $\overline{\text{INIT}}$  can be connected in parallel between all the FPGAs. Note that the data is organized with the MSB of each byte on pin D0 and the LSB of each byte on D7. The  $\overline{\text{CS}}$  pins are kept separate, insuring that each FPGA can be selected individually.  $\overline{\text{WRITE}}$  should be Low before loading the first bitstream and returned High after the last device has been programmed. Use  $\overline{\text{CS}}$  to select the appropriate FPGA for loading the bitstream and sending the configuration data. At the end of the bitstream, deselect the loaded device and select the next target FPGA by setting its  $\overline{\text{CS}}$  pin High. A free-running oscillator or other externally generated signal can be used for CCLK. The  $\overline{\text{BUSY}}$  signal can be ignored for frequencies below 50 MHz. For details about frequencies above 50 MHz, see XAPP138, Virtex Configuration and Readback. Once all the devices have been programmed, the DONE pin goes High.

3. At the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this has happened.
4. Repeat steps 2 and 3 until all the data has been sent.

5. De-assert  $\overline{\text{CS}}$  and  $\overline{\text{WRITE}}$ .

A flowchart for the write operation appears in [Figure 17](#). Note that if CCLK is slower than  $f_{\text{CCNH}}$ , the FPGA never asserts BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.



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Figure 16: Write Operations





Figure 18: SelectMAP Write Abort Waveforms

## Boundary-Scan Mode

In the boundary-scan mode, configuration is done through the IEEE 1149.1 Test Access Port. Note that the **PROGRAM** pin must be pulled High prior to reconfiguration. A Low on the **PROGRAM** pin resets the TAP controller and no JTAG operations can be performed.

Configuration through the TAP uses the **CFG\_IN** instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port (when using TCK as a start-up clock).

1. Load the **CFG\_IN** instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the **JSTART** instruction into IR
6. Enter the SDR state
7. Clock TCK through the startup sequence
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode is selected by a <101> or 001> on the mode pins (M2, M1, M0). For details on TAP characteristics, refer to XAPP139.

## Configuration Sequence

The configuration of Virtex devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user, as described below. The configuration process can also be initiated by asserting **PROGRAM**.

The end of the memory-clearing phase is signalled by **INIT** going High, and the completion of the entire process is signalled by **DONE** going High.

The power-up timing of configuration signals is shown in Figure 19. The corresponding timing characteristics are listed in Table 10.

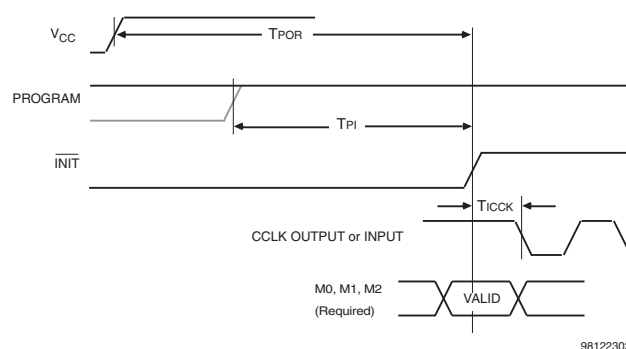


Figure 19: Power-Up Timing Configuration Signals

Table 10: Power-up Timing Characteristics

Description	Symbol	Value	Units
Power-on Reset	T <sub>POR</sub>	2.0	ms, max
Program Latency	T <sub>PL</sub>	100.0	μs, max
CCLK (output) Delay	T <sub>ICCK</sub>	0.5	μs, min
		4.0	μs, max
Program Pulse Width	T <sub>PROGRAM</sub>	300	ns, min

## Delaying Configuration

**INIT** can be held Low using an open-drain driver. An open-drain is required since **INIT** is a bidirectional open-drain pin that is held Low by the FPGA while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

## Start-Up Sequence

The default Start-up sequence is that one CCLK cycle after **DONE** goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed. In addition, the GTS, GSR, and GWE events can be made dependent on the **DONE** pins of multiple devices all going High, forcing the devices to start in synchronism. The sequence can also be paused at any stage until lock has been achieved on any or all DLLs.



## Virtex DC Characteristics

### Absolute Maximum Ratings

Symbol	Description <sup>(1)</sup>			Units
$V_{CCINT}$	Supply voltage relative to GND <sup>(2)</sup>		–0.5 to 3.0	V
$V_{CCO}$	Supply voltage relative to GND <sup>(2)</sup>		–0.5 to 4.0	V
$V_{REF}$	Input Reference Voltage		–0.5 to 3.6	V
$V_{IN}$	Input voltage relative to GND <sup>(3)</sup>	Using $V_{REF}$	–0.5 to 3.6	V
		Internal threshold	–0.5 to 5.5	V
$V_{TS}$	Voltage applied to 3-state output		–0.5 to 5.5	V
$V_{CC}$	Longest Supply Voltage Rise Time from 1V-2.375V		50	ms
$T_{STG}$	Storage temperature (ambient)		–65 to +150	°C
$T_J$	Junction temperature <sup>(4)</sup>	Plastic Packages	+125	°C

#### Notes:

- Stresses beyond those listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time can affect device reliability.
- Power supplies can turn on in any order.
- For protracted periods (e.g., longer than a day),  $V_{IN}$  should not exceed  $V_{CCO}$  by more than 3.6 V.
- For soldering guidelines and thermal considerations, see the "Device Packaging" information on [www.xilinx.com](http://www.xilinx.com).

### Recommended Operating Conditions

Symbol	Description		Min	Max	Units
$V_{CCINT}^{(1)}$	Input Supply voltage relative to GND, $T_J = 0\text{ °C to }+85\text{ °C}$	Commercial	2.5 – 5%	2.5 + 5%	V
	Input Supply voltage relative to GND, $T_J = -40\text{ °C to }+100\text{ °C}$	Industrial	2.5 – 5%	2.5 + 5%	V
$V_{CCO}^{(4)}$	Supply voltage relative to GND, $T_J = 0\text{ °C to }+85\text{ °C}$	Commercial	1.4	3.6	V
	Supply voltage relative to GND, $T_J = -40\text{ °C to }+100\text{ °C}$	Industrial	1.4	3.6	V
$T_{IN}$	Input signal transition time			250	ns

#### Notes:

- Correct operation is guaranteed with a minimum  $V_{CCINT}$  of 2.375 V (Nominal  $V_{CCINT}$  –5%). Below the minimum value, all delay parameters increase by 3% for each 50-mV reduction in  $V_{CCINT}$  below the specified range.
- At junction temperatures above those listed as Operating Conditions, delay parameters do increase. Please refer to the TRCE report.
- Input and output measurement threshold is ~50% of  $V_{CC}$ .
- Min and Max values for  $V_{CCO}$  are I/O Standard dependant.

### Virtex Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation net list. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Virtex devices unless otherwise noted.

### IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTTL levels. For other standards, adjust the delays with the values shown in , page 6.

Description	Device	Symbol	Speed Grade				Units
			Min	-6	-5	-4	
Propagation Delays							
Pad to I output, no delay	All	T <sub>IOPI</sub>	0.39	0.8	0.9	1.0	ns, max
Pad to I output, with delay	XCV50	T <sub>IOPID</sub>	0.8	1.5	1.7	1.9	ns, max
	XCV100		0.8	1.5	1.7	1.9	ns, max
	XCV150		0.8	1.5	1.7	1.9	ns, max
	XCV200		0.8	1.5	1.7	1.9	ns, max
	XCV300		0.8	1.5	1.7	1.9	ns, max
	XCV400		0.9	1.8	2.0	2.3	ns, max
	XCV600		0.9	1.8	2.0	2.3	ns, max
	XCV800		1.1	2.1	2.4	2.7	ns, max
	XCV1000		1.1	2.1	2.4	2.7	ns, max
Pad to output IQ via transparent latch, no delay	All	T <sub>IOPLI</sub>	0.8	1.6	1.8	2.0	ns, max
Pad to output IQ via transparent latch, with delay	XCV50	T <sub>IOPLID</sub>	1.9	3.7	4.2	4.8	ns, max
	XCV100		1.9	3.7	4.2	4.8	ns, max
	XCV150		2.0	3.9	4.3	4.9	ns, max
	XCV200		2.0	4.0	4.4	5.1	ns, max
	XCV300		2.0	4.0	4.4	5.1	ns, max
	XCV400		2.1	4.1	4.6	5.3	ns, max
	XCV600		2.1	4.2	4.7	5.4	ns, max
	XCV800		2.2	4.4	4.9	5.6	ns, max
	XCV1000		2.3	4.5	5.1	5.8	ns, max
Sequential Delays							
Clock CLK	All						
Minimum Pulse Width, High		T <sub>CH</sub>	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low		T <sub>CL</sub>	0.8	1.5	1.7	2.0	ns, min
Clock CLK to output IQ		T <sub>IOCKIQ</sub>	0.2	0.7	0.7	0.8	ns, max

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Clock CLK to Pad delay with OBUFT enabled (non-3-state)	$T_{IOCKP}$	1.0	2.9	3.2	3.5	ns, max
Clock CLK to Pad high-impedance (synchronous) <sup>(1)</sup>	$T_{IOCKHZ}$	1.1	2.3	2.5	2.9	ns, max
Clock CLK to valid data on Pad delay, plus enable delay for OBUFT	$T_{IOCKON}$	1.5	3.4	3.7	4.1	ns, max
<b>Setup and Hold Times before/after Clock CLK<sup>(2)</sup></b>		<b>Setup Time / Hold Time</b>				
O input	$T_{IOOCK}/T_{IOCKO}$	0.51 / 0	1.1 / 0	1.2 / 0	1.3 / 0	ns, min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$	0.37 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
SR input (OFF)	$T_{IOSRCKO}/T_{IOCKOSR}$	0.52 / 0	1.1 / 0	1.2 / 0	1.4 / 0	ns, min
3-State Setup Times, T input	$T_{IOTCK}/T_{IOCKT}$	0.34 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$	0.41 / 0	0.9 / 0	0.9 / 0	1.1 / 0	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$	0.49 / 0	1.0 / 0	1.1 / 0	1.3 / 0	ns, min
<b>Set/Reset Delays</b>						
SR input to Pad (asynchronous)	$T_{IOSRP}$	1.6	3.8	4.1	4.6	ns, max
SR input to Pad high-impedance (asynchronous) <sup>(1)</sup>	$T_{IOSRHZ}$	1.6	3.1	3.4	3.9	ns, max
SR input to valid data on Pad (asynchronous)	$T_{IOSRON}$	2.0	4.2	4.6	5.1	ns, max
GSR to Pad	$T_{IOGSRQ}$	4.9	9.7	10.9	12.5	ns, max

**Notes:**

1. 3-state turn-off delays should not be adjusted.
2. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

### Clock Distribution Guidelines

Description	Device	Symbol	Speed Grade			Units
			-6	-5	-4	
Global Clock Skew <sup>(1)</sup>						
Global Clock Skew between IOB Flip-flops	XCV50	T <sub>GSKEWIOB</sub>	0.10	0.12	0.14	ns, max
	XCV100		0.12	0.13	0.15	ns, max
	XCV150		0.12	0.13	0.15	ns, max
	XCV200		0.13	0.14	0.16	ns, max
	XCV300		0.14	0.16	0.18	ns, max
	XCV400		0.13	0.13	0.14	ns, max
	XCV600		0.14	0.15	0.17	ns, max
	XCV800		0.16	0.17	0.20	ns, max
	XCV1000		0.20	0.23	0.25	ns, max

#### Notes:

- These clock-skew delays are provided for guidance only. They reflect the delays encountered in a typical design under worst-case conditions. Precise values for a particular design are provided by the timing analyzer.

### Clock Distribution Switching Characteristics

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
GCLK IOB and Buffer						
Global Clock PAD to output.	T <sub>GPIO</sub>	0.33	0.7	0.8	0.9	ns, max
Global Clock Buffer I input to O output	T <sub>GIO</sub>	0.34	0.7	0.8	0.9	ns, max

## CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Combinatorial Delays						
4-input function: F/G inputs to X/Y outputs	T <sub>ILO</sub>	0.29	0.6	0.7	0.8	ns, max
5-input function: F/G inputs to F5 output	T <sub>IF5</sub>	0.32	0.7	0.8	0.9	ns, max
5-input function: F/G inputs to X output	T <sub>IF5X</sub>	0.36	0.8	0.8	1.0	ns, max
6-input function: F/G inputs to Y output via F6 MUX	T <sub>IF6Y</sub>	0.44	0.9	1.0	1.2	ns, max
6-input function: F5IN input to Y output	T <sub>F5INY</sub>	0.17	0.32	0.36	0.42	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T <sub>IFNCTL</sub>	0.31	0.7	0.7	0.8	ns, max
BY input to YB output	T <sub>BYYB</sub>	0.27	0.53	0.6	0.7	ns, max
Sequential Delays						
FF Clock CLK to XQ/YQ outputs	T <sub>CKO</sub>	0.54	1.1	1.2	1.4	ns, max
Latch Clock CLK to XQ/YQ outputs	T <sub>CKLO</sub>	0.6	1.2	1.4	1.6	ns, max
Setup and Hold Times before/after Clock CLK <sup>(1)</sup>	Setup Time / Hold Time					
4-input function: F/G Inputs	T <sub>ICK</sub> /T <sub>CKI</sub>	0.6 / 0	1.2 / 0	1.4 / 0	1.5 / 0	ns, min
5-input function: F/G inputs	T <sub>IF5CK</sub> /T <sub>CKIF5</sub>	0.7 / 0	1.3 / 0	1.5 / 0	1.7 / 0	ns, min
6-input function: F5IN input	T <sub>F5INCK</sub> /T <sub>CKF5IN</sub>	0.46 / 0	1.0 / 0	1.1 / 0	1.2 / 0	ns, min
6-input function: F/G inputs via F6 MUX	T <sub>IF6CK</sub> /T <sub>CKIF6</sub>	0.8 / 0	1.5 / 0	1.7 / 0	1.9 / 0	ns, min
BX/BY inputs	T <sub>DICK</sub> /T <sub>CKDI</sub>	0.30 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
CE input	T <sub>CECK</sub> /T <sub>CKCE</sub>	0.37 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
SR/BY inputs (synchronous)	T <sub>RCK</sub> T <sub>CKR</sub>	0.33 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T <sub>CH</sub>	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low	T <sub>CL</sub>	0.8	1.5	1.7	2.0	ns, min
Set/Reset						
Minimum Pulse Width, SR/BY inputs	T <sub>RPW</sub>	1.3	2.5	2.8	3.3	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T <sub>RQ</sub>	0.54	1.1	1.3	1.4	ns, max
Delay from GSR to XQ/YQ outputs	T <sub>IOGSRQ</sub>	4.9	9.7	10.9	12.5	ns, max
Toggle Frequency (MHz) (for export control)	F <sub>TOG</sub> (MHz)	625	333	294	250	MHz

### Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

## CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Combinatorial Delays						
F operand inputs to X via XOR	T <sub>OPX</sub>	0.37	0.8	0.9	1.0	ns, max
F operand input to XB output	T <sub>OPXB</sub>	0.54	1.1	1.3	1.4	ns, max
F operand input to Y via XOR	T <sub>OPY</sub>	0.8	1.5	1.7	2.0	ns, max
F operand input to YB output	T <sub>OPYB</sub>	0.8	1.5	1.7	2.0	ns, max
F operand input to COUT output	T <sub>OPCYF</sub>	0.6	1.2	1.3	1.5	ns, max
G operand inputs to Y via XOR	T <sub>OPGY</sub>	0.46	1.0	1.1	1.2	ns, max
G operand input to YB output	T <sub>OPGYB</sub>	0.8	1.6	1.8	2.1	ns, max
G operand input to COUT output	T <sub>OPCYG</sub>	0.7	1.3	1.4	1.6	ns, max
BX initialization input to COUT	T <sub>BXCY</sub>	0.41	0.9	1.0	1.1	ns, max
CIN input to X output via XOR	T <sub>CINX</sub>	0.21	0.41	0.46	0.53	ns, max
CIN input to XB	T <sub>CINXB</sub>	0.02	0.04	0.05	0.06	ns, max
CIN input to Y via XOR	T <sub>CINY</sub>	0.23	0.46	0.52	0.6	ns, max
CIN input to YB	T <sub>CINYB</sub>	0.23	0.45	0.51	0.6	ns, max
CIN input to COUT output	T <sub>BYP</sub>	0.05	0.09	0.10	0.11	ns, max
Multiplier Operation						
F1/2 operand inputs to XB output via AND	T <sub>FANDXB</sub>	0.18	0.36	0.40	0.46	ns, max
F1/2 operand inputs to YB output via AND	T <sub>FANDYB</sub>	0.40	0.8	0.9	1.1	ns, max
F1/2 operand inputs to COUT output via AND	T <sub>FANDCY</sub>	0.22	0.43	0.48	0.6	ns, max
G1/2 operand inputs to YB output via AND	T <sub>GANDYB</sub>	0.25	0.50	0.6	0.7	ns, max
G1/2 operand inputs to COUT output via AND	T <sub>GANDCY</sub>	0.07	0.13	0.15	0.17	ns, max
Setup and Hold Times before/after Clock CLK <sup>(1)</sup>	Setup Time / Hold Time					
CIN input to FFX	T <sub>CCKX</sub> /T <sub>CKCX</sub>	0.50 / 0	1.0 / 0	1.2 / 0	1.3 / 0	ns, min
CIN input to FFY	T <sub>CCKY</sub> /T <sub>CKCY</sub>	0.53 / 0	1.1 / 0	1.2 / 0	1.4 / 0	ns, min

### Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

## CLB SelectRAM Switching Characteristics

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Sequential Delays						
Clock CLK to X/Y outputs (WE active) 16 x 1 mode	T <sub>SHCKO16</sub>	1.2	2.3	2.6	3.0	ns, max
Clock CLK to X/Y outputs (WE active) 32 x 1 mode	T <sub>SHCKO32</sub>	1.2	2.7	3.1	3.5	ns, max
Shift-Register Mode						
Clock CLK to X/Y outputs	T <sub>REG</sub>	1.2	3.7	4.1	4.7	ns, max
Setup and Hold Times before/after Clock CLK <sup>(1)</sup>	Setup Time / Hold Time					
F/G address inputs	T <sub>AS</sub> /T <sub>AH</sub>	0.25 / 0	0.5 / 0	0.6 / 0	0.7 / 0	ns, min
BX/BY data inputs (DIN)	T <sub>DS</sub> /T <sub>DH</sub>	0.34 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
CE input (WE)	T <sub>WS</sub> /T <sub>WH</sub>	0.38 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
Shift-Register Mode						
BX/BY data inputs (DIN)	T <sub>SHDICK</sub>	0.34	0.7	0.8	0.9	ns, min
CE input (WS)	T <sub>SHCECK</sub>	0.38	0.8	0.9	1.0	ns, min
Clock CLK						
Minimum Pulse Width, High	T <sub>WPH</sub>	1.2	2.4	2.7	3.1	ns, min
Minimum Pulse Width, Low	T <sub>WPL</sub>	1.2	2.4	2.7	3.1	ns, min
Minimum clock period to meet address write cycle time	T <sub>WC</sub>	2.4	4.8	5.4	6.2	ns, min
Shift-Register Mode						
Minimum Pulse Width, High	T <sub>SRPH</sub>	1.2	2.4	2.7	3.1	ns, min
Minimum Pulse Width, Low	T <sub>SRPL</sub>	1.2	2.4	2.7	3.1	ns, min

**Notes:**

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.



## Virtex Pinout Information

### Pinout Tables

See [www.xilinx.com](http://www.xilinx.com) for updates or additional pinout information. For convenience, Table 2, Table 3 and Table 4 list the locations of special-purpose and power-supply pins. Pins not listed are either user I/Os or not connected, depending on the device/package combination. See the Pinout Diagrams starting on page 17 for any pins not listed for a particular part/package combination.

Table 2: Virtex Pinout Tables (Chip-Scale and QFP Packages)

Pin Name	Device	CS144	TQ144	PQ/HQ240
GCK0	All	K7	90	92
GCK1	All	M7	93	89
GCK2	All	A7	19	210
GCK3	All	A6	16	213
M0	All	M1	110	60
M1	All	L2	112	58
M2	All	N2	108	62
CCLK	All	B13	38	179
PROGRAM	All	L12	72	122
DONE	All	M12	74	120
INIT	All	L13	71	123
BUSY/DOUT	All	C11	39	178
D0/DIN	All	C12	40	177
D1	All	E10	45	167
D2	All	E12	47	163
D3	All	F11	51	156
D4	All	H12	59	145
D5	All	J13	63	138
D6	All	J11	65	134
D7	All	K10	70	124
WRITE	All	C10	32	185
CS	All	D10	33	184
TDI	All	A11	34	183
TDO	All	A12	36	181
TMS	All	B1	143	2
TCK	All	C3	2	239
V <sub>CCINT</sub>	All	A9, B6, C5, G3, G12, M5, M9, N6	10, 15, 25, 57, 84, 94, 99, 126	16, 32, 43, 77, 88, 104, 137, 148, 164, 198, 214, 225

Table 2: Virtex Pinout Tables (Chip-Scale and QFP Packages) (Continued)

Pin Name	Device	CS144	TQ144	PQ/HQ240
$V_{CCO}$	All	Banks 0 and 1: A2, A13, D7 Banks 2 and 3: B12, G11, M13 Banks 4 and 5: N1, N7, N13 Banks 6 and 7: B2, G2, M2	No I/O Banks in this package: 1, 17, 37, 55, 73, 92, 109, 128	No I/O Banks in this package: 15, 30, 44, 61, 76, 90, 105, 121, 136, 150, 165, 180, 197, 212, 226, 240
$V_{REF}$ Bank 0 ( $V_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all $V_{REF}$ pins are general I/O.	XCV50	C4, D6	5, 13	218, 232
	XCV100/150	... + B4	... + 7	... + 229
	XCV200/300	N/A	N/A	... + 236
	XCV400	N/A	N/A	... + 215
	XCV600	N/A	N/A	... + 230
	XCV800	N/A	N/A	... + 222
$V_{REF}$ Bank 1 ( $V_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all $V_{REF}$ pins are general I/O.	XCV50	A10, B8	22, 30	191, 205
	XCV100/150	... + D9	... + 28	... + 194
	XCV200/300	N/A	N/A	... + 187
	XCV400	N/A	N/A	... + 208
	XCV600	N/A	N/A	... + 193
	XCV800	N/A	N/A	... + 201
$V_{REF}$ Bank 2 ( $V_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all $V_{REF}$ pins are general I/O.	XCV50	D11, F10	42, 50	157, 171
	XCV100/150	... + D13	... + 44	... + 168
	XCV200/300	N/A	N/A	... + 175
	XCV400	N/A	N/A	... + 154
	XCV600	N/A	N/A	... + 169
	XCV800	N/A	N/A	... + 161

Table 2: Virtex Pinout Tables (Chip-Scale and QFP Packages) (Continued)

Pin Name	Device	CS144	TQ144	PQ/HQ240
<b>V<sub>REF</sub> Bank 6</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	H2, K1	116, 123	36, 50
	XCV100/150	... + J3	... + 118	... + 47
	XCV200/300	N/A	N/A	... + 54
	XCV400	N/A	N/A	... + 33
	XCV600	N/A	N/A	... + 48
	XCV800	N/A	N/A	... + 40
<b>V<sub>REF</sub> Bank 7</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	D4, E1	133, 140	9, 23
	XCV100/150	... + D2	... + 138	... + 12
	XCV200/300	N/A	N/A	... + 5
	XCV400	N/A	N/A	... + 26
	XCV600	N/A	N/A	... + 11
	XCV800	N/A	N/A	... + 19
<b>GND</b>	All	A1, B9, B11, C7, D5, E4, E11, F1, G10, J1, J12, L3, L5, L7, L9, N12	9, 18, 26, 35, 46, 54, 64, 75, 83, 91, 100, 111, 120, 129, 136, 144,	1, 8, 14, 22, 29, 37, 45, 51, 59, 69, 75, 83, 91, 98, 106, 112, 119, 129, 135, 143, 151, 158, 166, 172, 182, 190, 196, 204, 211, 219, 227, 233

Table 4: Virtex Pinout Tables (Fine-Pitch BGA) (Continued)

Pin Name	Device	FG256	FG456	FG676	FG680
$V_{REF}$ Bank 7 ( $V_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all $V_{REF}$ pins are general I/O.	XCV50	C1, H3	N/A	N/A	N/A
	XCV100/150	... + D1	E2, H4, K3	N/A	N/A
	XCV200/300	... + B1	... + D2	N/A	N/A
	XCV400	N/A	N/A	F4, G4, K6, M2, M5	N/A
	XCV600	N/A	N/A	... + H1	E38, G38, L36, N36, U36, U38
	XCV800	N/A	N/A	... + K1	... + N38
	XCV1000	N/A	N/A	N/A	... + F36
GND	All	A1, A16, B2, B15, F6, F7, F10, F11, G6, G7, G8, G9, G10, G11, H7, H8, H9, H10, J7, J8, J9, J10, K6, K7, K8, K9, K10, K11, L6, L7, L10, L11, R2, R15, T1, T16	A1, A22, B2, B21, C3, C20, J9, J10, J11, J12, J13, J14, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N9, N10, N11, N12, N13, N14, P9, P10, P11, P12, P13, P14, Y3, Y20, AA2, AA21, AB1, AB22	A1, A26, B2, B9, B14, B18, B25, C3, C24, D4, D23, E5, E22, J2, J25, K10, K11, K12, K13, K14, K15, K16, K17, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N2, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, P25, R10, R11, R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17, V2, V25, AB5, AB22, AC4, AC23, AD3, AD24, AE2, AE9, AE13, AE18, AE25, AF1, AF26	A1, A2, A3, A37, A38, A39, AA5, AA35, AH4, AH5, AH35, AH36, AR5, AR12, AR19, AR20, AR21, AR28, AR35, AT4, AT12, AT20, AT28, AT36, AU1, AU3, AU20, AU37, AU39, AV1, AV2, AV38, AV39, AW1, AW2, AW3, AW37, AW38, AW39, B1, B2, B38, B39, C1, C3, C20, C37, C39, D4, D12, D20, D28, D36, E5, E12, E19, E20, E21, E28, E35, M4, M5, M35, M36, W5, W35, Y3, Y4, Y5, Y35, Y36, Y37

## PQ240/HQ240 Pin Function Diagram

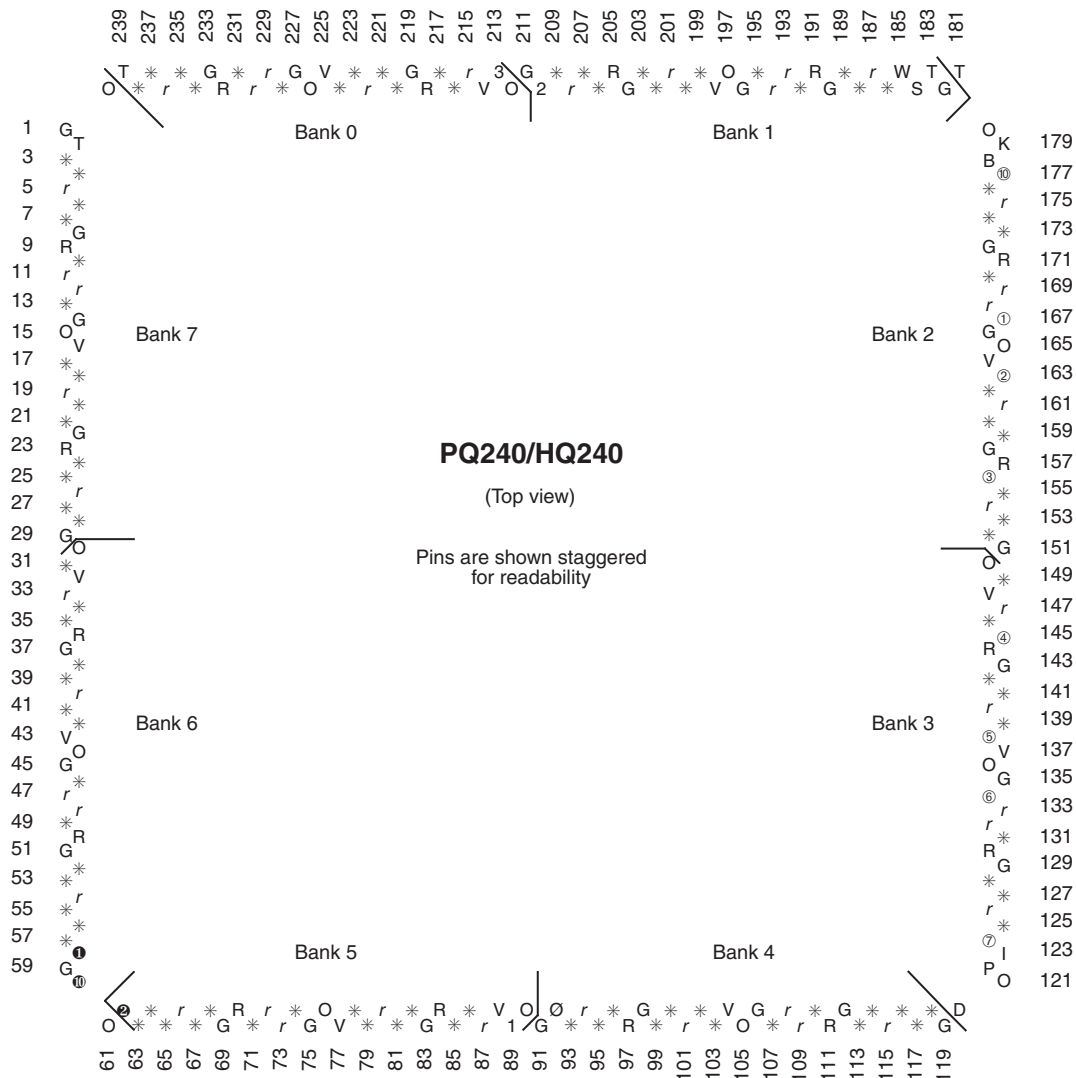
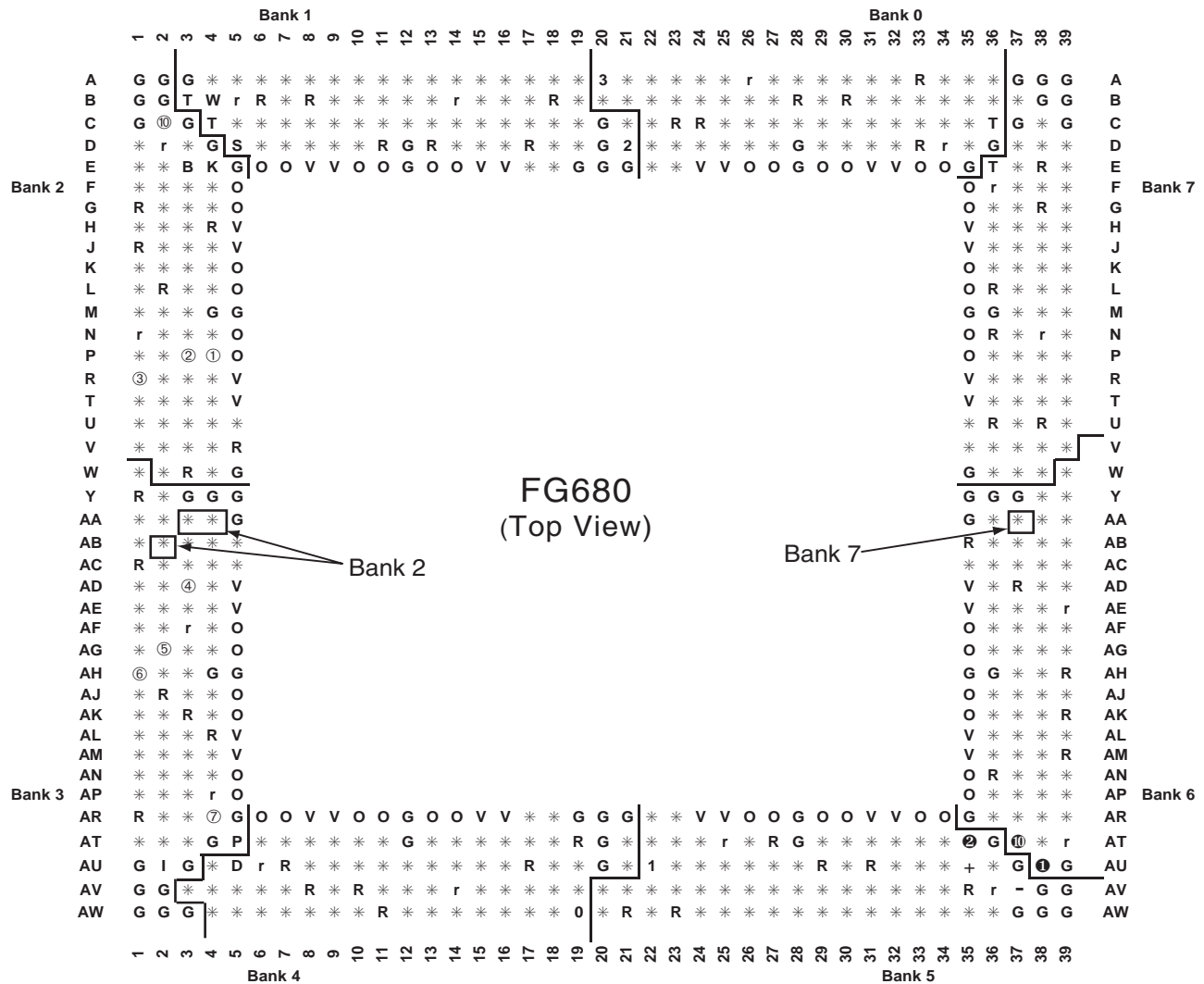


Figure 3: PQ240/HQ240 Pin Function Diagram

# FG680 Pin Function Diagram



Note: AA3, AA4, and AB2 are in Bank 2

Note: AA37 is in Bank 7

fg680\_12a

Figure 11: FG680 Pin Function Diagram