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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	384
Number of Logic Elements/Cells	1728
Total RAM Bits	32768
Number of I/O	94
Number of Gates	57906
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-TFBGA, CSPBGA
Supplier Device Package	144-LCSBGA (12x12)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xcv50-5cs144i">https://www.e-xfl.com/product-detail/xilinx/xcv50-5cs144i</a>

## Revision History

Date	Version	Revision
11/98	1.0	Initial Xilinx release.
01/99-02/99	1.2-1.3	Both versions updated package drawings and specs.
05/99	1.4	Addition of package drawings and specifications.
05/99	1.5	Replaced FG 676 & FG680 package drawings.
07/99	1.6	Changed Boundary Scan Information and changed Figure 11, Boundary Scan Bit Sequence. Updated IOB Input & Output delays. Added Capacitance info for different I/O Standards. Added 5 V tolerant information. Added DLL Parameters and waveforms and new Pin-to-pin Input and Output Parameter tables for Global Clock Input to Output and Setup and Hold. Changed Configuration Information including Figures 12, 14, 17 & 19. Added device-dependent listings for quiescent currents ICCINTQ and ICCOQ. Updated IOB Input and Output Delays based on default standard of LVTTTL, 12 mA, Fast Slew Rate. Added IOB Input Switching Characteristics Standard Adjustments.
09/99	1.7	Speed grade update to preliminary status, Power-on specification and Clock-to-Out Minimums additions, "0" hold time listing explanation, quiescent current listing update, and Figure 6 ADDRA input label correction. Added T <sub>IJITCC</sub> parameter, changed T <sub>OJIT</sub> to T <sub>OPHASE</sub> .
01/00	1.8	Update to speed.txt file 1.96. Corrections for CRs 111036, 111137, 112697, 115479, 117153, 117154, and 117612. Modified notes for Recommended Operating Conditions (voltage and temperature). Changed Bank information for V <sub>CCO</sub> in CS144 package on p.43.
01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
03/00	2.0	New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration.
05/00	2.1	Modified "Pins not listed..." statement. Speed grade update to Final status.
05/00	2.2	Modified Table 18.
09/00	2.3	<ul style="list-style-type: none"> <li>Added XCV400 values to table under <b>Minimum Clock-to-Out for Virtex Devices</b>.</li> <li>Corrected Units column in table under <b>IOB Input Switching Characteristics</b>.</li> <li>Added values to table under <b>CLB SelectRAM Switching Characteristics</b>.</li> </ul>
10/00	2.4	<ul style="list-style-type: none"> <li>Corrected Pinout information for devices in the BG256, BG432, and BG560 packages in Table 18.</li> <li>Corrected <b>BG256 Pin Function Diagram</b>.</li> </ul>
04/01	2.5	<ul style="list-style-type: none"> <li>Revised minimums for <b>Global Clock Set-Up and Hold for LVTTTL Standard, with DLL</b>.</li> <li>Converted file to modularized format. See <b>Virtex Data Sheet</b> section.</li> </ul>
03/13	4.0	The products listed in this data sheet are obsolete. See <a href="#">XCN10016</a> for further information.

## Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

- DS003-1, Virtex 2.5V FPGAs:  
Introduction and Ordering Information (Module 1)
- DS003-2, Virtex 2.5V FPGAs:  
Functional Description (Module 2)
- DS003-3, Virtex 2.5V FPGAs:  
DC and Switching Characteristics (Module 3)
- DS003-4, Virtex 2.5V FPGAs:  
Pinout Tables (Module 4)

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is

selected either from these pads or from signals in the general purpose routing.

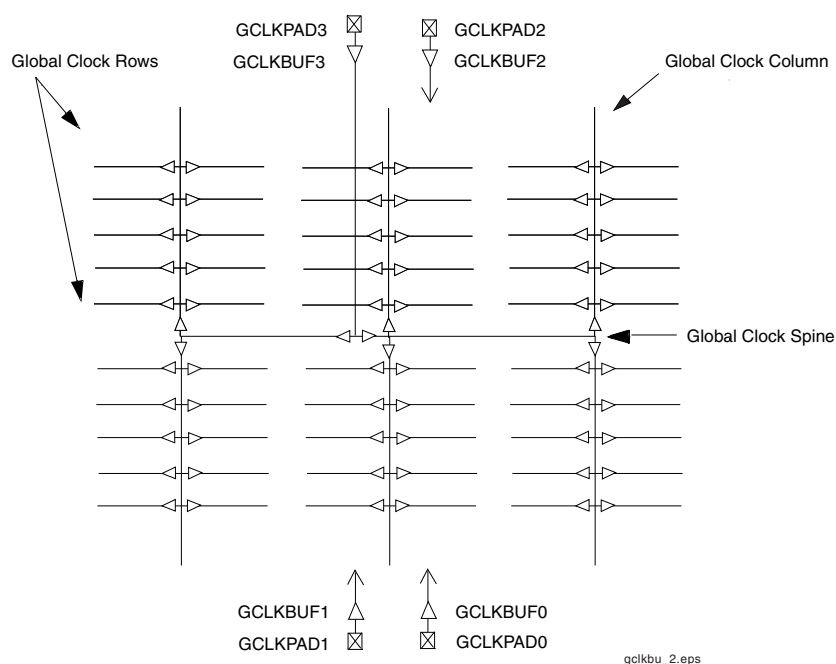


Figure 9: Global Clock Distribution Network

### Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Clock edges reach internal flip-flops one to four clock periods after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to de-skew a board level clock among multiple Virtex devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

See **DLL Timing Parameters**, page 21 of Module 3, for frequency range information.

### Boundary Scan

Virtex devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, and HIGHZ instructions. The TAP also supports two internal scan chains and configuration/readback of the device. The TAP uses dedicated package pins that always operate using LVTTTL. For TDO to operate using LVTTTL, the  $V_{CCO}$  for Bank 2 should be 3.3 V. Otherwise, TDO switches rail-to-rail between ground and  $V_{CCO}$ .

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including un-bonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections, provided the user design or application is turned off.

**Table 5** lists the boundary-scan instructions supported in Virtex FPGAs. Internal signals can be captured during EXTEST by connecting them to un-bonded or unused IOBs. They can also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Before the device is configured, all instructions except USER1 and USER2 are available. After configuration, all instructions are available. During configuration, it is recommended that those operations using the boundary-scan register (SAMPLE/PRELOAD, INTEST, EXTEST) not be performed.

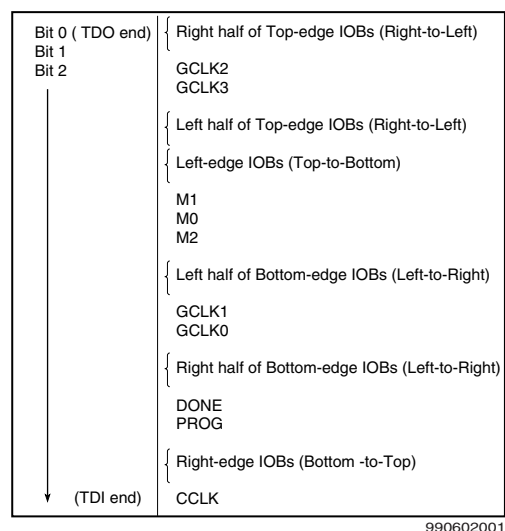


Figure 11: Boundary Scan Bit Sequence

Table 5: Boundary Scan Instructions

Boundary-Scan Command	Binary Code(4:0)	Description
EXTEST	00000	Enables boundary-scan EXTEST operation
SAMPLE/PRELOAD	00001	Enables boundary-scan SAMPLE/PRELOAD operation
USER 1	00010	Access user-defined register 1
USER 2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for read operations.
CFG_IN	00101	Access the configuration bus for write operations.
INTEST	00111	Enables boundary-scan INTEST operation
USERCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIGHZ	01010	3-states output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

## Identification Registers

The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined.

The IDCODE register has the following binary format:

vvvv:ffff:ffa:aaaa:aaaa:cccc:cccc:ccc1

where

v = the die version number

f = the family code (03h for Virtex family)

a = the number of CLB rows (ranges from 010h for XCV50 to 040h for XCV1000)

c = the company code (49h for Xilinx)

The USERCODE register is supported. By using the USER-CODE, a user-programmable identification code can be loaded and shifted out for examination. The identification code is embedded in the bitstream during bitstream generation and is valid only after configuration.

Table 6: IDCODEs Assigned to Virtex FPGAs

FPGA	IDCODE
XCV50	v0610093h
XCV100	v0614093h
XCV150	v0618093h
XCV200	v061C093h
XCV300	v0620093h
XCV400	v0628093h
XCV600	v0630093h
XCV800	v0638093h
XCV1000	v0640093h

## Including Boundary Scan in a Design

Since the boundary scan pins are dedicated, no special element needs to be added to the design unless an internal data register (USER1 or USER2) is desired.

If an internal data register is used, insert the boundary scan symbol and connect the necessary pins as appropriate.

## Development System

Virtex FPGAs are supported by the Xilinx Foundation and Alliance CAE tools. The basic methodology for Virtex design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation (for example, Synopsys FPGA Express), while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under the Xilinx Design Manager (XDM™) software, providing design-

ers with a common user interface regardless of their choice of entry and verification tools. The XDM software simplifies the selection of implementation options with pull-down menus and on-line help.

Application programs ranging from schematic capture to Placement and Routing (PAR) can be accessed through the XDM software. The program command sequence is generated prior to execution, and stored for documentation.

Several advanced software features facilitate Virtex design. RPMs, for example, are schematic-based macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the Xilinx FPGA Foundation development system provides interfaces to the following synthesis design environments.

- Synopsys (FPGA Compiler, FPGA Express)
- Exemplar (Spectrum)
- Synplicity (Synplify)

For schematic design entry, the Xilinx FPGA Foundation and alliance development system provides interfaces to the following schematic-capture design environments.

- Mentor Graphics V8 (Design Architect, QuickSim II)
- Viewlogic Systems (Viewdraw)

Third-party vendors support many other environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Virtex FPGAs supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The “soft macro” portion of the library contains detailed descriptions of common logic functions, but does not contain any partitioning or placement information. The performance of these macros depends, therefore, on the partitioning and placement obtained during implementation.

RPMs, on the other hand, do contain predetermined partitioning and placement information that permits optimal implementation of these functions. Users can create their own library of soft macros or RPMs based on the macros and primitives in the standard library.

The design environment supports hierarchical design entry, with high-level schematics that comprise major functional blocks, while lower-level schematics define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical

design, thus allowing the most convenient entry method to be used for each portion of the design.

## Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF net list for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floor planning.

The implementation software incorporates Timing Wizard® timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered on a schematic in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

## Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the net list for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the TRACE® static timing analyzer.

For in-circuit debugging, the development system includes a download and readback cable. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

## Configuration

Virtex devices are configured by loading configuration data into the internal configuration memory. Some of the pins used for this are dedicated configuration pins, while others can be re-used as general purpose inputs and outputs once configuration is complete.

The following are dedicated pins:

- Mode pins (M2, M1, M0)
- Configuration clock pin (CCLK)
- $\overline{\text{PROGRAM}}$  pin
- DONE pin
- Boundary-scan pins (TDI, TDO, TMS, TCK)

Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or it can be generated externally and provided to the FPGA as an input. The  $\overline{\text{PROGRAM}}$  pin must be pulled High prior to reconfiguration.

Note that some configuration pins can act as outputs. For correct operation, these pins can require a  $V_{\text{CCO}}$  of 3.3 V to permit LVTTTL operation. All the pins affected are in banks 2 or 3. The configuration pins needed for SelectMap (CS, Write) are located in bank 1.

Table 7: Configuration Codes

Configuration Mode	M2	M1	M0	CCLK Direction	Data Width	Serial D <sub>out</sub>	Configuration Pull-ups
Master-serial mode	0	0	0	Out	1	Yes	No
Boundary-scan mode	1	0	1	N/A	1	No	No
SelectMAP mode	1	1	0	In	8	No	No
Slave-serial mode	1	1	1	In	1	Yes	No
Master-serial mode	1	0	0	Out	1	Yes	Yes
Boundary-scan mode	0	0	1	N/A	1	No	Yes
SelectMAP mode	0	1	0	In	8	No	Yes
Slave-serial mode	0	1	1	In	1	Yes	Yes

### Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other source of serial configuration data. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

For more information on serial PROMs, see the PROM data sheet at:

<http://www.xilinx.com/bvdocs/publications/ds026.pdf>.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin. The data on the DOUT pin changes on the rising edge of CCLK.

The change of DOUT on the rising edge of CCLK differs from previous families, but does not cause a problem for

After Virtex devices are configured, unused IOBs function as 3-state OBUFTs with weak pull downs. For a more detailed description than that given below, see the XAPP138, Virtex Configuration and Readback.

## Configuration Modes

Virtex supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- SelectMAP mode
- Boundary-scan mode

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in Table 7.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected. However, it is recommended to drive the configuration mode pins externally.

mixed configuration chains. This change was made to improve serial configuration rates for Virtex-only chains.

Figure 12 shows a full master/slave system. A Virtex device in slave-serial mode should be connected as shown in the third device from the left.

Slave-serial mode is selected by applying <111> or <011> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave-serial the default mode if the pins are left unconnected. However, it is recommended to drive the configuration mode pins externally. Figure 13 shows slave-serial mode programming switching characteristics.

Table 8 provides more detail about the characteristics shown in Figure 13. Configuration must be delayed until the  $\overline{\text{INIT}}$  pins of all daisy-chained FPGAs are High.

## Master-Serial Mode

In master-serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM that feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge.

The interface is identical to slave-serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration. Switching to a lower frequency is prohibited.

The CCLK frequency is set using the ConfigRate option in the bitstream generation software. The maximum CCLK frequency that can be selected is 60 MHz. When selecting a CCLK frequency, ensure that the serial PROM and any

daisy-chained FPGAs are fast enough to support the clock rate.

On power-up, the CCLK frequency is 2.5 MHz. This frequency is used until the ConfigRate bits have been loaded when the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz.

Figure 12 shows a full master/slave system. In this system, the left-most device operates in master-serial mode. The remaining devices operate in slave-serial mode. The SPROM RESET pin is driven by INIT, and the CE input is driven by DONE. There is the potential for contention on the DONE pin, depending on the start-up sequence options chosen.

Figure 14 shows the timing of master-serial configuration. Master-serial mode is selected by a <000> or <100> on the mode pins (M2, M1, M0). Table 8 shows the timing information for Figure 14.

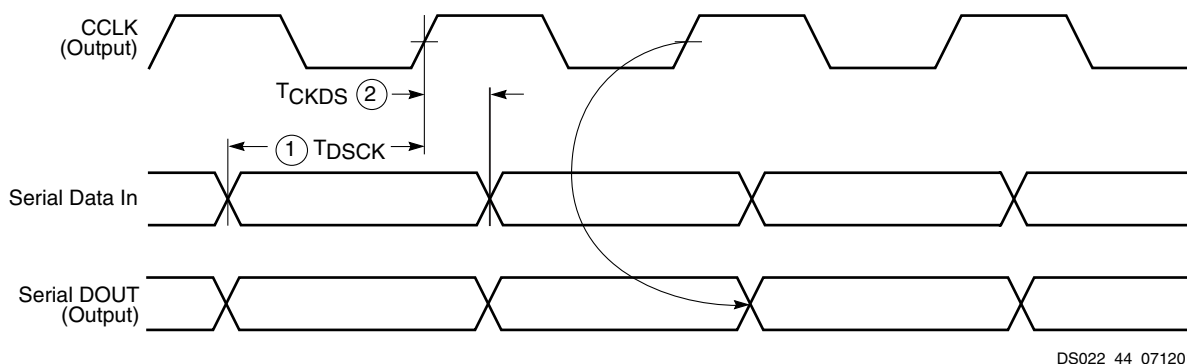


Figure 14: Master-Serial Mode Programming Switching Characteristics

At power-up,  $V_{CC}$  must rise from 1.0 V to  $V_{CC}$  min in less than 50 ms, otherwise delay configuration by pulling PROGRAM Low until  $V_{CC}$  is valid.

The sequence of operations necessary to configure a Virtex FPGA serially appears in Figure 15.

## SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the FPGA with a BUSY flag controlling the flow of data.

An external data source provides a byte stream, CCLK, a Chip Select ( $\overline{CS}$ ) signal and a Write signal ( $\overline{WRITE}$ ). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

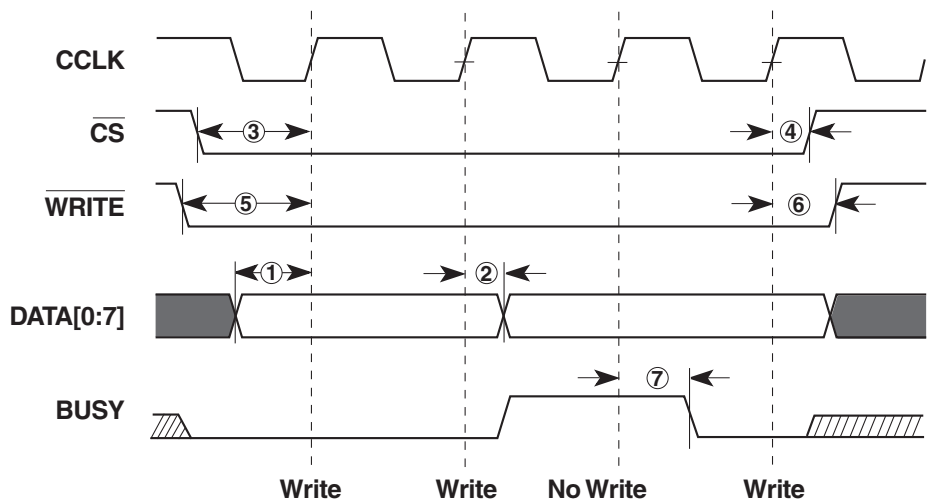
Data can also be read using the SelectMAP mode. If  $\overline{WRITE}$  is not asserted, configuration data is read out of the FPGA as part of a readback operation.

In the SelectMAP mode, multiple Virtex devices can be chained in parallel. DATA pins (D7:D0), CCLK,  $\overline{WRITE}$ ,  $\overline{BUSY}$ ,  $\overline{PROGRAM}$ ,  $\overline{DONE}$ , and  $\overline{INIT}$  can be connected in parallel between all the FPGAs. Note that the data is organized with the MSB of each byte on pin DO and the LSB of each byte on D7. The  $\overline{CS}$  pins are kept separate, insuring that each FPGA can be selected individually.  $\overline{WRITE}$  should be Low before loading the first bitstream and returned High after the last device has been programmed. Use  $\overline{CS}$  to select the appropriate FPGA for loading the bitstream and sending the configuration data. at the end of the bitstream, deselect the loaded device and select the next target FPGA by setting its  $\overline{CS}$  pin High. A free-running oscillator or other externally generated signal can be used for CCLK. The  $\overline{BUSY}$  signal can be ignored for frequencies below 50 MHz. For details about frequencies above 50 MHz, see XAPP138, Virtex Configuration and Readback. Once all the devices have been programmed, the  $\overline{DONE}$  pin goes High.

3. At the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this has happened.
4. Repeat steps 2 and 3 until all the data has been sent.

5. De-assert  $\overline{\text{CS}}$  and  $\overline{\text{WRITE}}$ .

A flowchart for the write operation appears in [Figure 17](#). Note that if CCLK is slower than  $f_{\text{CCNH}}$ , the FPGA never asserts BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.



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Figure 16: Write Operations

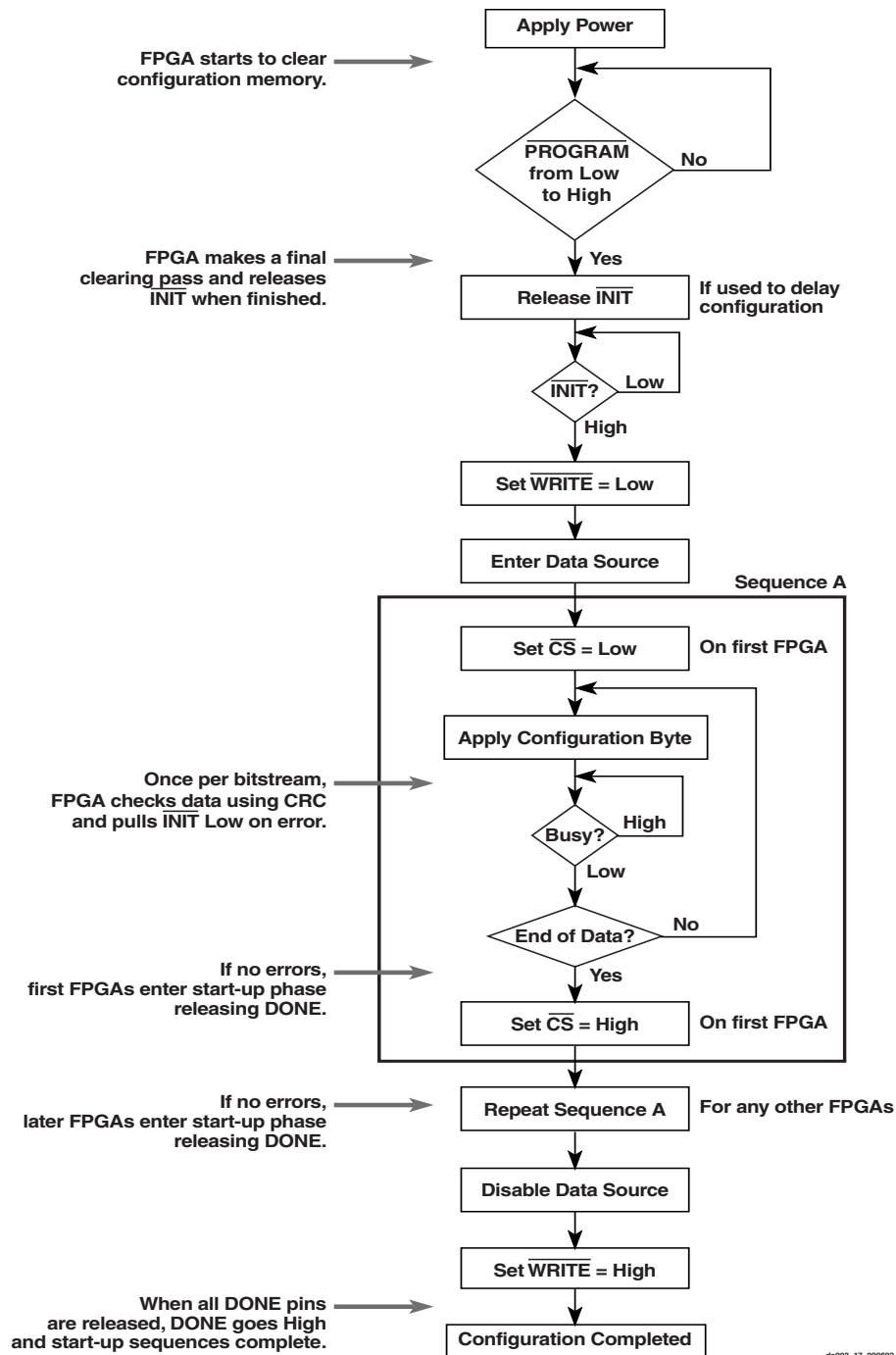


Figure 17: SelectMAP Flowchart for Write Operation

### Abort

During a given assertion of  $\overline{CS}$ , the user cannot switch from a write to a read, or vice-versa. This action causes the current packet command to be aborted. The device will remain BUSY until the aborted operation has completed. Following an abort, data is assumed to be unaligned to word boundar-

ies, and the FPGA requires a new synchronization word prior to accepting any new packets.

To initiate an abort during a write operation, de-assert  $\overline{WRITE}$ . At the rising edge of CCLK, an abort is initiated, as shown in Figure 18.

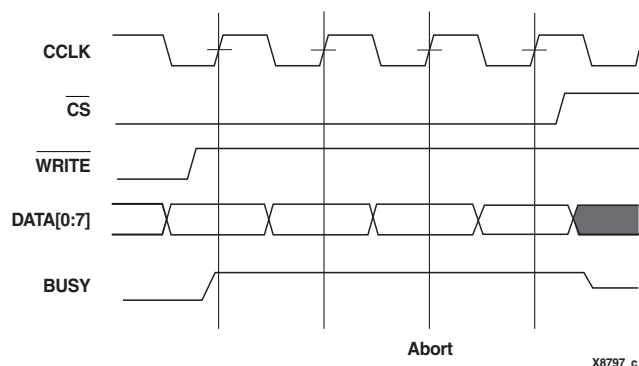


Figure 18: SelectMAP Write Abort Waveforms

## Boundary-Scan Mode

In the boundary-scan mode, configuration is done through the IEEE 1149.1 Test Access Port. Note that the **PROGRAM** pin must be pulled High prior to reconfiguration. A Low on the **PROGRAM** pin resets the TAP controller and no JTAG operations can be performed.

Configuration through the TAP uses the **CFG\_IN** instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port (when using TCK as a start-up clock).

1. Load the **CFG\_IN** instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the **JSTART** instruction into IR
6. Enter the SDR state
7. Clock TCK through the startup sequence
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode is selected by a <101> or 001> on the mode pins (M2, M1, M0). For details on TAP characteristics, refer to XAPP139.

## Configuration Sequence

The configuration of Virtex devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user, as described below. The configuration process can also be initiated by asserting **PROGRAM**.

The end of the memory-clearing phase is signalled by **INIT** going High, and the completion of the entire process is signalled by **DONE** going High.

The power-up timing of configuration signals is shown in Figure 19. The corresponding timing characteristics are listed in Table 10.

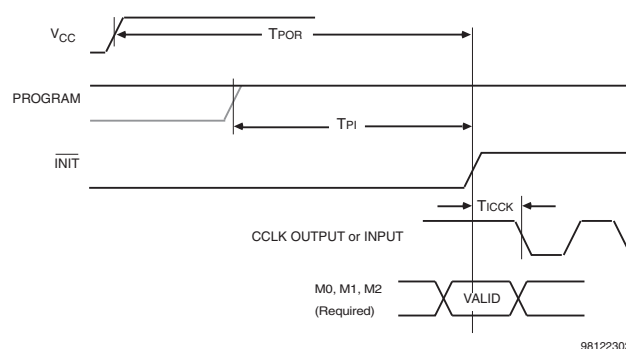


Figure 19: Power-Up Timing Configuration Signals

Table 10: Power-up Timing Characteristics

Description	Symbol	Value	Units
Power-on Reset	T <sub>POR</sub>	2.0	ms, max
Program Latency	T <sub>PL</sub>	100.0	μs, max
CCLK (output) Delay	T <sub>ICCK</sub>	0.5	μs, min
		4.0	μs, max
Program Pulse Width	T <sub>PROGRAM</sub>	300	ns, min

## Delaying Configuration

**INIT** can be held Low using an open-drain driver. An open-drain is required since **INIT** is a bidirectional open-drain pin that is held Low by the FPGA while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

## Start-Up Sequence

The default Start-up sequence is that one CCLK cycle after **DONE** goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed. In addition, the GTS, GSR, and GWE events can be made dependent on the **DONE** pins of multiple devices all going High, forcing the devices to start in synchronism. The sequence can also be paused at any stage until lock has been achieved on any or all DLLs.

## Virtex DC Characteristics

### Absolute Maximum Ratings

Symbol	Description <sup>(1)</sup>			Units
$V_{CCINT}$	Supply voltage relative to GND <sup>(2)</sup>		–0.5 to 3.0	V
$V_{CCO}$	Supply voltage relative to GND <sup>(2)</sup>		–0.5 to 4.0	V
$V_{REF}$	Input Reference Voltage		–0.5 to 3.6	V
$V_{IN}$	Input voltage relative to GND <sup>(3)</sup>	Using $V_{REF}$	–0.5 to 3.6	V
		Internal threshold	–0.5 to 5.5	V
$V_{TS}$	Voltage applied to 3-state output		–0.5 to 5.5	V
$V_{CC}$	Longest Supply Voltage Rise Time from 1V-2.375V		50	ms
$T_{STG}$	Storage temperature (ambient)		–65 to +150	°C
$T_J$	Junction temperature <sup>(4)</sup>	Plastic Packages	+125	°C

**Notes:**

- Stresses beyond those listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time can affect device reliability.
- Power supplies can turn on in any order.
- For protracted periods (e.g., longer than a day),  $V_{IN}$  should not exceed  $V_{CCO}$  by more than 3.6 V.
- For soldering guidelines and thermal considerations, see the "Device Packaging" information on [www.xilinx.com](http://www.xilinx.com).

### Recommended Operating Conditions

Symbol	Description		Min	Max	Units
$V_{CCINT}^{(1)}$	Input Supply voltage relative to GND, $T_J = 0\text{ °C to }+85\text{ °C}$	Commercial	2.5 – 5%	2.5 + 5%	V
	Input Supply voltage relative to GND, $T_J = -40\text{ °C to }+100\text{ °C}$	Industrial	2.5 – 5%	2.5 + 5%	V
$V_{CCO}^{(4)}$	Supply voltage relative to GND, $T_J = 0\text{ °C to }+85\text{ °C}$	Commercial	1.4	3.6	V
	Supply voltage relative to GND, $T_J = -40\text{ °C to }+100\text{ °C}$	Industrial	1.4	3.6	V
$T_{IN}$	Input signal transition time			250	ns

**Notes:**

- Correct operation is guaranteed with a minimum  $V_{CCINT}$  of 2.375 V (Nominal  $V_{CCINT}$  –5%). Below the minimum value, all delay parameters increase by 3% for each 50-mV reduction in  $V_{CCINT}$  below the specified range.
- At junction temperatures above those listed as Operating Conditions, delay parameters do increase. Please refer to the TRCE report.
- Input and output measurement threshold is ~50% of  $V_{CC}$ .
- Min and Max values for  $V_{CCO}$  are I/O Standard dependant.

### DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Device	Min	Max	Units
$V_{DRINT}$	Data Retention $V_{CCINT}$ Voltage (below which configuration data can be lost)	All	2.0		V
$V_{DRIO}$	Data Retention $V_{CCO}$ Voltage (below which configuration data can be lost)	All	1.2		V
$I_{CCINTQ}$	Quiescent $V_{CCINT}$ supply current <sup>(1,3)</sup>	XCV50		50	mA
		XCV100		50	mA
		XCV150		50	mA
		XCV200		75	mA
		XCV300		75	mA
		XCV400		75	mA
		XCV600		100	mA
		XCV800		100	mA
		XCV1000		100	mA
$I_{CCOQ}$	Quiescent $V_{CCO}$ supply current <sup>(1)</sup>	XCV50		2	mA
		XCV100		2	mA
		XCV150		2	mA
		XCV200		2	mA
		XCV300		2	mA
		XCV400		2	mA
		XCV600		2	mA
		XCV800		2	mA
		XCV1000		2	mA
$I_{REF}$	$V_{REF}$ current per $V_{REF}$ pin	All		20	$\mu$ A
$I_L$	Input or output leakage current	All	-10	+10	$\mu$ A
$C_{IN}$	Input capacitance (sample tested)	BGA, PQ, HQ, packages		8	pF
$I_{RPU}$	Pad pull-up (when selected) @ $V_{in} = 0$ V, $V_{CCO} = 3.3$ V (sample tested)	All	Note (2)	0.25	mA
$I_{RPD}$	Pad pull-down (when selected) @ $V_{in} = 3.6$ V (sample tested)		Note (2)	0.15	mA

#### Notes:

1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.
3. Multiply  $I_{CCINTQ}$  limit by two for industrial grade.

### IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Description	Symbol	Standard <sup>(1)</sup>	Speed Grade				Unit s
			Min	-6	-5	-4	
Output Delay Adjustments							
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T <sub>OLVTTL_S2</sub>	LVTTL, Slow, 2 mA	4.2	14.7	15.8	17.0	ns
	T <sub>OLVTTL_S4</sub>	4 mA	2.5	7.5	8.0	8.6	ns
	T <sub>OLVTTL_S6</sub>	6 mA	1.8	4.8	5.1	5.6	ns
	T <sub>OLVTTL_S8</sub>	8 mA	1.2	3.0	3.3	3.5	ns
	T <sub>OLVTTL_S12</sub>	12 mA	1.0	1.9	2.1	2.2	ns
	T <sub>OLVTTL_S16</sub>	16 mA	0.9	1.7	1.9	2.0	ns
	T <sub>OLVTTL_S24</sub>	24 mA	0.8	1.3	1.4	1.6	ns
	T <sub>OLVTTL_F2</sub>	LVTTL, Fast, 2mA	1.9	13.1	14.0	15.1	ns
	T <sub>OLVTTL_F4</sub>	4 mA	0.7	5.3	5.7	6.1	ns
	T <sub>OLVTTL_F6</sub>	6 mA	0.2	3.1	3.3	3.6	ns
	T <sub>OLVTTL_F8</sub>	8 mA	0.1	1.0	1.1	1.2	ns
	T <sub>OLVTTL_F12</sub>	12 mA	0	0	0	0	ns
	T <sub>OLVTTL_F16</sub>	16 mA	−0.10	−0.05	−0.05	−0.05	ns
	T <sub>OLVTTL_F24</sub>	24 mA	−0.10	−0.20	−0.21	−0.23	ns
	T <sub>OLVCMOS2</sub>	LVC MOS2	0.10	0.10	0.11	0.12	ns
	T <sub>OPCI33_3</sub>	PCI, 33 MHz, 3.3 V	0.50	2.3	2.5	2.7	ns
	T <sub>OPCI33_5</sub>	PCI, 33 MHz, 5.0 V	0.40	2.8	3.0	3.3	ns
	T <sub>OPCI66_3</sub>	PCI, 66 MHz, 3.3 V	0.10	−0.40	−0.42	−0.46	ns
	T <sub>OGTL</sub>	GTL	0.6	0.50	0.54	0.6	ns
	T <sub>OGTLP</sub>	GTL+	0.7	0.8	0.9	1.0	ns
	T <sub>OHSTL_I</sub>	HSTL I	0.10	−0.50	−0.53	−0.5	ns
	T <sub>OHSTL_III</sub>	HSTL III	−0.10	−0.9	−0.9	−1.0	ns
	T <sub>OHSTL_IV</sub>	HSTL IV	−0.20	−1.0	−1.0	−1.1	ns
	T <sub>OSSTL2_I</sub>	SSTL2 I	−0.10	−0.50	−0.53	−0.5	ns
	T <sub>OSSTL2_II</sub>	SSTL2 II	−0.20	−0.9	−0.9	−1.0	ns
	T <sub>OSSTL3_I</sub>	SSTL3 I	−0.20	−0.50	−0.53	−0.5	ns
	T <sub>OSSTL3_II</sub>	SSTL3 II	−0.30	−1.0	−1.0	−1.1	ns
	T <sub>OCTT</sub>	CTT	0	−0.6	−0.6	−0.6	ns
	T <sub>OAGP</sub>	AGP	0	−0.9	−0.9	−1.0	ns

#### Notes:

- Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTTL. For other I/O standards and different loads, see [Table 2](#) and [Table 3](#).

## Calculation of $T_{i\text{oop}}$ as a Function of Capacitance

$T_{i\text{oop}}$  is the propagation delay from the O Input of the IOB to the pad. The values for  $T_{i\text{oop}}$  were based on the standard capacitive load ( $C_{sl}$ ) for each I/O standard as listed in [Table 2](#).

Table 2: Constants for Calculating  $T_{i\text{oop}}$

Standard	Csl (pF)	fl (ns/pF)
LVTTL Fast Slew Rate, 2mA drive	35	0.41
LVTTL Fast Slew Rate, 4mA drive	35	0.20
LVTTL Fast Slew Rate, 6mA drive	35	0.13
LVTTL Fast Slew Rate, 8mA drive	35	0.079
LVTTL Fast Slew Rate, 12mA drive	35	0.044
LVTTL Fast Slew Rate, 16mA drive	35	0.043
LVTTL Fast Slew Rate, 24mA drive	35	0.033
LVTTL Slow Slew Rate, 2mA drive	35	0.41
LVTTL Slow Slew Rate, 4mA drive	35	0.20
LVTTL Slow Slew Rate, 6mA drive	35	0.100
LVTTL Slow Slew Rate, 8mA drive	35	0.086
LVTTL Slow Slew Rate, 12mA drive	35	0.058
LVTTL Slow Slew Rate, 16mA drive	35	0.050
LVTTL Slow Slew Rate, 24mA drive	35	0.048
LVCMS2	35	0.041
PCI 33MHz 5V	50	0.050
PCI 33MHZ 3.3 V	10	0.050
PCI 66 MHz 3.3 V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

### Notes:

1. I/O parameter measurements are made with the capacitance values shown above. See Application Note XAPP133 on [www.xilinx.com](http://www.xilinx.com) for appropriate terminations.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

For other capacitive loads, use the formulas below to calculate the corresponding  $T_{i\text{oop}}$ .

$$T_{i\text{oop}} = T_{i\text{oop}} + T_{\text{opadjust}} + (C_{\text{load}} - C_{sl}) * fl$$

Where:

$T_{\text{opadjust}}$  is reported above in the Output Delay Adjustment section.

$C_{\text{load}}$  is the capacitive load for the design.

Table 3: Delay Measurement Methodology

Standard	$V_L$ (1)	$V_H$ (1)	Meas. Point	$V_{REF}$ Typ (2)
LVTTL	0	3	1.4	-
LVCMS2	0	2.5	1.125	-
PCI33_5	Per PCI Spec			-
PCI33_3	Per PCI Spec			-
PCI66_3	Per PCI Spec			-
GTL	$V_{REF} - 0.2$	$V_{REF} + 0.2$	$V_{REF}$	0.80
GTL+	$V_{REF} - 0.2$	$V_{REF} + 0.2$	$V_{REF}$	1.0
HSTL Class I	$V_{REF} - 0.5$	$V_{REF} + 0.5$	$V_{REF}$	0.75
HSTL Class III	$V_{REF} - 0.5$	$V_{REF} + 0.5$	$V_{REF}$	0.90
HSTL Class IV	$V_{REF} - 0.5$	$V_{REF} + 0.5$	$V_{REF}$	0.90
SSTL3 I & II	$V_{REF} - 1.0$	$V_{REF} + 1.0$	$V_{REF}$	1.5
SSTL2 I & II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	$V_{REF}$	1.25
CTT	$V_{REF} - 0.2$	$V_{REF} + 0.2$	$V_{REF}$	1.5
AGP	$V_{REF} - (0.2 \times V_{CCO})$	$V_{REF} + (0.2 \times V_{CCO})$	$V_{REF}$	Per AGP Spec

### Notes:

1. Input waveform switches between  $V_L$  and  $V_H$ .
2. Measurements are made at  $V_{REF}$  (Typ), Maximum, and Minimum. Worst-case values are reported.
3. I/O parameter measurements are made with the capacitance values shown in [Table 2](#). See Application Note XAPP133 on [www.xilinx.com](http://www.xilinx.com) for appropriate terminations.
4. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

### CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Combinatorial Delays						
4-input function: F/G inputs to X/Y outputs	T <sub>ILO</sub>	0.29	0.6	0.7	0.8	ns, max
5-input function: F/G inputs to F5 output	T <sub>IF5</sub>	0.32	0.7	0.8	0.9	ns, max
5-input function: F/G inputs to X output	T <sub>IF5X</sub>	0.36	0.8	0.8	1.0	ns, max
6-input function: F/G inputs to Y output via F6 MUX	T <sub>IF6Y</sub>	0.44	0.9	1.0	1.2	ns, max
6-input function: F5IN input to Y output	T <sub>F5INY</sub>	0.17	0.32	0.36	0.42	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T <sub>IFNCTL</sub>	0.31	0.7	0.7	0.8	ns, max
BY input to YB output	T <sub>BYYB</sub>	0.27	0.53	0.6	0.7	ns, max
Sequential Delays						
FF Clock CLK to XQ/YQ outputs	T <sub>CKO</sub>	0.54	1.1	1.2	1.4	ns, max
Latch Clock CLK to XQ/YQ outputs	T <sub>CKLO</sub>	0.6	1.2	1.4	1.6	ns, max
Setup and Hold Times before/after Clock CLK <sup>(1)</sup>	Setup Time / Hold Time					
4-input function: F/G Inputs	T <sub>ICK</sub> /T <sub>CKI</sub>	0.6 / 0	1.2 / 0	1.4 / 0	1.5 / 0	ns, min
5-input function: F/G inputs	T <sub>IF5CK</sub> /T <sub>CKIF5</sub>	0.7 / 0	1.3 / 0	1.5 / 0	1.7 / 0	ns, min
6-input function: F5IN input	T <sub>F5INCK</sub> /T <sub>CKF5IN</sub>	0.46 / 0	1.0 / 0	1.1 / 0	1.2 / 0	ns, min
6-input function: F/G inputs via F6 MUX	T <sub>IF6CK</sub> /T <sub>CKIF6</sub>	0.8 / 0	1.5 / 0	1.7 / 0	1.9 / 0	ns, min
BX/BY inputs	T <sub>DICK</sub> /T <sub>CKDI</sub>	0.30 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
CE input	T <sub>CECK</sub> /T <sub>CKCE</sub>	0.37 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
SR/BY inputs (synchronous)	T <sub>RCK</sub> T <sub>CKR</sub>	0.33 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T <sub>CH</sub>	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low	T <sub>CL</sub>	0.8	1.5	1.7	2.0	ns, min
Set/Reset						
Minimum Pulse Width, SR/BY inputs	T <sub>RPW</sub>	1.3	2.5	2.8	3.3	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T <sub>RQ</sub>	0.54	1.1	1.3	1.4	ns, max
Delay from GSR to XQ/YQ outputs	T <sub>IOGSRQ</sub>	4.9	9.7	10.9	12.5	ns, max
Toggle Frequency (MHz) (for export control)	F <sub>TOG</sub> (MHz)	625	333	294	250	MHz

#### Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Date	Version	Revision
01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
03/00	2.0	New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration.
05/00	2.1	Modified "Pins not listed..." statement. Speed grade update to Final status.
05/00	2.2	Modified Table 18.
09/00	2.3	<ul style="list-style-type: none"> <li>Added XCV400 values to table under <b>Minimum Clock-to-Out for Virtex Devices</b>.</li> <li>Corrected Units column in table under <b>IOB Input Switching Characteristics</b>.</li> <li>Added values to table under <b>CLB SelectRAM Switching Characteristics</b>.</li> </ul>
10/00	2.4	<ul style="list-style-type: none"> <li>Corrected Pinout information for devices in the BG256, BG432, and BG560 packages in Table 18.</li> <li>Corrected <b>BG256 Pin Function Diagram</b>.</li> </ul>
04/02/01	2.5	<ul style="list-style-type: none"> <li>Revised minimums for <b>Global Clock Set-Up and Hold for LVTTTL Standard, with DLL</b>.</li> <li>Converted file to modularized format. See the <b>Virtex Data Sheet</b> section.</li> </ul>
04/19/01	2.6	<ul style="list-style-type: none"> <li>Clarified TIOCKP and TIOCKON <b>IOB Output Switching Characteristics</b> descriptors.</li> </ul>
07/19/01	2.7	<ul style="list-style-type: none"> <li>Under <b>Absolute Maximum Ratings</b>, changed (T<sub>SOL</sub>) to 220 °C.</li> </ul>
07/26/01	2.8	<ul style="list-style-type: none"> <li>Removed T<sub>SOL</sub> parameter and added footnote to <b>Absolute Maximum Ratings</b> table.</li> </ul>
10/29/01	2.9	<ul style="list-style-type: none"> <li>Updated the speed grade designations used in data sheets, and added <b>Table 1</b>, which shows the current speed grade designation for each device.</li> </ul>
02/01/02	3.0	<ul style="list-style-type: none"> <li>Added footnote to <b>DC Input and Output Levels</b> table.</li> </ul>
07/19/02	3.1	<ul style="list-style-type: none"> <li>Removed mention of MIL-M-38510/605 specification.</li> <li>Added link to xapp158 from the <b>Power-On Power Supply Requirements</b> section.</li> </ul>
09/10/02	3.2	<ul style="list-style-type: none"> <li>Added Clock CLK to <b>IOB Input Switching Characteristics</b> and <b>IOB Output Switching Characteristics</b>.</li> </ul>
03/01/13	4.0	The products listed in this data sheet are obsolete. See <a href="#">XCN10016</a> for further information.

## Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

- DS003-1, Virtex 2.5V FPGAs:  
Introduction and Ordering Information (Module 1)
- DS003-2, Virtex 2.5V FPGAs:  
Functional Description (Module 2)
- DS003-3, Virtex 2.5V FPGAs:  
DC and Switching Characteristics (Module 3)
- DS003-4, Virtex 2.5V FPGAs:  
Pinout Tables (Module 4)

Table 2: Virtex Pinout Tables (Chip-Scale and QFP Packages) (Continued)

Pin Name	Device	CS144	TQ144	PQ/HQ240
<b>V<sub>REF</sub> Bank 3</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	H11, K12	60, 68	130, 144
	XCV100/150	... + J10	... + 66	... + 133
	XCV200/300	N/A	N/A	... + 126
	XCV400	N/A	N/A	... + 147
	XCV600	N/A	N/A	... + 132
	XCV800	N/A	N/A	... + 140
<b>V<sub>REF</sub> Bank 4</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	L8, L10	79, 87	97, 111
	XCV100/150	... + N10	... + 81	... + 108
	XCV200/300	N/A	N/A	... + 115
	XCV400	N/A	N/A	... + 94
	XCV600	N/A	N/A	... + 109
	XCV800	N/A	N/A	... + 101
<b>V<sub>REF</sub> Bank 5</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	L4, L6	96, 104	70, 84
	XCV100/150	... + N4	... + 102	... + 73
	XCV200/300	N/A	N/A	... + 66
	XCV400	N/A	N/A	... + 87
	XCV600	N/A	N/A	... + 72
	XCV800	N/A	N/A	... + 80

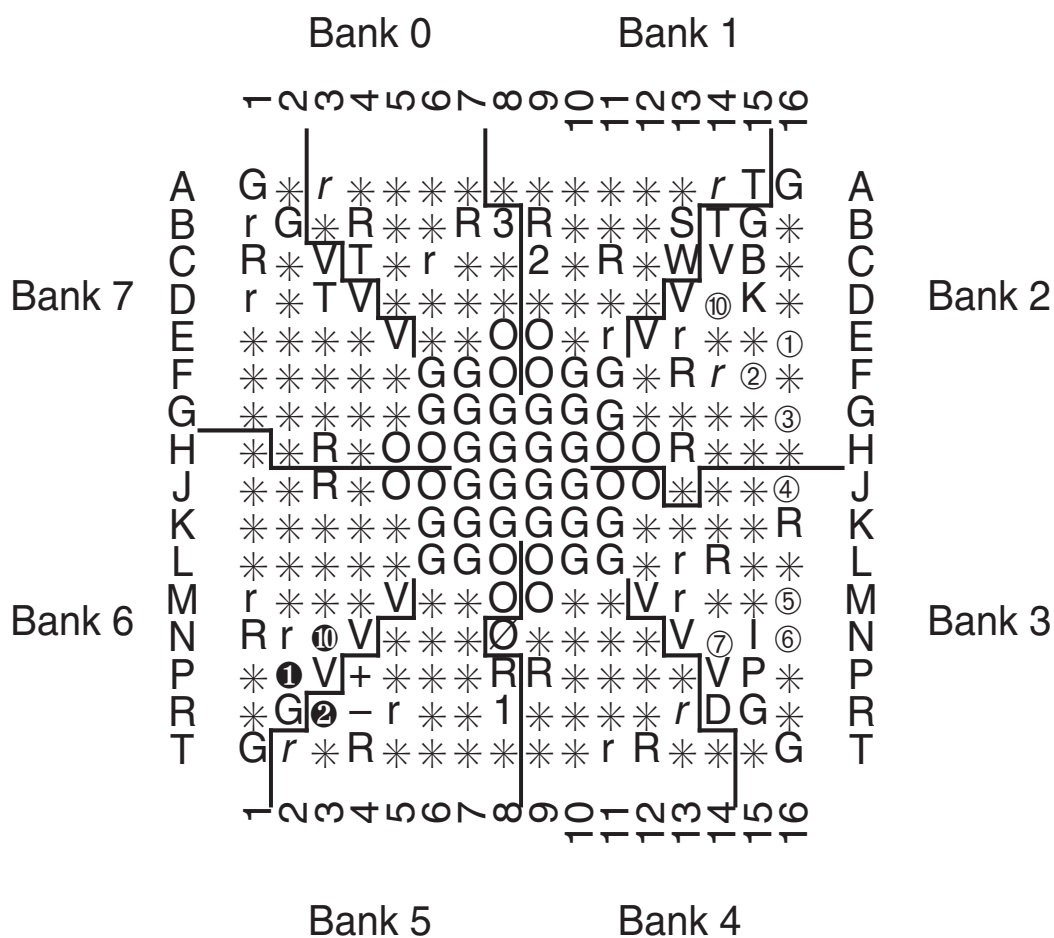
Table 4: Virtex Pinout Tables (Fine-Pitch BGA)

Pin Name	Device	FG256	FG456	FG676	FG680
GCK0	All	N8	W12	AA14	AW19
GCK1	All	R8	Y11	AB13	AU22
GCK2	All	C9	A11	C13	D21
GCK3	All	B8	C11	E13	A20
M0	All	N3	AB2	AD4	AT37
M1	All	P2	U5	W7	AU38
M2	All	R3	Y4	AB6	AT35
CCLK	All	D15	B22	D24	E4
PROGRAM	All	P15	W20	AA22	AT5
DONE	All	R14	Y19	AB21	AU5
INIT	All	N15	V19	Y21	AU2
BUSY/DOUT	All	C15	C21	E23	E3
D0/DIN	All	D14	D20	F22	C2
D1	All	E16	H22	K24	P4
D2	All	F15	H20	K22	P3
D3	All	G16	K20	M22	R1
D4	All	J16	N22	R24	AD3
D5	All	M16	R21	U23	AG2
D6	All	N16	T22	V24	AH1
D7	All	N14	Y21	AB23	AR4
WRITE	All	C13	A20	C22	B4
CS	All	B13	C19	E21	D5
TDI	All	A15	B20	D22	B3
TDO	All	B14	A21	C23	C4
TMS	All	D3	D3	F5	E36
TCK	All	C4	C4	E6	C36
DXN	All	R4	Y5	AB7	AV37
DXP	All	P4	V6	Y8	AU35

Table 4: Virtex Pinout Tables (Fine-Pitch BGA) (Continued)

Pin Name	Device	FG256	FG456	FG676	FG680
<b>V<sub>REF</sub> Bank 1</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	B9, C11	N/A	N/A	N/A
	XCV100/150	... + E11	A18, B13, E14	N/A	N/A
	XCV200/300	... + A14	... + A19	N/A	N/A
	XCV400	N/A	N/A	A14, C20, C21, D15, G16	N/A
	XCV600	N/A	N/A	... + B19	B6, B8, B18, D11, D13, D17
	XCV800	N/A	N/A	... + A17	... + B14
	XCV1000	N/A	N/A	N/A	... + B5
<b>V<sub>REF</sub> Bank 2</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	F13, H13	N/A	N/A	N/A
	XCV100/150	... + F14	F21, H18, K21	N/A	N/A
	XCV200/300	... + E13	... + D22	N/A	N/A
	XCV400	N/A	N/A	F24, H23, K20, M23, M26	N/A
	XCV600	N/A	N/A	... + G26	G1, H4, J1, L2, V5, W3
	XCV800	N/A	N/A	... + K25	... + N1
	XCV1000	N/A	N/A	N/A	... + D2
<b>V<sub>REF</sub> Bank 3</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	K16, L14	N/A	N/A	N/A
	XCV100/150	... + L13	N21, R19, U21	N/A	N/A
	XCV200/300	... + M13	... + U20	N/A	N/A
	XCV400	N/A	N/A	R23, R25, U21, W22, W23	N/A
	XCV600	N/A	N/A	... + W26	AC1, AJ2, AK3, AL4, AR1, Y1
	XCV800	N/A	N/A	... + U25	... + AF3
	XCV1000	N/A	N/A	N/A	... + AP4

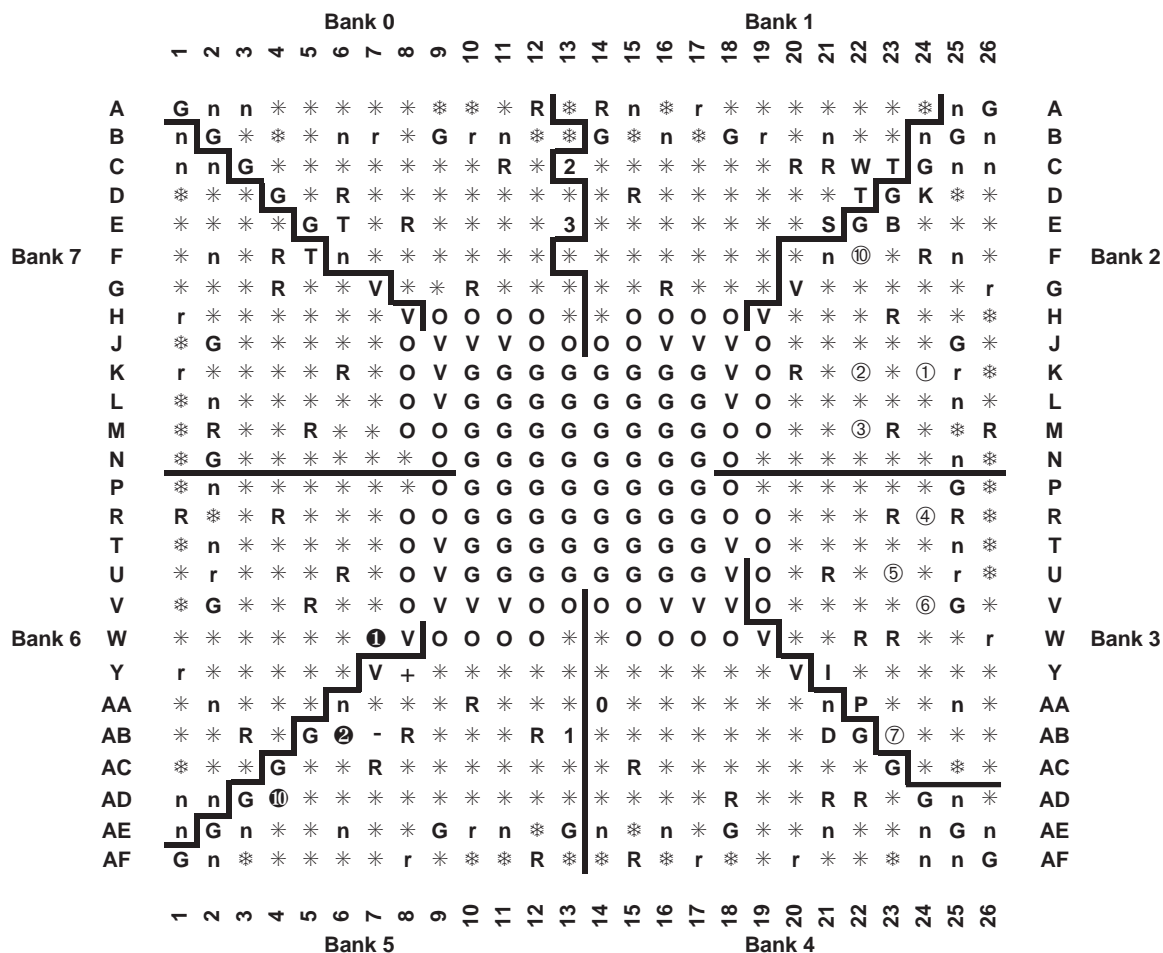
## FG256 Pin Function Diagram



## FG256 (Top view)

Figure 8: FG256 Pin Function Diagram

## FG676 Pin Function Diagram



**FG676**  
(Top view)

fg676a

Figure 10: FG676 Pin Function Diagram

**Notes:**

Packages FG456 and FG676 are layout compatible.