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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	384
Number of Logic Elements/Cells	1728
Total RAM Bits	32768
Number of I/O	166
Number of Gates	57906
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv50-5pq240c

Virtex Architecture

Virtex devices feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing resources. The abundance of routing resources permits the Virtex family to accommodate even the largest and most complex designs.

Virtex FPGAs are SRAM-based, and are customized by loading configuration data into internal memory cells. In some modes, the FPGA reads its own configuration data from an external PROM (master serial mode). Otherwise, the configuration data is written into the FPGA (SelectMAP™, slave serial, and JTAG modes).

The standard Xilinx Foundation™ and Alliance Series™ Development systems deliver complete design support for Virtex, covering every aspect from behavioral and schematic entry, through simulation, automatic design translation and implementation, to the creation, downloading, and readback of a configuration bit stream.

Higher Performance

Virtex devices provide better performance than previous generations of FPGA. Designs can achieve synchronous system clock rates up to 200 MHz including I/O. Virtex inputs and outputs comply fully with PCI specifications, and interfaces can be implemented that operate at 33 MHz or 66 MHz. Additionally, Virtex supports the hot-swapping requirements of Compact PCI.

Xilinx thoroughly benchmarked the Virtex family. While performance is design-dependent, many designs operated internally at speeds in excess of 100 MHz and can achieve 200 MHz. Table 2 shows performance data for representative circuits, using worst-case timing parameters.

Table 2: Performance for Common Circuit Functions

Function	Bits	Virtex -6
Register-to-Register		
Adder	16	5.0 ns
	64	7.2 ns
Pipelined Multiplier	8 x 8	5.1 ns
	16 x 16	6.0 ns
Address Decoder	16	4.4 ns
	64	6.4 ns
16:1 Multiplexer		5.4 ns
Parity Tree	9	4.1 ns
	18	5.0 ns
	36	6.9 ns
Chip-to-Chip		
HSTL Class IV		200 MHz
LVTTTL, 16mA, fast slew		180 MHz

Virtex Device/Package Combinations and Maximum I/O

Table 3: Virtex Family Maximum User I/O by Device/Package (Excluding Dedicated Clock Pins)

Package	XCV50	XCV100	XCV150	XCV200	XCV300	XCV400	XCV600	XCV800	XCV1000
CS144	94	94							
TQ144	98	98							
PQ240	166	166	166	166	166				
HQ240						166	166	166	
BG256	180	180	180	180					
BG352			260	260	260				
BG432					316	316	316	316	
BG560						404	404	404	404
FG256	176	176	176	176					
FG456			260	284	312				
FG676						404	444	444	
FG680							512	512	512

Virtex Ordering Information

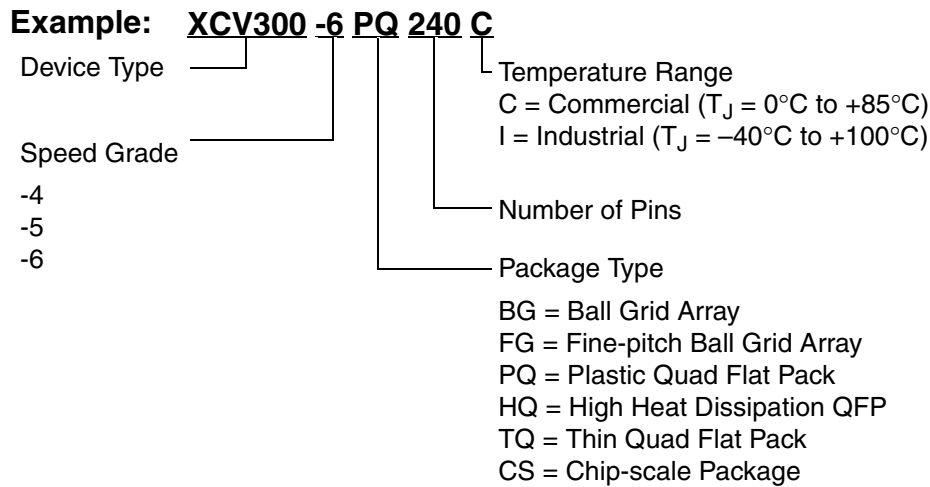
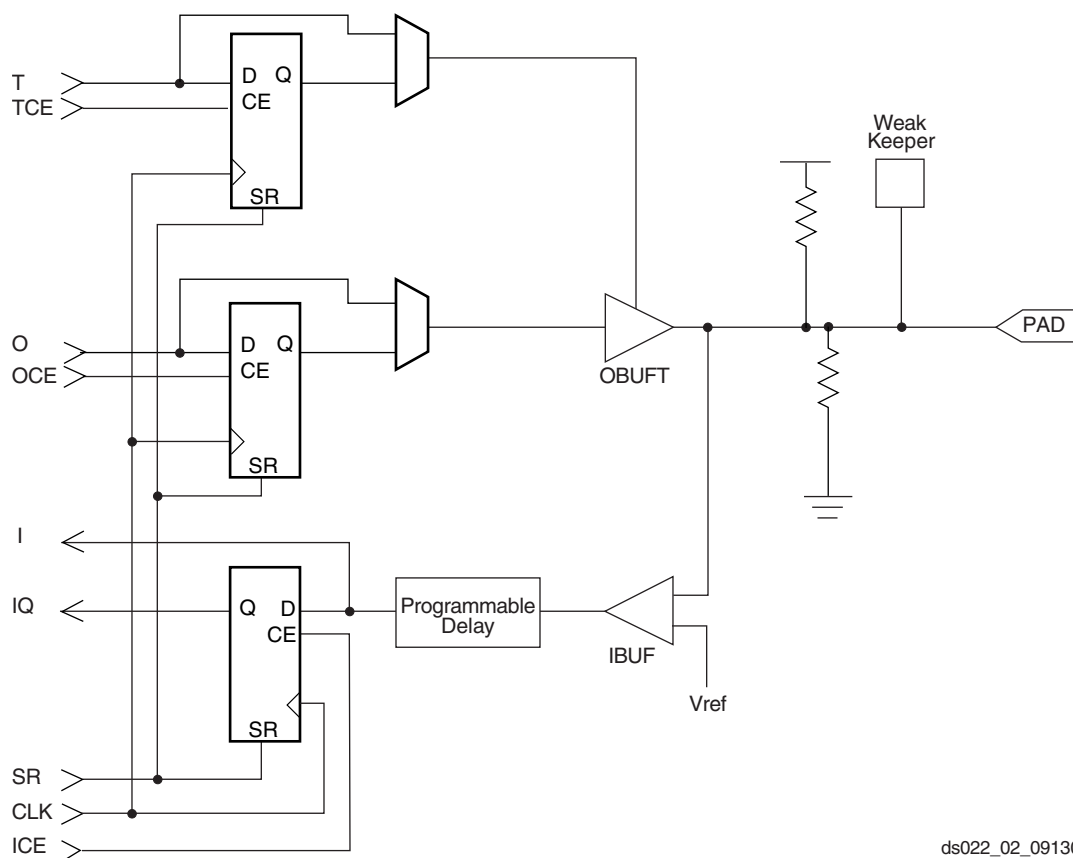


Figure 1: Virtex Ordering Information



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Figure 2: Virtex Input/Output Block (IOB)

Table 1: Supported Select I/O Standards

I/O Standard	Input Reference Voltage (V_{REF})	Output Source Voltage (V_{CCO})	Board Termination Voltage (V_{TT})	5 V Tolerant
LVTTL 2 – 24 mA	N/A	3.3	N/A	Yes
LVC MOS2	N/A	2.5	N/A	Yes
PCI, 5 V	N/A	3.3	N/A	Yes
PCI, 3.3 V	N/A	3.3	N/A	No
GTL	0.8	N/A	1.2	No
GTL+	1.0	N/A	1.5	No
HSTL Class I	0.75	1.5	0.75	No
HSTL Class III	0.9	1.5	1.5	No
HSTL Class IV	0.9	1.5	1.5	No
SSTL3 Class I & II	1.5	3.3	1.5	No
SSTL2 Class I & II	1.25	2.5	1.25	No
CTT	1.5	3.3	1.5	No
AGP	1.32	3.3	N/A	No

more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary. All the V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage, and not used for I/O.

In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or can be connected to the V_{CCO} voltage to permit migration to a larger device if necessary.

In TQ144 and PQ/HQ240 packages, all V_{CCO} pins are bonded together internally, and consequently the same V_{CCO} voltage must be connected to all of them. In the CS144 package, bank pairs that share a side are interconnected internally, permitting four choices for V_{CCO} . In both cases, the V_{REF} pins remain internally connected as eight banks, and can be used as described previously.

Configurable Logic Block

The basic building block of the Virtex CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and a storage element. The output from the function generator in each LC drives both the CLB output and the D input of the flip-flop. Each Virtex CLB contains four LCs, organized in two similar slices, as shown in Figure 4.

Figure 5 shows a more detailed view of a single slice.

In addition to the four basic LCs, the Virtex CLB contains logic that combines function generators to provide functions

of five or six inputs. Consequently, when estimating the number of system gates provided by a given device, each CLB counts as 4.5 LCs.

Look-Up Tables

Virtex function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16x1-bit dual-port synchronous RAM.

The Virtex LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

Storage Elements

The storage elements in the Virtex slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by the function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each Slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals can be configured to operate asynchronously. All of the control signals are independently invertible, and are shared by the two flip-flops within the slice.

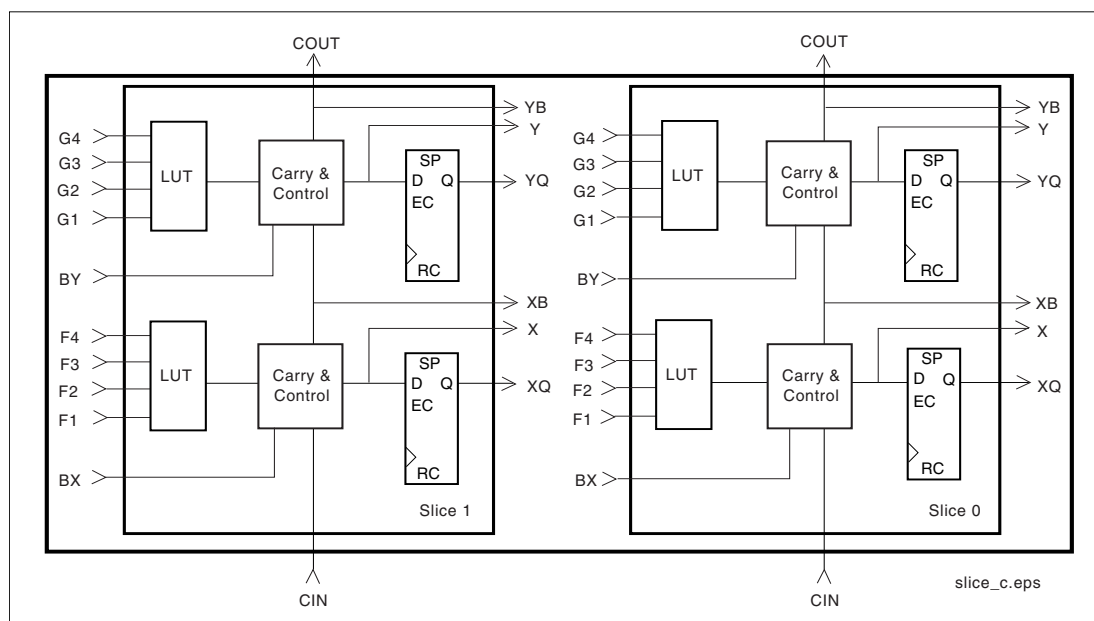


Figure 4: 2-Slice Virtex CLB

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is

selected either from these pads or from signals in the general purpose routing.

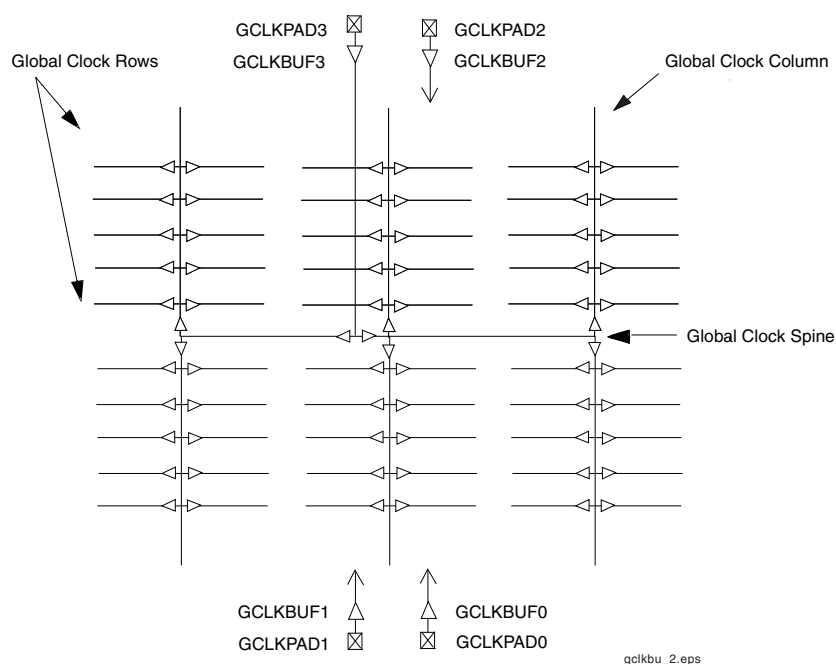


Figure 9: Global Clock Distribution Network

Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Clock edges reach internal flip-flops one to four clock periods after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to de-skew a board level clock among multiple Virtex devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

See **DLL Timing Parameters**, page 21 of Module 3, for frequency range information.

Boundary Scan

Virtex devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, and HIGHZ instructions. The TAP also supports two internal scan chains and configuration/readback of the device. The TAP uses dedicated package pins that always operate using LVTTTL. For TDO to operate using LVTTTL, the V_{CCO} for Bank 2 should be 3.3 V. Otherwise, TDO switches rail-to-rail between ground and V_{CCO} .

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including un-bonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections, provided the user design or application is turned off.

Table 5 lists the boundary-scan instructions supported in Virtex FPGAs. Internal signals can be captured during EXTEST by connecting them to un-bonded or unused IOBs. They can also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Before the device is configured, all instructions except USER1 and USER2 are available. After configuration, all instructions are available. During configuration, it is recommended that those operations using the boundary-scan register (SAMPLE/PRELOAD, INTEST, EXTEST) not be performed.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

Figure 10 is a diagram of the Virtex Series boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Instruction Set

The Virtex Series boundary scan instruction set also includes instructions to configure the device and read back configuration data (CFG_IN, CFG_OUT, and JSTART). The complete instruction set is coded as shown in **Table 5**.

Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out, and 3-State Control. Non-IOB pins have appropriate partial bit population if input-only or output-only. Each EXTEST CAPTURED-OR state captures all In, Out, and 3-state pins.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA supports up to two additional internal scan chains that can be specified using the BSCAN macro. The macro provides two user pins (SEL1 and SEL2) which are decoded of the USER1 and USER2 instructions respectively. For these instructions, two corresponding pins (TDO1 and TDO2) allow user scan data to be shifted out of TDO.

Likewise, there are individual clock pins (DRCK1 and DRCK2) for each user register. There is a common input pin (TDI) and shared output pins that represent the state of the TAP controller (RESET, SHIFT, and UPDATE).

Bit Sequence

The order within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contribute all three bits.

From a cavity-up view of the chip (as shown in EPIC), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in **Figure 11**.

BSDL (Boundary Scan Description Language) files for Virtex Series devices are available on the Xilinx web site in the File Download area.

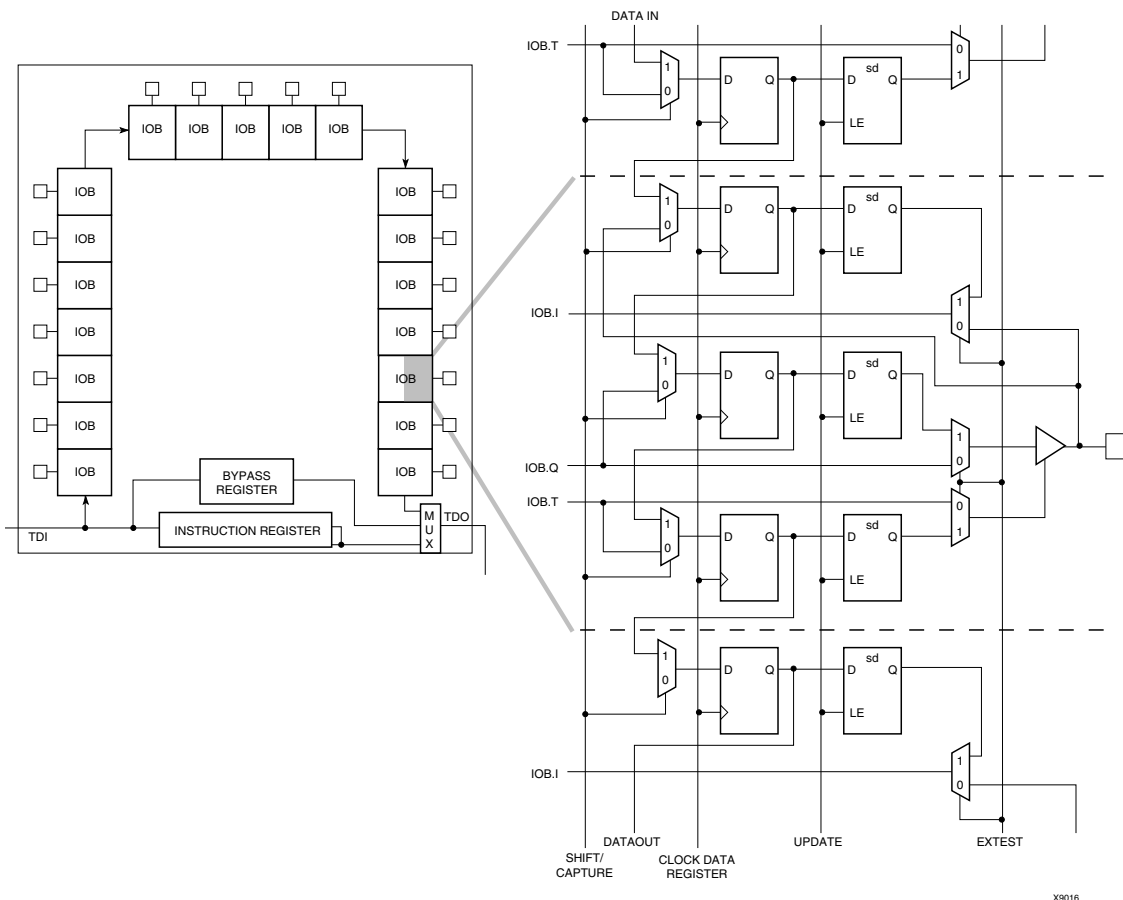


Figure 10: Virtex Series Boundary Scan Logic

Date	Version	Revision
01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
03/00	2.0	New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration.
05/00	2.1	Modified “Pins not listed...” statement. Speed grade update to Final status.
05/00	2.2	Modified Table 18.
09/00	2.3	<ul style="list-style-type: none"> Added XCV400 values to table under Minimum Clock-to-Out for Virtex Devices. Corrected Units column in table under IOB Input Switching Characteristics. Added values to table under CLB SelectRAM Switching Characteristics.
10/00	2.4	<ul style="list-style-type: none"> Corrected Pinout information for devices in the BG256, BG432, and BG560 packages in Table 18. Corrected BG256 Pin Function Diagram.
04/01	2.5	<ul style="list-style-type: none"> Revised minimums for Global Clock Set-Up and Hold for LVTTTL Standard, with DLL. Updated SelectMAP Write Timing Characteristics values in Table 9. Converted file to modularized format. See the Virtex Data Sheet section.
07/19/01	2.6	<ul style="list-style-type: none"> Made minor edits to text under Configuration.
07/19/02	2.7	<ul style="list-style-type: none"> Made minor edit to Figure 16 and Figure 18.
09/10/02	2.8	<ul style="list-style-type: none"> Added clarifications in the Configuration, Boundary-Scan Mode, and Block SelectRAM sections. Revised Figure 17.
12/09/02	2.8.1	<ul style="list-style-type: none"> Added clarification in the Boundary Scan section. Corrected number of buffered Hex lines listed in General Purpose Routing section.
03/01/13	4.0	The products listed in this data sheet are obsolete. See XCN10016 for further information.

Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

- DS003-1, Virtex 2.5V FPGAs:
Introduction and Ordering Information (Module 1)
- DS003-2, Virtex 2.5V FPGAs:
Functional Description (Module 2)
- DS003-3, Virtex 2.5V FPGAs:
DC and Switching Characteristics (Module 3)
- DS003-4, Virtex 2.5V FPGAs:
Pinout Tables (Module 4)

IOB Input Switching Characteristics Standard Adjustments

Description	Symbol	Standard ⁽¹⁾	Speed Grade				Units
			Min	-6	-5	-4	
Data Input Delay Adjustments							
Standard-specific data input delay adjustments	T _{ILVTTL}	LVTTL	0	0	0	0	ns
	T _{ILVCMOS2}	LVC MOS2	−0.02	−0.04	−0.04	−0.05	ns
	T _{I PCI33_3}	PCI, 33 MHz, 3.3 V	−0.05	−0.11	−0.12	−0.14	ns
	T _{I PCI33_5}	PCI, 33 MHz, 5.0 V	0.13	0.25	0.28	0.33	ns
	T _{I PCI66_3}	PCI, 66 MHz, 3.3 V	−0.05	−0.11	−0.12	−0.14	ns
	T _{IGTL}	GTL	0.10	0.20	0.23	0.26	ns
	T _{IGTLP}	GTL+	0.06	0.11	0.12	0.14	ns
	T _{IHSTL}	HSTL	0.02	0.03	0.03	0.04	ns
	T _{ISSTL2}	SSTL2	−0.04	−0.08	−0.09	−0.10	ns
	T _{ISSTL3}	SSTL3	−0.02	−0.04	−0.05	−0.06	ns
	T _{ICTT}	CTT	0.01	0.02	0.02	0.02	ns
	T _{IAGP}	AGP	−0.03	−0.06	−0.07	−0.08	ns

Notes:

- Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see [Table 3](#).

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in [IOB Output Switching Characteristics Standard Adjustments, page 9](#).

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Propagation Delays						
O input to Pad	T _{IOOP}	1.2	2.9	3.2	3.5	ns, max
O input to Pad via transparent latch	T _{IOOLP}	1.4	3.4	3.7	4.0	ns, max
3-State Delays						
T input to Pad high-impedance ⁽¹⁾	T _{IOTHZ}	1.0	2.0	2.2	2.4	ns, max
T input to valid data on Pad	T _{IOTON}	1.4	3.1	3.3	3.7	ns, max
T input to Pad high-impedance via transparent latch ⁽¹⁾	T _{IOTLPHZ}	1.2	2.4	2.6	3.0	ns, max
T input to valid data on Pad via transparent latch	T _{IOTLPON}	1.6	3.5	3.8	4.2	ns, max
GTS to Pad high impedance ⁽¹⁾	T _{GTS}	2.5	4.9	5.5	6.3	ns, max
Sequential Delays						
Clock CLK						
Minimum Pulse Width, High	T _{CH}	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low	T _{CL}	0.8	1.5	1.7	2.0	ns, min

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Clock CLK to Pad delay with OBUFT enabled (non-3-state)	T_{IOCKP}	1.0	2.9	3.2	3.5	ns, max
Clock CLK to Pad high-impedance (synchronous) ⁽¹⁾	T_{IOCKHZ}	1.1	2.3	2.5	2.9	ns, max
Clock CLK to valid data on Pad delay, plus enable delay for OBUFT	T_{IOCKON}	1.5	3.4	3.7	4.1	ns, max
Setup and Hold Times before/after Clock CLK⁽²⁾		Setup Time / Hold Time				
O input	T_{IOOCK}/T_{IOCKO}	0.51 / 0	1.1 / 0	1.2 / 0	1.3 / 0	ns, min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$	0.37 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
SR input (OFF)	$T_{IOSRCKO}/T_{IOCKOSR}$	0.52 / 0	1.1 / 0	1.2 / 0	1.4 / 0	ns, min
3-State Setup Times, T input	T_{IOTCK}/T_{IOCKT}	0.34 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$	0.41 / 0	0.9 / 0	0.9 / 0	1.1 / 0	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$	0.49 / 0	1.0 / 0	1.1 / 0	1.3 / 0	ns, min
Set/Reset Delays						
SR input to Pad (asynchronous)	T_{IOSRP}	1.6	3.8	4.1	4.6	ns, max
SR input to Pad high-impedance (asynchronous) ⁽¹⁾	T_{IOSRHZ}	1.6	3.1	3.4	3.9	ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}	2.0	4.2	4.6	5.1	ns, max
GSR to Pad	T_{IOGSRQ}	4.9	9.7	10.9	12.5	ns, max

Notes:

1. 3-state turn-off delays should not be adjusted.
2. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

I/O Standard Global Clock Input Adjustments

Description	Symbol	Standard ⁽¹⁾	Speed Grade				Units
			Min	-6	-5	-4	
Data Input Delay Adjustments							
Standard-specific global clock input delay adjustments	T _{GPLVTTL}	LVTTL	0	0	0	0	ns, max
	T _{GPLVCMOS2}	LVC MOS2	−0.02	−0.04	−0.04	−0.05	ns, max
	T _{GP PCI33_3}	PCI, 33 MHz, 3.3 V	−0.05	−0.11	−0.12	−0.14	ns, max
	T _{GP PCI33_5}	PCI, 33 MHz, 5.0 V	0.13	0.25	0.28	0.33	ns, max
	T _{GP PCI66_3}	PCI, 66 MHz, 3.3 V	−0.05	−0.11	−0.12	−0.14	ns, max
	T _{GPGTL}	GTL	0.7	0.8	0.9	0.9	ns, max
	T _{GPGTLP}	GTL+	0.7	0.8	0.8	0.8	ns, max
	T _{GPHSTL}	HSTL	0.7	0.7	0.7	0.7	ns, max
	T _{GPSSTL2}	SSTL2	0.6	0.52	0.51	0.50	ns, max
	T _{GPSSTL3}	SSTL3	0.6	0.6	0.55	0.54	ns, max
	T _{GPCTT}	CTT	0.7	0.7	0.7	0.7	ns, max
	T _{GPAGP}	AGP	0.6	0.54	0.53	0.52	ns, max

Notes:

1. Input timing for GPLVTTL is measured at 1.4 V. For other I/O standards, see [Table 3](#).

CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Combinatorial Delays						
F operand inputs to X via XOR	T _{OPX}	0.37	0.8	0.9	1.0	ns, max
F operand input to XB output	T _{OPXB}	0.54	1.1	1.3	1.4	ns, max
F operand input to Y via XOR	T _{OPY}	0.8	1.5	1.7	2.0	ns, max
F operand input to YB output	T _{OPYB}	0.8	1.5	1.7	2.0	ns, max
F operand input to COUT output	T _{OPCYF}	0.6	1.2	1.3	1.5	ns, max
G operand inputs to Y via XOR	T _{OPGY}	0.46	1.0	1.1	1.2	ns, max
G operand input to YB output	T _{OPGYB}	0.8	1.6	1.8	2.1	ns, max
G operand input to COUT output	T _{OPCYG}	0.7	1.3	1.4	1.6	ns, max
BX initialization input to COUT	T _{BXCY}	0.41	0.9	1.0	1.1	ns, max
CIN input to X output via XOR	T _{CINX}	0.21	0.41	0.46	0.53	ns, max
CIN input to XB	T _{CINXB}	0.02	0.04	0.05	0.06	ns, max
CIN input to Y via XOR	T _{CINY}	0.23	0.46	0.52	0.6	ns, max
CIN input to YB	T _{CINYB}	0.23	0.45	0.51	0.6	ns, max
CIN input to COUT output	T _{BYP}	0.05	0.09	0.10	0.11	ns, max
Multiplier Operation						
F1/2 operand inputs to XB output via AND	T _{FANDXB}	0.18	0.36	0.40	0.46	ns, max
F1/2 operand inputs to YB output via AND	T _{FANDYB}	0.40	0.8	0.9	1.1	ns, max
F1/2 operand inputs to COUT output via AND	T _{FANDCY}	0.22	0.43	0.48	0.6	ns, max
G1/2 operand inputs to YB output via AND	T _{GANDYB}	0.25	0.50	0.6	0.7	ns, max
G1/2 operand inputs to COUT output via AND	T _{GANDCY}	0.07	0.13	0.15	0.17	ns, max
Setup and Hold Times before/after Clock CLK ⁽¹⁾	Setup Time / Hold Time					
CIN input to FFX	T _{CCKX} /T _{CKCX}	0.50 / 0	1.0 / 0	1.2 / 0	1.3 / 0	ns, min
CIN input to FFY	T _{CCKY} /T _{CKCY}	0.53 / 0	1.1 / 0	1.2 / 0	1.4 / 0	ns, min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

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01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
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05/00	2.2	Modified Table 18.
09/00	2.3	<ul style="list-style-type: none"> Added XCV400 values to table under Minimum Clock-to-Out for Virtex Devices. Corrected Units column in table under IOB Input Switching Characteristics. Added values to table under CLB SelectRAM Switching Characteristics.
10/00	2.4	<ul style="list-style-type: none"> Corrected Pinout information for devices in the BG256, BG432, and BG560 packages in Table 18. Corrected BG256 Pin Function Diagram.
04/02/01	2.5	<ul style="list-style-type: none"> Revised minimums for Global Clock Set-Up and Hold for LVTTTL Standard, with DLL. Converted file to modularized format. See the Virtex Data Sheet section.
04/19/01	2.6	<ul style="list-style-type: none"> Clarified TIOCKP and TIOCKON IOB Output Switching Characteristics descriptors.
07/19/01	2.7	<ul style="list-style-type: none"> Under Absolute Maximum Ratings, changed (T_{SOL}) to 220 °C.
07/26/01	2.8	<ul style="list-style-type: none"> Removed T_{SOL} parameter and added footnote to Absolute Maximum Ratings table.
10/29/01	2.9	<ul style="list-style-type: none"> Updated the speed grade designations used in data sheets, and added Table 1, which shows the current speed grade designation for each device.
02/01/02	3.0	<ul style="list-style-type: none"> Added footnote to DC Input and Output Levels table.
07/19/02	3.1	<ul style="list-style-type: none"> Removed mention of MIL-M-38510/605 specification. Added link to xapp158 from the Power-On Power Supply Requirements section.
09/10/02	3.2	<ul style="list-style-type: none"> Added Clock CLK to IOB Input Switching Characteristics and IOB Output Switching Characteristics.
03/01/13	4.0	The products listed in this data sheet are obsolete. See XCN10016 for further information.

Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

- DS003-1, Virtex 2.5V FPGAs:
Introduction and Ordering Information (Module 1)
- DS003-2, Virtex 2.5V FPGAs:
Functional Description (Module 2)
- DS003-3, Virtex 2.5V FPGAs:
DC and Switching Characteristics (Module 3)
- DS003-4, Virtex 2.5V FPGAs:
Pinout Tables (Module 4)



Virtex™ 2.5 V Field Programmable Gate Arrays

DS003-4 (v4.0) March 1, 2013

Production Product Specification

Virtex Pin Definitions

Table 1: Special Purpose Pins

Pin Name	Dedicated Pin	Direction	Description
GCK0, GCK1, GCK2, GCK3	Yes	Input	Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin: it is an input for SelectMAP and slave-serial modes, and output in master-serial mode. After configuration, it is input only, logic level = Don't Care.
PROGRAM	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output can be open drain.
INIT	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. The pin becomes a user I/O after configuration.
BUSY/ DOUT	No	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration unless the SelectMAP port is retained. In bit-serial modes, DOUT provides header information to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In SelectMAP mode, D0 - D7 are configuration data pins. These pins become user I/Os after configuration unless the SelectMAP port is retained. In bit-serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
WRITE	No	Input	In SelectMAP mode, the active-low Write Enable signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
CS	No	Input	In SelectMAP mode, the active-low Chip Select signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary-scan Test-Access-Port pins, as defined in IEEE 1149.1.
DXN, DXP	Yes	N/A	Temperature-sensing diode pins. (Anode: DXP, cathode: DXN)
V _{CCINT}	Yes	Input	Power-supply pins for the internal core logic.
V _{CCO}	Yes	Input	Power-supply pins for the output drivers (subject to banking rules)
V _{REF}	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground

Table 2: Virtex Pinout Tables (Chip-Scale and QFP Packages) (Continued)

Pin Name	Device	CS144	TQ144	PQ/HQ240
V_{REF} Bank 6 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	H2, K1	116, 123	36, 50
	XCV100/150	... + J3	... + 118	... + 47
	XCV200/300	N/A	N/A	... + 54
	XCV400	N/A	N/A	... + 33
	XCV600	N/A	N/A	... + 48
	XCV800	N/A	N/A	... + 40
V_{REF} Bank 7 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	D4, E1	133, 140	9, 23
	XCV100/150	... + D2	... + 138	... + 12
	XCV200/300	N/A	N/A	... + 5
	XCV400	N/A	N/A	... + 26
	XCV600	N/A	N/A	... + 11
	XCV800	N/A	N/A	... + 19
GND	All	A1, B9, B11, C7, D5, E4, E11, F1, G10, J1, J12, L3, L5, L7, L9, N12	9, 18, 26, 35, 46, 54, 64, 75, 83, 91, 100, 111, 120, 129, 136, 144,	1, 8, 14, 22, 29, 37, 45, 51, 59, 69, 75, 83, 91, 98, 106, 112, 119, 129, 135, 143, 151, 158, 166, 172, 182, 190, 196, 204, 211, 219, 227, 233

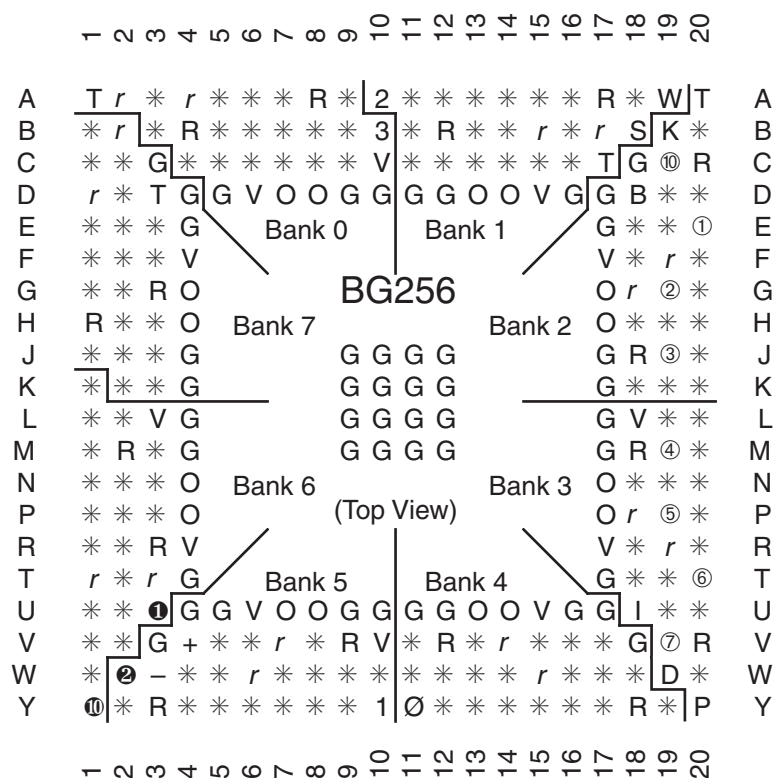
Table 3: Virtex Pinout Tables (BGA) (Continued)

Pin Name	Device	BG256	BG352	BG432	BG560
V_{REF} Bank 3 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	M18, V20	N/A	N/A	N/A
	XCV100/150	... + R19	R4, V4, Y3	N/A	N/A
	XCV200/300	... + P18	... + AC2	V2, AB4, AD4, AF3	N/A
	XCV400	N/A	N/A	... + U2	V4, W5, AD3, AE5, AK2
	XCV600	N/A	N/A	... + AC3	... + AF1
	XCV800	N/A	N/A	... + Y3	... + AA4
	XCV1000	N/A	N/A	N/A	... + AH4
V_{REF} Bank 4 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	V12, Y18	N/A	N/A	N/A
	XCV100/150	... + W15	AC12, AE5, AE8,	N/A	N/A
	XCV200/300	... + V14	... + AE4	AJ7, AL4, AL8, AL13	N/A
	XCV400	N/A	N/A	... + AK15	AL7, AL10, AL16, AM4, AM14
	XCV600	N/A	N/A	... + AK8	... + AL9
	XCV800	N/A	N/A	... + AJ12	... + AK13
	XCV1000	N/A	N/A	N/A	... + AN3
V_{REF} Bank 5 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	V9, Y3	N/A	N/A	N/A
	XCV100/150	... + W6	AC15, AC18, AD20	N/A	N/A
	XCV200/300	... + V7	... + AE23	AJ18, AJ25, AK23, AK27	N/A
	XCV400	N/A	N/A	... + AJ17	AJ18, AJ25, AL20, AL24, AL29
	XCV600	N/A	N/A	... + AL24	... + AM26
	XCV800	N/A	N/A	... + AH19	... + AN23
	XCV1000	N/A	N/A	N/A	... + AK28
V_{REF} Bank 6 (V _{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V _{REF} pins are general I/O.	XCV50	M2, R3	N/A	N/A	N/A
	XCV100/150	... + T1	R24, Y26, AA25,	N/A	N/A
	XCV200/300	... + T3	... + AD26	V28, AB28, AE30, AF28	N/A
	XCV400	N/A	N/A	... + U28	V29, Y32, AD31, AE29, AK32
	XCV600	N/A	N/A	... + AC28	... + AE31
	XCV800	N/A	N/A	... + Y30	... + AA30
	XCV1000	N/A	N/A	N/A	... + AH30

Table 4: Virtex Pinout Tables (Fine-Pitch BGA) (Continued)

Pin Name	Device	FG256	FG456	FG676	FG680
No Connect (No-connect pins are listed incrementally. All pins listed for both the required device and all larger devices listed in the same package are no connects.)	XCV800	N/A	N/A	A2, A3, A15, A25, B1, B6, B11, B16, B21, B24, B26, C1, C2, C25, C26, F2, F6, F21, F25, L2, L25, N25, P2, T2, T25, AA2, AA6, AA21, AA25, AD1, AD2, AD25, AE1, AE3, AE6, AE11, AE14, AE16, AE21, AE24, AE26, AF2, AF24, AF25	N/A
	XCV600	N/A	N/A	same as above	N/A
	XCV400	N/A	N/A	... + A9, A10, A13, A16, A24, AC1, AC25, AE12, AE15, AF3, AF10, AF11, AF13, AF14, AF16, AF18, AF23, B4, B12, B13, B15, B17, D1, D25, H26, J1, K26, L1, M1, M25, N1, N26, P1, P26, R2, R26, T1, T26, U26, V1	N/A
	XCV300	N/A	D4, D19, W4, W19	N/A	N/A
	XCV200	N/A	... + A2, A6, A12, B11, B16, C2, D1, D18, E17, E19, G2, G22, L2, L19, M2, M21, R3, R20, U3, U18, Y22, AA1, AA3, AA11, AA16, AB7, AB12, AB21,	N/A	N/A
	XCV150	N/A	... + A13, A14, C8, C9, E13, F11, H21, J1, J4, K2, K18, K19, M17, N1, P1, P5, P22, R22, W13, W15, AA9, AA10, AB8, AB14	N/A	N/A

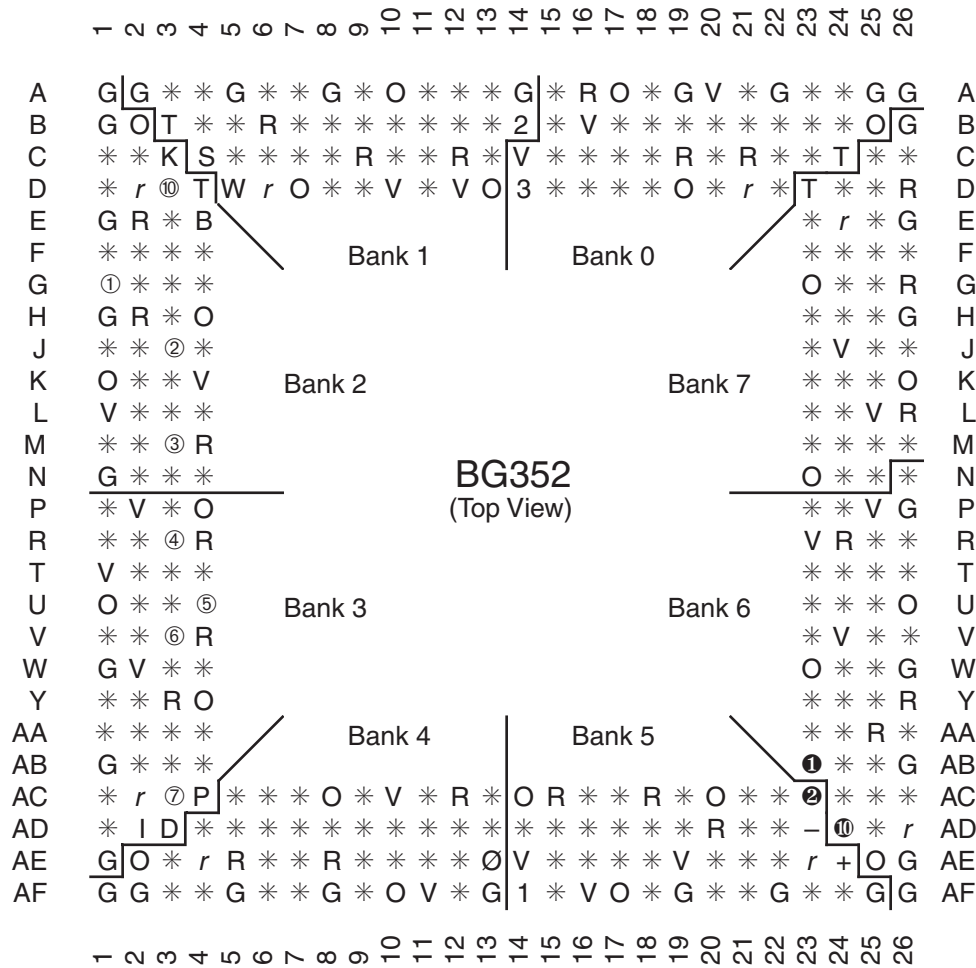
BG256 Pin Function Diagram



DS003_18_100300

Figure 4: BG256 Pin Function Diagram

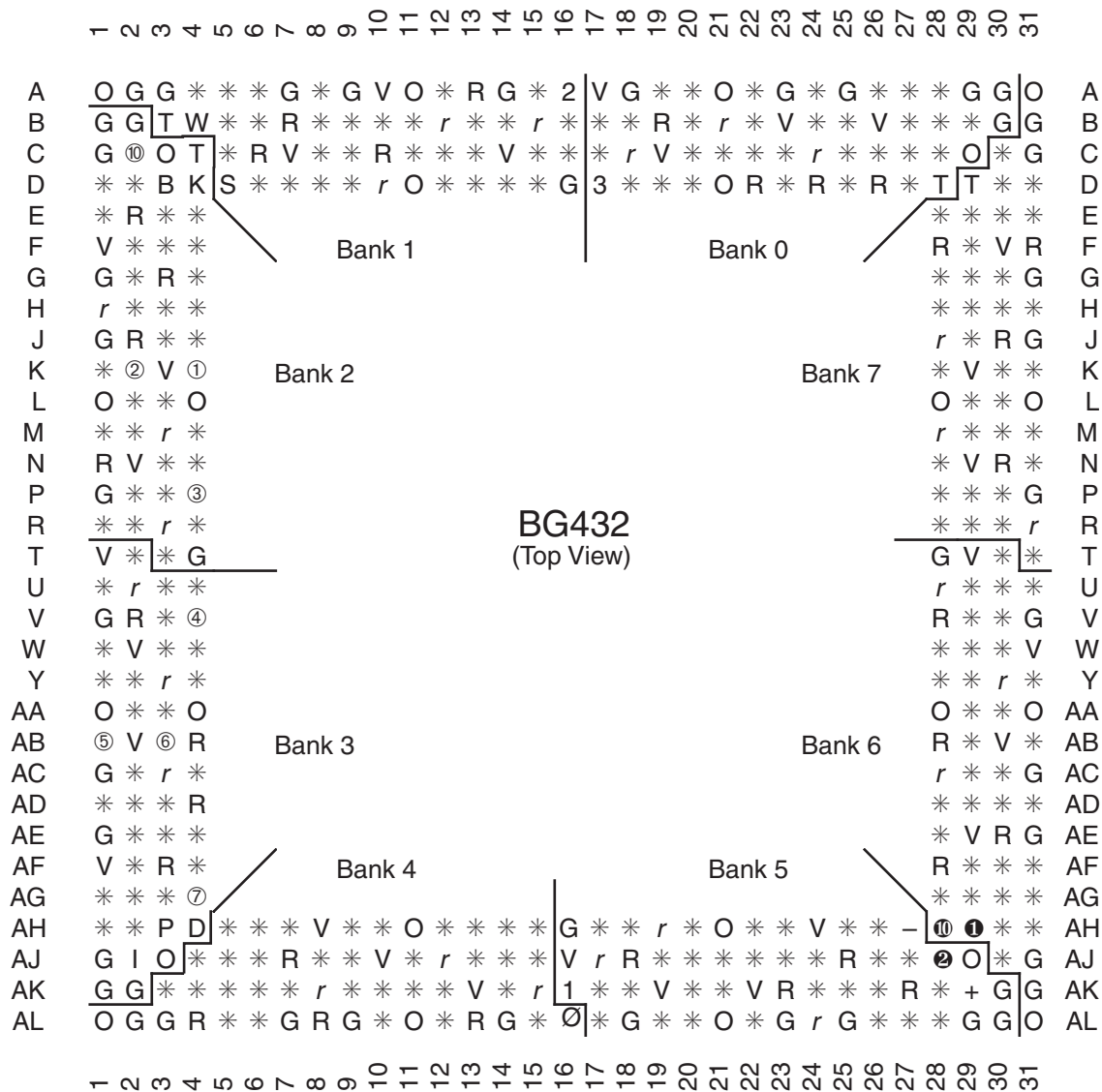
BG352 Pin Function Diagram



DS003_19_100600

Figure 5: BG352 Pin Function Diagram

BG432 Pin Function Diagram



DS003_21_100300

Figure 6: BG432 Pin Function Diagram