# AMD Xilinx - XCV800-4BG432C Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 4704 |
| Number of Logic Elements/Cells | 21168 |
| Total RAM Bits | 114688 |
| Number of I/O | 316 |
| Number of Gates | 888439 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 432-LBGA Exposed Pad, Metal |
| Supplier Device Package | 432-MBGA (40x40) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xcv800-4bg432c |

Email: info@E-XFL.COM
Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

### *Master-Serial Mode*

In master-serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM that feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge.

The interface is identical to slave-serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration. Switching to a lower frequency is prohibited.

The CCLK frequency is set using the ConfigRate option in the bitstream generation software. The maximum CCLK frequency that can be selected is 60 MHz. When selecting a CCLK frequency, ensure that the serial PROM and any daisy-chained FPGAs are fast enough to support the clock rate.

On power-up, the CCLK frequency is 2.5 MHz. This frequency is used until the ConfigRate bits have been loaded when the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz.

Figure 12 shows a full master/slave system. In this system, the left-most device operates in master-serial mode. The remaining devices operate in slave-serial mode. The SPROM RESET pin is driven by INIT, and the CE input is driven by DONE. There is the potential for contention on the DONE pin, depending on the start-up sequence options chosen.

Figure 14 shows the timing of master-serial configuration. Master-serial mode is selected by a <000> or <100> on the mode pins (M2, M1, M0). Table 8 shows the timing information for Figure 14.

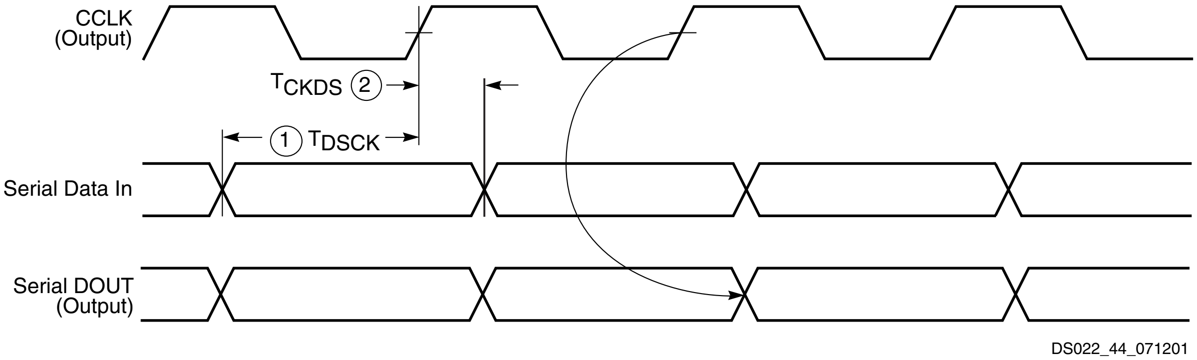


*Figure 14:* **Master-Serial Mode Programming Switching Characteristics**

At power-up, $V_{CC}$ must rise from 1.0 V to $V_{CC}$ min in less than 50 ms, otherwise delay configuration by pulling PROGRAM Low until $V_{CC}$ is valid.

The sequence of operations necessary to configure a Virtex FPGA serially appears in Figure 15.

### *SelectMAP Mode*

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the FPGA with a BUSY flag controlling the flow of data.

An external data source provides a byte stream, CCLK, a Chip Select (CS) signal and a Write signal (WRITE). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

Data can also be read using the SelectMAP mode. If WRITE is not asserted, configuration data is read out of the FPGA as part of a readback operation.

In the SelectMAP mode, multiple Virtex devices can be chained in parallel. DATA pins (D7:D0), CCLK, WRITE, BUSY, PROGRAM, DONE, and INIT can be connected in parallel between all the FPGAs. Note that the data is organized with the MSB of each byte on pin DO and the LSB of each byte on D7. The CS pins are kept separate, insuring that each FPGA can be selected individually. WRITE should be Low before loading the first bitstream and returned High after the last device has been programmed. Use CS to select the appropriate FPGA for loading the bitstream and sending the configuration data. at the end of the bitstream, deselect the loaded device and select the next target FPGA by setting its CS pin High. A free-running oscillator or other externally generated signal can be used for CCLK. The BUSY signal can be ignored for frequencies below 50 MHz. For details about frequencies above 50 MHz, see XAPP138, Virtex Configuration and Readback. Once all the devices have been programmed, the DONE pin goes High.

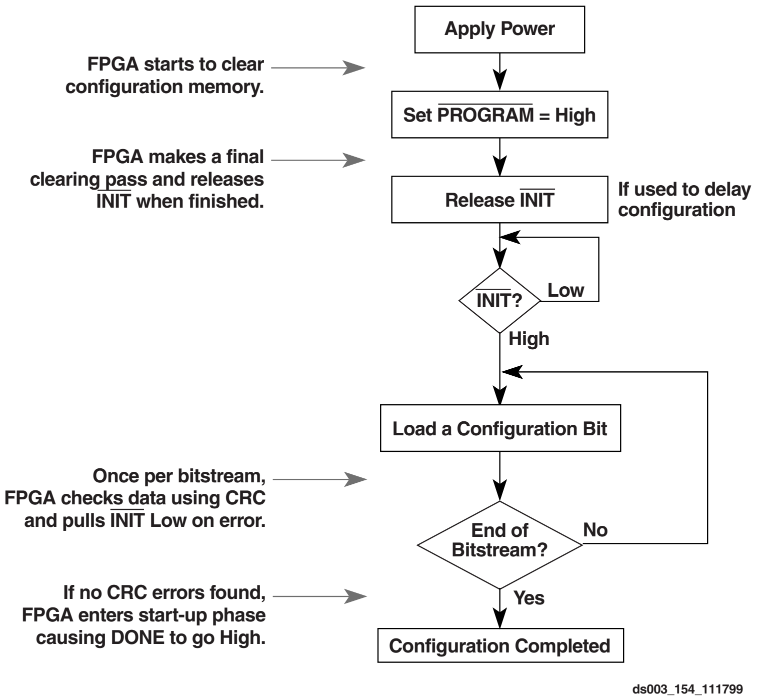


*Figure 15:* **Serial Configuration Flowchart**

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained to permit high-speed 8-bit readback.

Retention of the SelectMAP port is selectable on a design-by-design basis when the bitstream is generated. If retention is selected, PROHIBIT constraints are required to prevent the SelectMAP-port pins from being used as user I/O.

Multiple Virtex FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, $\overline{\text{WRITE}}$, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the $\overline{\text{CS}}$ pin of each device in turn and writing the appropriate data. see Table 9 for SelectMAP Write Timing Characteristics.

*Table 9:* **SelectMAP Write Timing Characteristics**

| | Description | | Symbol | | Units |
|---|---|---|---|---|---|
| CCLK | $D_{0\text{-}7}$ Setup/Hold | 1/2 | $T_{SMDCC}/T_{SMCCD}$ | 5.0 / 1.7 | ns, min |
| | $\overline{\text{CS}}$ Setup/Hold | 3/4 | $T_{SMCSCC}/T_{SMCCCS}$ | 7.0 / 1.7 | ns, min |
| | $\overline{\text{WRITE}}$ Setup/Hold | 5/6 | $T_{SMCCW}/T_{SMWCC}$ | 7.0 / 1.7 | ns, min |
| | BUSY Propagation Delay | 7 | $T_{SMCKBY}$ | 12.0 | ns, max |
| | Maximum Frequency | | $F_{CC}$ | 66 | MHz, max |
| | Maximum Frequency with no handshake | | $F_{CCNH}$ | 50 | MHz, max |

### *Write*

Write operations send packets of configuration data into the FPGA. The sequence of operations for a multi-cycle write operation is shown below. Note that a configuration packet can be split into many such sequences. The packet does not have to complete within one assertion of $\overline{\text{CS}}$, illustrated in Figure 16.

1. Assert $\overline{\text{WRITE}}$ and $\overline{\text{CS}}$ Low. Note that when $\overline{\text{CS}}$ is asserted on successive CCLKs, $\overline{\text{WRITE}}$ must remain either asserted or de-asserted. Otherwise an abort will be initiated, as described below.
2. Drive data onto D[7:0]. Note that to avoid contention, the data source should not be enabled while $\overline{\text{CS}}$ is Low and $\overline{\text{WRITE}}$ is High. Similarly, while $\overline{\text{WRITE}}$ is High, no more that one $\overline{\text{CS}}$ should be asserted.

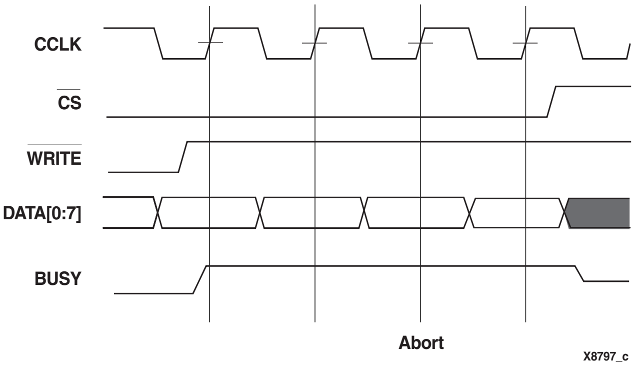


*Figure 18:* **SelectMAP Write Abort Waveforms**

### *Boundary-Scan Mode*

In the boundary-scan mode, configuration is done through the IEEE 1149.1 Test Access Port. Note that the $\overline{\text{PROGRAM}}$ pin must be pulled High prior to reconfiguration. A Low on the $\overline{\text{PROGRAM}}$ pin resets the TAP controller and no JTAG operations can be performed.

Configuration through the TAP uses the CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port (when using TCK as a start-up clock).

1. Load the CFG_IN instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the JSTART instruction into IR
6. Enter the SDR state
7. Clock TCK through the startup sequence
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode is selected by a <101> or 001> on the mode pins (M2, M1, M0). For details on TAP characteristics, refer to XAPP139.

## Configuration Sequence

The configuration of Virtex devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user, as described below. The configuration process can also be initiated by asserting $\overline{\text{PROGRAM}}$. The end of the memory-clearing phase is signalled by $\overline{\text{INIT}}$ going High, and the completion of the entire process is signalled by DONE going High.

The power-up timing of configuration signals is shown in Figure 19. The corresponding timing characteristics are listed in Table 10.

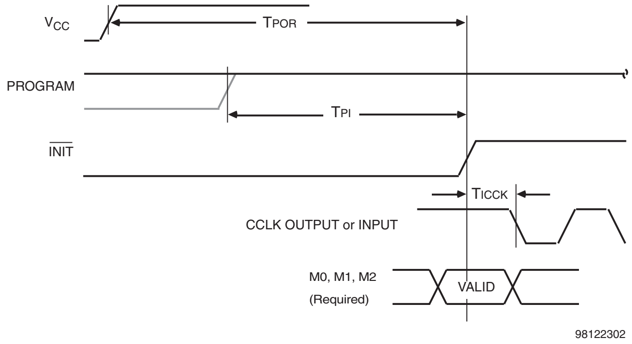


*Figure 19:* **Power-Up Timing Configuration Signals**

*Table 10:* **Power-up Timing Characteristics**

| Description | Symbol | Value | Units |
|---|---|---|---|
| Power-on Reset | $T_{POR}$ | 2.0 | ms, max |
| Program Latency | $T_{PL}$ | 100.0 | µs, max |
| CCLK (output) Delay | $T_{ICCK}$ | 0.5 | µs, min |
| | | 4.0 | µs, max |
| Program Pulse Width | $T_{PROGRAM}$ | 300 | ns, min |

### *Delaying Configuration*

$\overline{\text{INIT}}$ can be held Low using an open-drain driver. An open-drain is required since $\overline{\text{INIT}}$ is a bidirectional open-drain pin that is held Low by the FPGA while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

### *Start-Up Sequence*

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed. In addition, the GTS, GSR, and GWE events can be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start in synchronism. The sequence can also be paused at any stage until lock has been achieved on any or all DLLs.

## DC Characteristics Over Recommended Operating Conditions

| Symbol | Description | Device | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{DRINT}$ | Data Retention $V_{CCINT}$ Voltage<br>(below which configuration data can be lost) | All | 2.0 | | V |
| $V_{DRIO}$ | Data Retention $V_{CCO}$ Voltage<br>(below which configuration data can be lost) | All | 1.2 | | V |
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current$^{(1,3)}$ | XCV50 | | 50 | mA |
| | | XCV100 | | 50 | mA |
| | | XCV150 | | 50 | mA |
| | | XCV200 | | 75 | mA |
| | | XCV300 | | 75 | mA |
| | | XCV400 | | 75 | mA |
| | | XCV600 | | 100 | mA |
| | | XCV800 | | 100 | mA |
| | | XCV1000 | | 100 | mA |
| $I_{CCOQ}$ | Quiescent $V_{CCO}$ supply current$^{(1)}$ | XCV50 | | 2 | mA |
| | | XCV100 | | 2 | mA |
| | | XCV150 | | 2 | mA |
| | | XCV200 | | 2 | mA |
| | | XCV300 | | 2 | mA |
| | | XCV400 | | 2 | mA |
| | | XCV600 | | 2 | mA |
| | | XCV800 | | 2 | mA |
| | | XCV1000 | | 2 | mA |
| $I_{REF}$ | $V_{REF}$ current per $V_{REF}$ pin | All | | 20 | µA |
| $I_L$ | Input or output leakage current | All | –10 | +10 | µA |
| $C_{IN}$ | Input capacitance (sample tested)<br>BGA, PQ, HQ, packages | All | | 8 | pF |
| $I_{RPU}$ | Pad pull-up (when selected) @ $V_{in}$ = 0 V, $V_{CCO}$ = 3.3 V (sample tested) | All | Note (2) | 0.25 | mA |
| $I_{RPD}$ | Pad pull-down (when selected) @ $V_{in}$ = 3.6 V (sample tested) | | Note (2) | 0.15 | mA |

**Notes:**

1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.
3. Multiply $I_{CCINTQ}$ limit by two for industrial grade.

| Description | Device | Symbol | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | -6 | -5 | -4 | |
| **Setup and Hold Times with respect to Clock CLK at IOB input register(1)** | | | **Setup Time / Hold Time** | | | | |
| Pad, no delay | All | $T_{IOPICK}/T_{IOICKP}$ | 0.8 / 0 | 1.6 / 0 | 1.8 / 0 | 2.0 / 0 | ns, min |
| Pad, with delay | XCV50 | $T_{IOPICKD}/T_{IOICKPD}$ | 1.9 / 0 | 3.7 / 0 | 4.1 / 0 | 4.7 / 0 | ns, min |
| | XCV100 | | 1.9 / 0 | 3.7 / 0 | 4.1 / 0 | 4.7 / 0 | ns, min |
| | XCV150 | | 1.9 / 0 | 3.8 / 0 | 4.3 / 0 | 4.9 / 0 | ns, min |
| | XCV200 | | 2.0 / 0 | 3.9 / 0 | 4.4 / 0 | 5.0 / 0 | ns, min |
| | XCV300 | | 2.0 / 0 | 3.9 / 0 | 4.4 / 0 | 5.0 / 0 | ns, min |
| | XCV400 | | 2.1 / 0 | 4.1 / 0 | 4.6 / 0 | 5.3 / 0 | ns, min |
| | XCV600 | | 2.1 / 0 | 4.2 / 0 | 4.7 / 0 | 5.4 / 0 | ns, min |
| | XCV800 | | 2.2 / 0 | 4.4 / 0 | 4.9 / 0 | 5.6 / 0 | ns, min |
| | XCV1000 | | 2.3 / 0 | 4.5 / 0 | 5.0 / 0 | 5.8 / 0 | ns, min |
| ICE input | All | $T_{IOICECK}/T_{IOCKICE}$ | 0.37/ 0 | 0.8 / 0 | 0.9 / 0 | 1.0 / 0 | ns, max |
| **Set/Reset Delays** | | | | | | | |
| SR input (IFF, synchronous) | All | $T_{IOSRCKI}$ | 0.49 | 1.0 | 1.1 | 1.3 | ns, max |
| SR input to IQ (asynchronous) | All | $T_{IOSRIQ}$ | 0.70 | 1.4 | 1.6 | 1.8 | ns, max |
| GSR to output IQ | All | $T_{GSRQ}$ | 4.9 | 9.7 | 10.9 | 12.5 | ns, max |

**Notes:**

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see Table 3.

## Calculation of $T_{ioop}$ as a Function of Capacitance

$T_{ioop}$ is the propagation delay from the O Input of the IOB to the pad. The values for $T_{ioop}$ were based on the standard capacitive load (Csl) for each I/O standard as listed in Table 2.

*Table 2:* **Constants for Calculating $T_{ioop}$**

| Standard | Csl (pF) | fl (ns/pF) |
|---|---|---|
| LVTTL Fast Slew Rate, 2mA drive | 35 | 0.41 |
| LVTTL Fast Slew Rate, 4mA drive | 35 | 0.20 |
| LVTTL Fast Slew Rate, 6mA drive | 35 | 0.13 |
| LVTTL Fast Slew Rate, 8mA drive | 35 | 0.079 |
| LVTTL Fast Slew Rate, 12mA drive | 35 | 0.044 |
| LVTTL Fast Slew Rate, 16mA drive | 35 | 0.043 |
| LVTTL Fast Slew Rate, 24mA drive | 35 | 0.033 |
| LVTTL Slow Slew Rate, 2mA drive | 35 | 0.41 |
| LVTTL Slow Slew Rate, 4mA drive | 35 | 0.20 |
| LVTTL Slow Slew Rate, 6mA drive | 35 | 0.100 |
| LVTTL Slow Slew Rate, 8mA drive | 35 | 0.086 |
| LVTTL Slow Slew Rate, 12mA drive | 35 | 0.058 |
| LVTTL Slow Slew Rate, 16mA drive | 35 | 0.050 |
| LVTTL Slow Slew Rate, 24mA drive | 35 | 0.048 |
| LVCMOS2 | 35 | 0.041 |
| PCI 33MHz 5V | 50 | 0.050 |
| PCI 33MHZ 3.3 V | 10 | 0.050 |
| PCI 66 MHz 3.3 V | 10 | 0.033 |
| GTL | 0 | 0.014 |
| GTL+ | 0 | 0.017 |
| HSTL Class I | 20 | 0.022 |
| HSTL Class III | 20 | 0.016 |
| HSTL Class IV | 20 | 0.014 |
| SSTL2 Class I | 30 | 0.028 |
| SSTL2 Class II | 30 | 0.016 |
| SSTL3 Class I | 30 | 0.029 |
| SSTL3 Class II | 30 | 0.016 |
| CTT | 20 | 0.035 |
| AGP | 10 | 0.037 |

**Notes:**

1. I/O parameter measurements are made with the capacitance values shown above. See Application Note XAPP133 on www.xilinx.com for appropriate terminations.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

For other capacitive loads, use the formulas below to calculate the corresponding $T_{ioop}$.

$$T_{ioop} = T_{ioop} + T_{opadjust} + (C_{load} - C_{sl}) * fl$$

Where:

$T_{opadjust}$ is reported above in the Output Delay Adjustment section.

$C_{load}$ is the capacitive load for the design.

*Table 3:* **Delay Measurement Methodology**

| Standard | $V_L$(1) | $V_H$(1) | Meas. Point | $V_{REF}$ Typ(2) |
|---|---|---|---|---|
| LVTTL | 0 | 3 | 1.4 | - |
| LVCMOS2 | 0 | 2.5 | 1.125 | - |
| PCI33_5 | Per PCI Spec | | | - |
| PCI33_3 | Per PCI Spec | | | - |
| PCI66_3 | Per PCI Spec | | | - |
| GTL | $V_{REF} -0.2$ | $V_{REF} +0.2$ | $V_{REF}$ | 0.80 |
| GTL+ | $V_{REF} -0.2$ | $V_{REF} +0.2$ | $V_{REF}$ | 1.0 |
| HSTL Class I | $V_{REF} -0.5$ | $V_{REF} +0.5$ | $V_{REF}$ | 0.75 |
| HSTL Class III | $V_{REF} -0.5$ | $V_{REF} +0.5$ | $V_{REF}$ | 0.90 |
| HSTL Class IV | $V_{REF} -0.5$ | $V_{REF} +0.5$ | $V_{REF}$ | 0.90 |
| SSTL3 I & II | $V_{REF} -1.0$ | $V_{REF} +1.0$ | $V_{REF}$ | 1.5 |
| SSTL2 I & II | $V_{REF} -0.75$ | $V_{REF} +0.75$ | $V_{REF}$ | 1.25 |
| CTT | $V_{REF} -0.2$ | $V_{REF} +0.2$ | $V_{REF}$ | 1.5 |
| AGP | $V_{REF} -$ $(0.2xV_{CCO})$ | $V_{REF} +$ $(0.2xV_{CCO})$ | $V_{REF}$ | Per AGP Spec |

**Notes:**

1. Input waveform switches between $V_L$ and $V_H$.
2. Measurements are made at VREF (Typ), Maximum, and Minimum. Worst-case values are reported.
3. I/O parameter measurements are made with the capacitance values shown in Table 2. See Application Note XAPP133 on www.xilinx.com for appropriate terminations.
4. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

## CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

| Description | Symbol | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | Min | -6 | -5 | -4 | |
| Combinatorial Delays | | | | | | |
| F operand inputs to X via XOR | $T_{OPX}$ | 0.37 | 0.8 | 0.9 | 1.0 | ns, max |
| F operand input to XB output | $T_{OPXB}$ | 0.54 | 1.1 | 1.3 | 1.4 | ns, max |
| F operand input to Y via XOR | $T_{OPY}$ | 0.8 | 1.5 | 1.7 | 2.0 | ns, max |
| F operand input to YB output | $T_{OPYB}$ | 0.8 | 1.5 | 1.7 | 2.0 | ns, max |
| F operand input to COUT output | $T_{OPCYF}$ | 0.6 | 1.2 | 1.3 | 1.5 | ns, max |
| G operand inputs to Y via XOR | $T_{OPGY}$ | 0.46 | 1.0 | 1.1 | 1.2 | ns, max |
| G operand input to YB output | $T_{OPGYB}$ | 0.8 | 1.6 | 1.8 | 2.1 | ns, max |
| G operand input to COUT output | $T_{OPCYG}$ | 0.7 | 1.3 | 1.4 | 1.6 | ns, max |
| BX initialization input to COUT | $T_{BXCY}$ | 0.41 | 0.9 | 1.0 | 1.1 | ns, max |
| CIN input to X output via XOR | $T_{CINX}$ | 0.21 | 0.41 | 0.46 | 0.53 | ns, max |
| CIN input to XB | $T_{CINXB}$ | 0.02 | 0.04 | 0.05 | 0.06 | ns, max |
| CIN input to Y via XOR | $T_{CINY}$ | 0.23 | 0.46 | 0.52 | 0.6 | ns, max |
| CIN input to YB | $T_{CINYB}$ | 0.23 | 0.45 | 0.51 | 0.6 | ns, max |
| CIN input to COUT output | $T_{BYP}$ | 0.05 | 0.09 | 0.10 | 0.11 | ns, max |
| Multiplier Operation | | | | | | |
| F1/2 operand inputs to XB output via AND | $T_{FANDXB}$ | 0.18 | 0.36 | 0.40 | 0.46 | ns, max |
| F1/2 operand inputs to YB output via AND | $T_{FANDYB}$ | 0.40 | 0.8 | 0.9 | 1.1 | ns, max |
| F1/2 operand inputs to COUT output via AND | $T_{FANDCY}$ | 0.22 | 0.43 | 0.48 | 0.6 | ns, max |
| G1/2 operand inputs to YB output via AND | $T_{GANDYB}$ | 0.25 | 0.50 | 0.6 | 0.7 | ns, max |
| G1/2 operand inputs to COUT output via AND | $T_{GANDCY}$ | 0.07 | 0.13 | 0.15 | 0.17 | ns, max |
| Setup and Hold Times before/after Clock CLK(1) | Setup Time / Hold Time | | | | | |
| CIN input to FFX | $T_{CCKX}/T_{CKCX}$ | 0.50 / 0 | 1.0 / 0 | 1.2 / 0 | 1.3 / 0 | ns, min |
| CIN input to FFY | $T_{CCKY}/T_{CKCY}$ | 0.53 / 0 | 1.1 / 0 | 1.2 / 0 | 1.4 / 0 | ns, min |

**Notes:**

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

## Block RAM Switching Characteristics

| Description | Symbol | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | Min | -6 | -5 | -4 | |
| Sequential Delays | | | | | | |
| Clock CLK to DOUT output | $T_{BCKO}$ | 1.7 | 3.4 | 3.8 | 4.3 | ns, max |
| Setup and Hold Times before/after Clock CLK(1) | Setup Time / Hold Time | | | | | |
| ADDR inputs | $T_{BACK}/T_{BCKA}$ | 0.6 / 0 | 1.2 / 0 | 1.3 / 0 | 1.5 / 0 | ns, min |
| DIN inputs | $T_{BDCK}/T_{BCKD}$ | 0.6 / 0 | 1.2 / 0 | 1.3 / 0 | 1.5 / 0 | ns, min |
| EN input | $T_{BECK}/T_{BCKE}$ | 1.3 / 0 | 2.6 / 0 | 3.0 / 0 | 3.4 / 0 | ns, min |
| RST input | $T_{BRCK}/T_{BCKR}$ | 1.3 / 0 | 2.5 / 0 | 2.7 / 0 | 3.2 / 0 | ns, min |
| WEN input | $T_{BWCK}/T_{BCKW}$ | 1.2 / 0 | 2.3 / 0 | 2.6 / 0 | 3.0 / 0 | ns, min |
| Clock CLK | | | | | | |
| Minimum Pulse Width, High | $T_{BPWH}$ | 0.8 | 1.5 | 1.7 | 2.0 | ns, min |
| Minimum Pulse Width, Low | $T_{BPWL}$ | 0.8 | 1.5 | 1.7 | 2.0 | ns, min |
| CLKA -> CLKB setup time for different ports | $T_{BCCS}$ | | 3.0 | 3.5 | 4.0 | ns, min |

**Notes:**

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

## TBUF Switching Characteristics

| Description | Symbol | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | Min | -6 | -5 | -4 | |
| Combinatorial Delays | | | | | | |
| IN input to OUT output | $T_{IO}$ | 0 | 0 | 0 | 0 | ns, max |
| TRI input to OUT output high-impedance | $T_{OFF}$ | 0.05 | 0.09 | 0.10 | 0.11 | ns, max |
| TRI input to valid data on OUT output | $T_{ON}$ | 0.05 | 0.09 | 0.10 | 0.11 | ns, max |

## JTAG Test Access Port Switching Characteristics

| Description | Symbol | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -6 | -5 | -4 | |
| TMS and TDI Setup times before TCK | $T_{TAPTCK}$ | 4.0 | 4.0 | 4.0 | ns, min |
| TMS and TDI Hold times after TCK | $T_{TCKTAP}$ | 2.0 | 2.0 | 2.0 | ns, min |
| Output delay from clock TCK to output TDO | $T_{TCKTDO}$ | 11.0 | 11.0 | 11.0 | ns, max |
| Maximum TCK clock frequency | $F_{TCK}$ | 33 | 33 | 33 | MHz, max |

# Virtex Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

## Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL

| Description | Symbol | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | -6 | -5 | -4 | |
| LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DLL. For data *output* with different standards, adjust delays with the values shown in Output Delay Adjustments. | $T_{ICKOFDLL}$ | XCV50 | 1.0 | 3.1 | 3.3 | 3.6 | ns, max |
| | | XCV100 | 1.0 | 3.1 | 3.3 | 3.6 | ns, max |
| | | XCV150 | 1.0 | 3.1 | 3.3 | 3.6 | ns, max |
| | | XCV200 | 1.0 | 3.1 | 3.3 | 3.6 | ns, max |
| | | XCV300 | 1.0 | 3.1 | 3.3 | 3.6 | ns, max |
| | | XCV400 | 1.0 | 3.1 | 3.3 | 3.6 | ns, max |
| | | XCV600 | 1.0 | 3.1 | 3.3 | 3.6 | ns, max |
| | | XCV800 | 1.0 | 3.1 | 3.3 | 3.6 | ns, max |
| | | XCV1000 | 1.0 | 3.1 | 3.3 | 3.6 | ns, max |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see Table 2 and Table 3.
3. DLL output jitter is already included in the timing calculation.

## Global Clock Input-to-Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL

| Description | Symbol | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | -6 | -5 | -4 | |
| LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DLL. For data *output* with different standards, adjust delays with the values shown in Input and Output Delay Adjustments. For I/O standards requiring $V_{REF}$, such as GTL, GTL+, SSTL, HSTL, CTT, and AGO, an additional 600 ps must be added. | $T_{ICKOF}$ | XCV50 | 1.5 | 4.6 | 5.1 | 5.7 | ns, max |
| | | XCV100 | 1.5 | 4.6 | 5.1 | 5.7 | ns, max |
| | | XCV150 | 1.5 | 4.7 | 5.2 | 5.8 | ns, max |
| | | XCV200 | 1.5 | 4.7 | 5.2 | 5.8 | ns, max |
| | | XCV300 | 1.5 | 4.7 | 5.2 | 5.9 | ns, max |
| | | XCV400 | 1.5 | 4.8 | 5.3 | 6.0 | ns, max |
| | | XCV600 | 1.6 | 4.9 | 5.4 | 6.0 | ns, max |
| | | XCV800 | 1.6 | 4.9 | 5.5 | 6.2 | ns, max |
| | | XCV1000 | 1.7 | 5.0 | 5.6 | 6.3 | ns, max |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see Table 2 and Table 3.

## Minimum Clock-to-Out for Virtex Devices

| | With DLL | Without DLL | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| I/O Standard | All Devices | V50 | V100 | V150 | V200 | V300 | V400 | V600 | V800 | V1000 | Units |
| *LVTTL_S2 | 5.2 | 6.0 | 6.0 | 6.0 | 6.0 | 6.1 | 6.1 | 6.1 | 6.1 | 6.1 | ns |
| *LVTTL_S4 | 3.5 | 4.3 | 4.3 | 4.3 | 4.3 | 4.4 | 4.4 | 4.4 | 4.4 | 4.4 | ns |
| *LVTTL_S6 | 2.8 | 3.6 | 3.6 | 3.6 | 3.6 | 3.7 | 3.7 | 3.7 | 3.7 | 3.7 | ns |
| *LVTTL_S8 | 2.2 | 3.1 | 3.1 | 3.1 | 3.1 | 3.1 | 3.1 | 3.2 | 3.2 | 3.2 | ns |
| *LVTTL_S12 | 2.0 | 2.9 | 2.9 | 2.9 | 2.9 | 2.9 | 2.9 | 3.0 | 3.0 | 3.0 | ns |
| *LVTTL_S16 | 1.9 | 2.8 | 2.8 | 2.8 | 2.8 | 2.8 | 2.8 | 2.9 | 2.9 | 2.9 | ns |
| *LVTTL_S24 | 1.8 | 2.6 | 2.6 | 2.7 | 2.7 | 2.7 | 2.7 | 2.7 | 2.7 | 2.8 | ns |
| *LVTTL_F2 | 2.9 | 3.8 | 3.8 | 3.8 | 3.8 | 3.8 | 3.8 | 3.9 | 3.9 | 3.9 | ns |
| *LVTTL_F4 | 1.7 | 2.6 | 2.6 | 2.6 | 2.6 | 2.6 | 2.6 | 2.7 | 2.7 | 2.7 | ns |
| *LVTTL_F6 | 1.2 | 2.0 | 2.0 | 2.0 | 2.1 | 2.1 | 2.1 | 2.1 | 2.1 | 2.2 | ns |
| *LVTTL_F8 | 1.1 | 1.9 | 1.9 | 1.9 | 1.9 | 2.0 | 2.0 | 2.0 | 2.0 | 2.0 | ns |
| *LVTTL_F12 | 1.0 | 1.8 | 1.8 | 1.8 | 1.8 | 1.9 | 1.9 | 1.9 | 1.9 | 1.9 | ns |
| *LVTTL_F16 | 0.9 | 1.7 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1.9 | 1.9 | ns |
| *LVTTL_F24 | 0.9 | 1.7 | 1.7 | 1.7 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1.9 | ns |
| LVCMOS2 | 1.1 | 1.9 | 1.9 | 1.9 | 2.0 | 2.0 | 2.0 | 2.0 | 2.0 | 2.1 | ns |
| PCI33_3 | 1.5 | 2.4 | 2.4 | 2.4 | 2.4 | 2.4 | 2.4 | 2.5 | 2.5 | 2.5 | ns |
| PCI33_5 | 1.4 | 2.2 | 2.2 | 2.3 | 2.3 | 2.3 | 2.3 | 2.3 | 2.3 | 2.4 | ns |
| PCI66_3 | 1.1 | 1.9 | 1.9 | 2.0 | 2.0 | 2.0 | 2.0 | 2.0 | 2.1 | 2.1 | ns |
| GTL | 1.6 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 2.6 | 2.6 | 2.6 | ns |
| GTL+ | 1.7 | 2.5 | 2.5 | 2.6 | 2.6 | 2.6 | 2.6 | 2.6 | 2.6 | 2.7 | ns |
| HSTL I | 1.1 | 1.9 | 1.9 | 1.9 | 1.9 | 2.0 | 2.0 | 2.0 | 2.0 | 2.0 | ns |
| HSTL III | 0.9 | 1.7 | 1.7 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1.9 | ns |
| HSTL IV | 0.8 | 1.6 | 1.6 | 1.6 | 1.7 | 1.7 | 1.7 | 1.7 | 1.7 | 1.8 | ns |
| SSTL2 I | 0.9 | 1.7 | 1.7 | 1.7 | 1.7 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | ns |
| SSTL2 II | 0.8 | 1.6 | 1.6 | 1.6 | 1.6 | 1.7 | 1.7 | 1.7 | 1.7 | 1.7 | ns |
| SSTL3 I | 0.8 | 1.6 | 1.7 | 1.7 | 1.7 | 1.7 | 1.7 | 1.7 | 1.8 | 1.8 | ns |
| SSTL3 II | 0.7 | 1.5 | 1.5 | 1.6 | 1.6 | 1.6 | 1.6 | 1.6 | 1.6 | 1.7 | ns |
| CTT | 1.0 | 1.8 | 1.8 | 1.8 | 1.9 | 1.9 | 1.9 | 1.9 | 1.9 | 2.0 | ns |
| AGP | 1.0 | 1.8 | 1.8 | 1.9 | 1.9 | 1.9 | 1.9 | 1.9 | 1.9 | 2.0 | ns |

*S = Slow Slew Rate, F = Fast Slew Rate

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Input and output timing is measured at 1.4 V for LVTTL. For other I/O standards, see Table 3. In all cases, an 8 pF external capacitive load is used.

| Date | Version | Revision |
|---|---|---|
| 01/00 | 1.9 | Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes. |
| 03/00 | 2.0 | New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration. |
| 05/00 | 2.1 | Modified "Pins not listed..." statement. Speed grade update to Final status. |
| 05/00 | 2.2 | Modified Table 18. |
| 09/00 | 2.3 | • Added XCV400 values to table under **Minimum Clock-to-Out for Virtex Devices**.<br>• Corrected Units column in table under **IOB Input Switching Characteristics**.<br>• Added values to table under **CLB SelectRAM Switching Characteristics**. |
| 10/00 | 2.4 | • Corrected Pinout information for devices in the BG256, BG432, and BG560 packages in Table 18.<br>• Corrected **BG256 Pin Function Diagram**. |
| 04/02/01 | 2.5 | • Revised minimums for **Global Clock Set-Up and Hold for LVTTL Standard, with DLL**.<br>• Converted file to modularized format. See the **Virtex Data Sheet** section. |
| 04/19/01 | 2.6 | • Clarified TIOCKP and TIOCKON **IOB Output Switching Characteristics** descriptors. |
| 07/19/01 | 2.7 | • Under **Absolute Maximum Ratings**, changed ($T_{SOL}$) to 220 °C. |
| 07/26/01 | 2.8 | • Removed $T_{SOL}$ parameter and added footnote to **Absolute Maximum Ratings** table. |
| 10/29/01 | 2.9 | • Updated the speed grade designations used in data sheets, and added Table 1, which shows the current speed grade designation for each device. |
| 02/01/02 | 3.0 | • Added footnote to **DC Input and Output Levels** table. |
| 07/19/02 | 3.1 | • Removed mention of MIL-M-38510/605 specification.<br>• Added link to xapp158 from the **Power-On Power Supply Requirements** section. |
| 09/10/02 | 3.2 | • Added Clock CLK to **IOB Input Switching Characteristics** and **IOB Output Switching Characteristics**. |
| 03/01/13 | 4.0 | The products listed in this data sheet are obsolete. See **XCN10016** for further information. |

## Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

- DS003-1, Virtex 2.5V FPGAs:
  Introduction and Ordering Information (Module 1)
- DS003-2, Virtex 2.5V FPGAs:
  Functional Description (Module 2)
- DS003-3, Virtex 2.5V FPGAs:
  DC and Switching Characteristics (Module 3)
- DS003-4, Virtex 2.5V FPGAs:
  Pinout Tables (Module 4)

# Virtex Pinout Information

## Pinout Tables

See **www.xilinx.com** for updates or additional pinout information. For convenience, Table 2, Table 3 and Table 4 list the locations of special-purpose and power-supply pins. Pins not listed are either user I/Os or not connected, depending on the device/package combination. See the Pinout Diagrams starting on page 17 for any pins not listed for a particular part/package combination.

*Table 2:* **Virtex Pinout Tables (Chip-Scale and QFP Packages)**

| Pin Name | Device | CS144 | TQ144 | PQ/HQ240 |
|---|---|---|---|---|
| GCK0 | All | K7 | 90 | 92 |
| GCK1 | All | M7 | 93 | 89 |
| GCK2 | All | A7 | 19 | 210 |
| GCK3 | All | A6 | 16 | 213 |
| M0 | All | M1 | 110 | 60 |
| M1 | All | L2 | 112 | 58 |
| M2 | All | N2 | 108 | 62 |
| CCLK | All | B13 | 38 | 179 |
| PROGRAM | All | L12 | 72 | 122 |
| DONE | All | M12 | 74 | 120 |
| INIT | All | L13 | 71 | 123 |
| BUSY/DOUT | All | C11 | 39 | 178 |
| D0/DIN | All | C12 | 40 | 177 |
| D1 | All | E10 | 45 | 167 |
| D2 | All | E12 | 47 | 163 |
| D3 | All | F11 | 51 | 156 |
| D4 | All | H12 | 59 | 145 |
| D5 | All | J13 | 63 | 138 |
| D6 | All | J11 | 65 | 134 |
| D7 | All | K10 | 70 | 124 |
| WRITE | All | C10 | 32 | 185 |
| CS | All | D10 | 33 | 184 |
| TDI | All | A11 | 34 | 183 |
| TDO | All | A12 | 36 | 181 |
| TMS | All | B1 | 143 | 2 |
| TCK | All | C3 | 2 | 239 |
| $V_{CCINT}$ | All | A9, B6, C5, G3, G12, M5, M9, N6 | 10, 15, 25, 57, 84, 94, 99, 126 | 16, 32, 43, 77, 88, 104, 137, 148, 164, 198, 214, 225 |

*Table 3:* **Virtex Pinout Tables (BGA)**

| Pin Name | Device | BG256 | BG352 | BG432 | BG560 |
|---|---|---|---|---|---|
| GCK0 | All | Y11 | AE13 | AL16 | AL17 |
| GCK1 | All | Y10 | AF14 | AK16 | AJ17 |
| GCK2 | All | A10 | B14 | A16 | D17 |
| GCK3 | All | B10 | D14 | D17 | A17 |
| M0 | All | Y1 | AD24 | AH28 | AJ29 |
| M1 | All | U3 | AB23 | AH29 | AK30 |
| M2 | All | W2 | AC23 | AJ28 | AN32 |
| CCLK | All | B19 | C3 | D4 | C4 |
| PROGRAM | All | Y20 | AC4 | AH3 | AM1 |
| DONE | All | W19 | AD3 | AH4 | AJ5 |
| INIT | All | U18 | AD2 | AJ2 | AH5 |
| BUSY/DOUT | All | D18 | E4 | D3 | D4 |
| D0/DIN | All | C19 | D3 | C2 | E4 |
| D1 | All | E20 | G1 | K4 | K3 |
| D2 | All | G19 | J3 | K2 | L4 |
| D3 | All | J19 | M3 | P4 | P3 |
| D4 | All | M19 | R3 | V4 | W4 |
| D5 | All | P19 | U4 | AB1 | AB5 |
| D6 | All | T20 | V3 | AB3 | AC4 |
| D7 | All | V19 | AC3 | AG4 | AJ4 |
| WRITE | All | A19 | D5 | B4 | D6 |
| CS | All | B18 | C4 | D5 | A2 |
| TDI | All | C17 | B3 | B3 | D5 |
| TDO | All | A20 | D4 | C4 | E6 |
| TMS | All | D3 | D23 | D29 | B33 |
| TCK | All | A1 | C24 | D28 | E29 |
| DXN | All | W3 | AD23 | AH27 | AK29 |
| DXP | All | V4 | AE24 | AK29 | AJ28 |

*Table 3:* **Virtex Pinout Tables (BGA)** ***(Continued)***

| Pin Name | Device | BG256 | BG352 | BG432 | BG560 |
|---|---|---|---|---|---|
| $V_{CCO}$, Bank 7 | All | G4, H4 | G23, K26, N23 | A31, L28, L31 | C32, D33, K33, N32, T33 |
| $V_{REF}$, Bank 0<br>(VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)<br>Within each bank, if input reference voltage is not required, all $V_{REF}$ pins are general I/O. | XCV50 | A8, B4 | N/A | N/A | N/A |
| | XCV100/150 | ... + A4 | A16,C19, C21 | N/A | N/A |
| | XCV200/300 | ... + A2 | ... + D21 | B19, D22, D24, D26 | N/A |
| | XCV400 | N/A | N/A | ... + C18 | A19, D20, D26, E23, E27 |
| | XCV600 | N/A | N/A | ... + C24 | ... + E24 |
| | XCV800 | N/A | N/A | ... + B21 | ... + E21 |
| | XCV1000 | N/A | N/A | N/A | ... + D29 |
| $V_{REF}$, Bank 1<br>(VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)<br>Within each bank, if input reference voltage is not required, all $V_{REF}$ pins are general I/O. | XCV50 | A17, B12 | N/A | N/A | N/A |
| | XCV100/150 | ... + B15 | B6, C9, C12 | N/A | N/A |
| | XCV200/300 | ... + B17 | ... + D6 | A13, B7, C6, C10 | N/A |
| | XCV400 | N/A | N/A | ... + B15 | A6, D7, D11, D16, E15 |
| | XCV600 | N/A | N/A | ... + D10 | ... + D10 |
| | XCV800 | N/A | N/A | ... + B12 | ... + D13 |
| | XCV1000 | N/A | N/A | N/A | ... + E7 |
| $V_{REF}$, Bank 2<br>($V_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)<br>Within each bank, if input reference voltage is not required, all $V_{REF}$ pins are general I/O. | XCV50 | C20, J18 | N/A | N/A | N/A |
| | XCV100/150 | ... + F19 | E2, H2, M4 | N/A | N/A |
| | XCV200/300 | ... + G18 | ... + D2 | E2, G3, J2, N1 | N/A |
| | XCV400 | N/A | N/A | ... + R3 | G5, H4, L5, P4, R1 |
| | XCV600 | N/A | N/A | ... + H1 | ... + K5 |
| | XCV800 | N/A | N/A | ... + M3 | ... + N5 |
| | XCV1000 | N/A | N/A | N/A | ... + B3 |

*Table 4:* **Virtex Pinout Tables (Fine-Pitch BGA)** ***(Continued)***

| Pin Name | Device | FG256 | FG456 | FG676 | FG680 |
|---|---|---|---|---|---|
| $V_{REF}$, Bank 4<br>($V_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)<br>Within each bank, if input reference voltage is not required, all $V_{REF}$ pins are general I/O. | XCV50 | P9, T12 | N/A | N/A | N/A |
| | XCV100/150 | ... + T11 | AA13, AB16, AB19 | N/A | N/A |
| | XCV200/300 | ... + R13 | ... + AB20 | N/A | N/A |
| | XCV400 | N/A | N/A | AC15, AD18, AD21, AD22, AF15 | N/A |
| | XCV600 | N/A | N/A | ... + AF20 | AT19, AU7, AU17, AV8, AV10, AW11 |
| | XCV800 | N/A | N/A | ... + AF17 | ... + AV14 |
| | XCV1000 | N/A | N/A | N/A | ... + AU6 |
| $V_{REF}$, Bank 5<br>($V_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)<br>Within each bank, if input reference voltage is not required, all $V_{REF}$ pins are general I/O. | XCV50 | T4, P8 | N/A | N/A | N/A |
| | XCV100/150 | ... + R5 | W8, Y10, AA5 | N/A | N/A |
| | XCV200/300 | ... + T2 | ... + Y6 | N/A | N/A |
| | XCV400 | N/A | N/A | AA10, AB8, AB12, AC7, AF12 | N/A |
| | XCV600 | N/A | N/A | ... + AF8 | AT27, AU29, AU31, AV35, AW21, AW23 |
| | XCV800 | N/A | N/A | ... + AE10 | ... + AT25 |
| | XCV1000 | N/A | N/A | N/A | ... + AV36 |
| $V_{REF}$, Bank 6<br>($V_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)<br>Within each bank, if input reference voltage is not required, all $V_{REF}$ pins are general I/O. | XCV50 | J3, N1 | N/A | N/A | N/A |
| | XCV100/150 | ... + M1 | N2, R4, T3 | N/A | N/A |
| | XCV200/300 | ... + N2 | ... + Y1 | N/A | N/A |
| | XCV400 | N/A | N/A | AB3, R1, R4, U6, V5 | N/A |
| | XCV600 | N/A | N/A | ... + Y1 | AB35, AD37, AH39, AK39, AM39, AN36 |
| | XCV800 | N/A | N/A | ... + U2 | ... + AE39 |
| | XCV1000 | N/A | N/A | N/A | ... + AT39 |

*Table 4:* **Virtex Pinout Tables (Fine-Pitch BGA)** ***(Continued)***

| Pin Name | Device | FG256 | FG456 | FG676 | FG680 |
|---|---|---|---|---|---|
| No Connect<br>(No-connect pins are listed incrementally. All pins listed for both the required device and all larger devices listed in the same package are no connects.) | XCV800 | N/A | N/A | A2, A3, A15, A25, B1, B6, B11, B16, B21, B24, B26, C1, C2, C25, C26, F2, F6, F21, F25, L2, L25, N25, P2, T2, T25, AA2, AA6, AA21, AA25, AD1, AD2, AD25, AE1, AE3, AE6, AE11, AE14, AE16, AE21, AE24, AE26, AF2, AF24, AF25 | N/A |
| | XCV600 | N/A | N/A | same as above | N/A |
| | XCV400 | N/A | N/A | ... + A9, A10, A13, A16, A24, AC1, AC25, AE12, AE15, AF3, AF10, AF11, AF13, AF14, AF16, AF18, AF23, B4, B12, B13, B15, B17, D1, D25, H26, J1, K26, L1, M1, M25, N1, N26, P1, P26, R2, R26, T1, T26, U26, V1 | N/A |
| | XCV300 | N/A | D4, D19, W4, W19 | N/A | N/A |
| | XCV200 | N/A | ... + A2, A6, A12, B11, B16, C2, D1, D18, E17, E19, G2, G22, L2, L19, M2, M21, R3, R20, U3, U18, Y22, AA1, AA3, AA11, AA16, AB7, AB12, AB21, | N/A | N/A |
| | XCV150 | N/A | ... + A13, A14, C8, C9, E13, F11, H21, J1, J4, K2, K18, K19, M17, N1, P1, P5, P22, R22, W13, W15, AA9, AA10, AB8, AB14 | N/A | N/A |

## TQ144 Pin Function Diagram

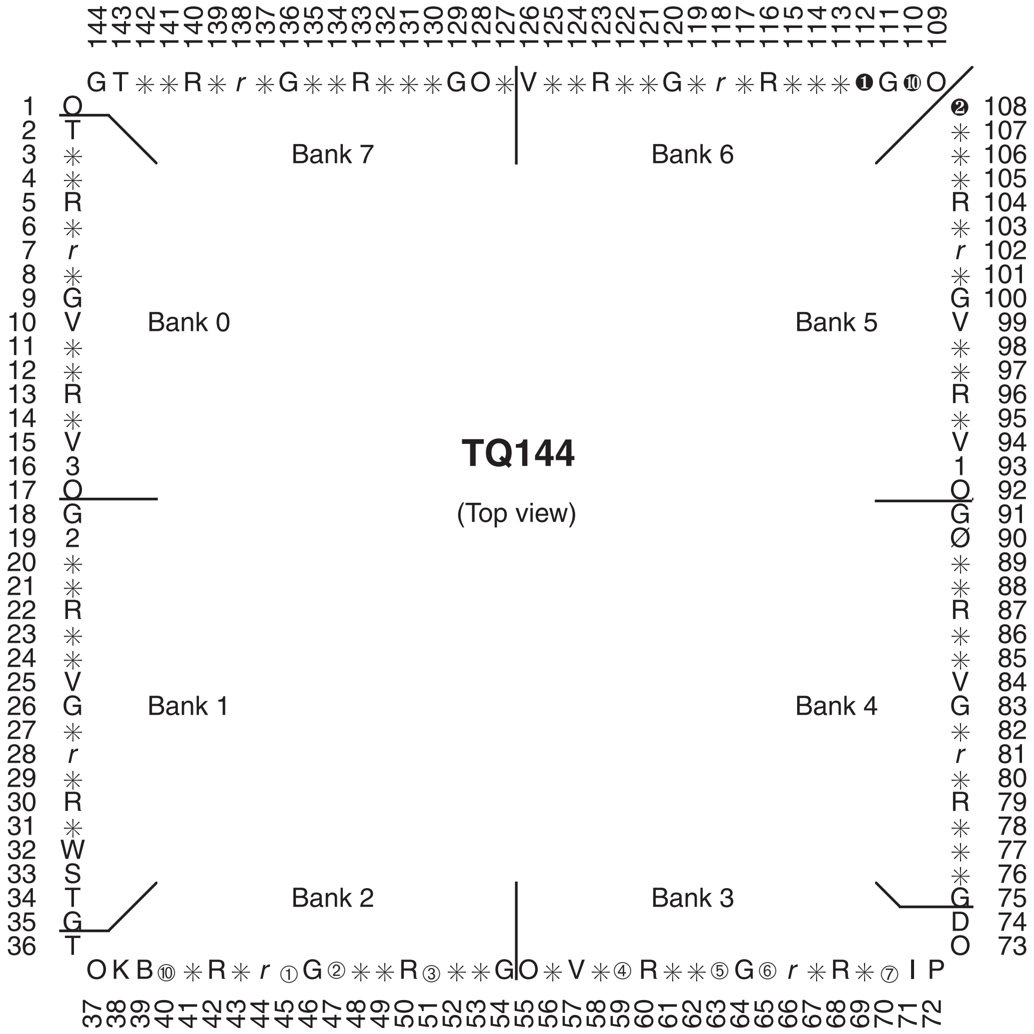


*Figure 2:* **TQ144 Pin Function Diagram**

## FG256 Pin Function Diagram

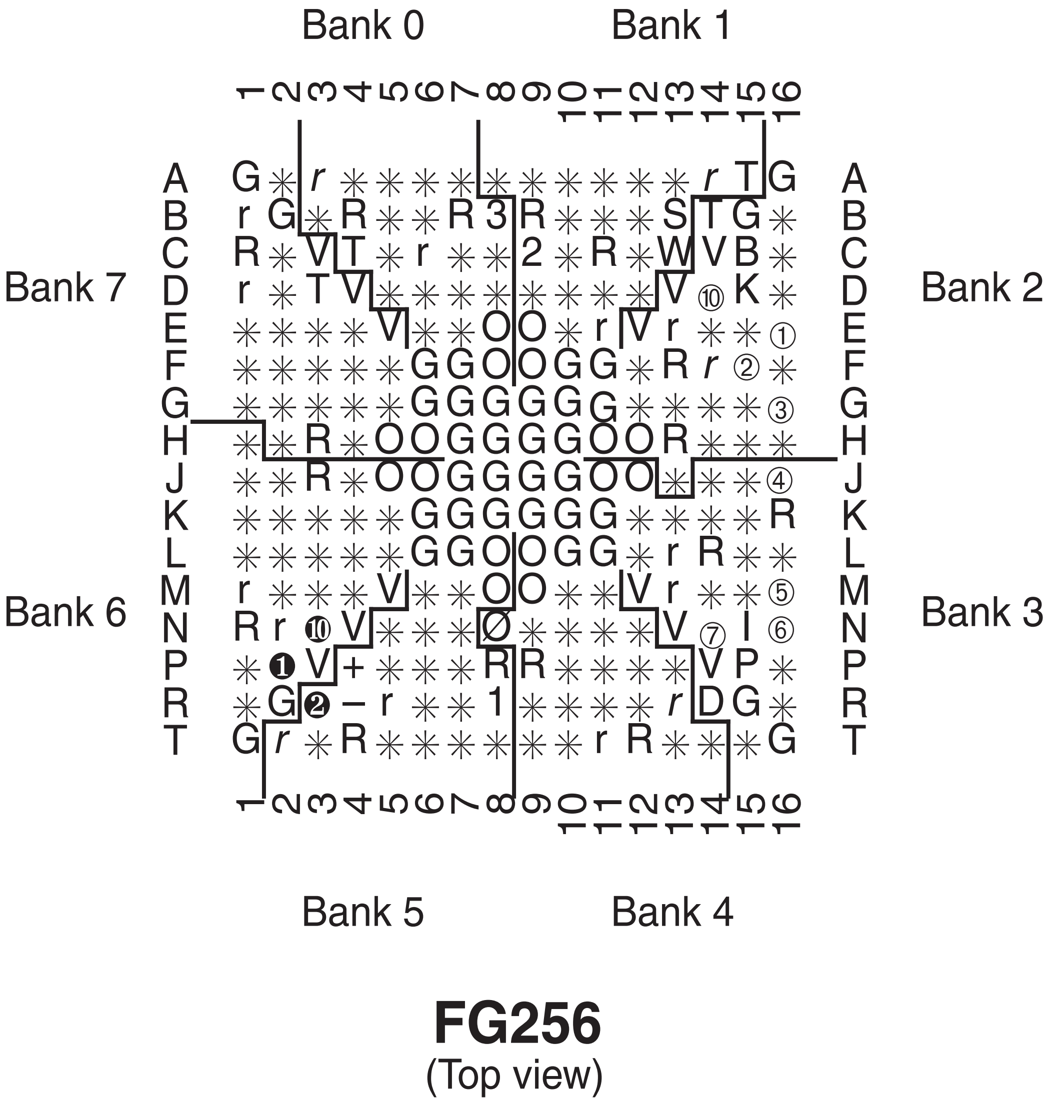
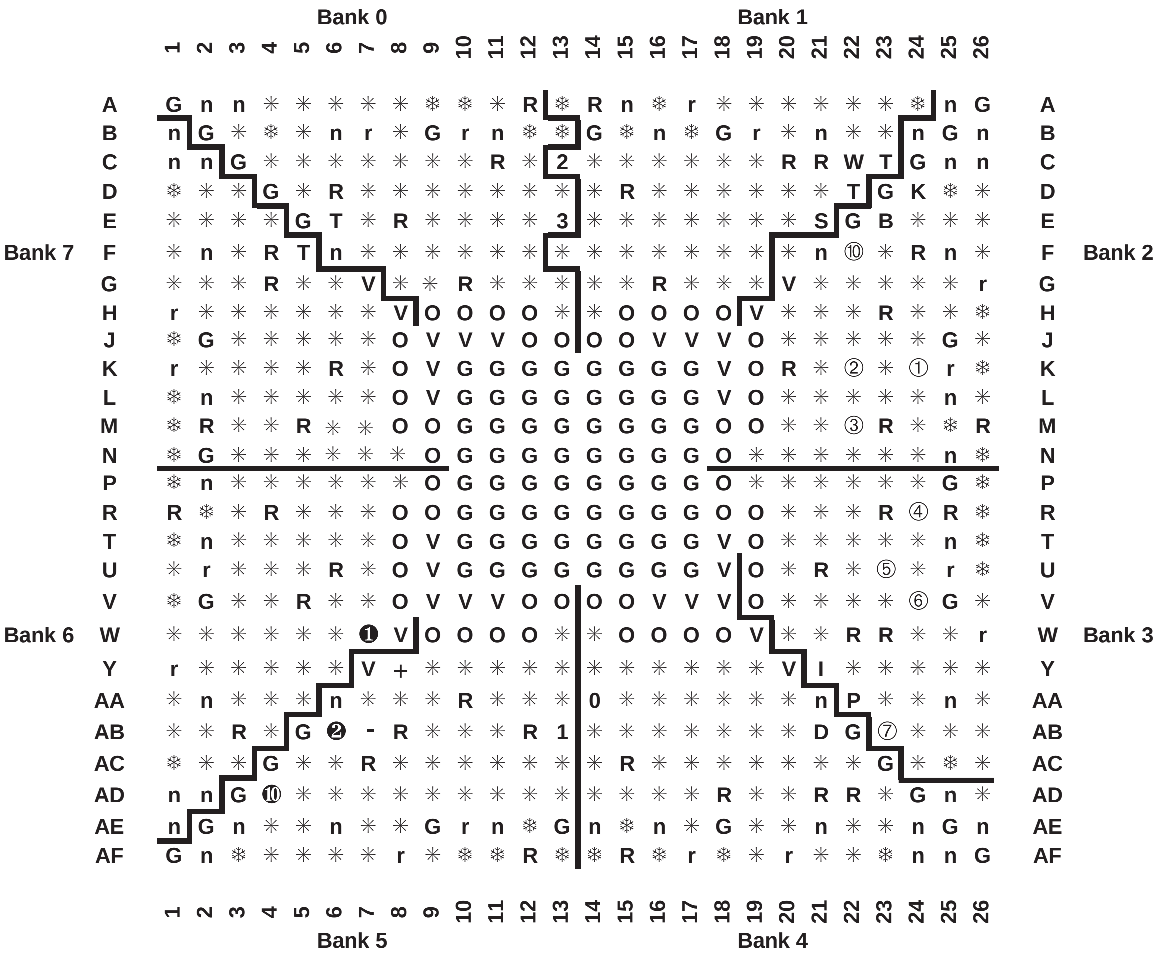


*Figure 8:* **FG256 Pin Function Diagram**

## FG676 Pin Function Diagram



| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | G | n | n | ✳ | ✳ | ✳ | ✳ | ✳ | ❄ | ❄ | ✳ | R | ❄ | R | n | ❄ | r | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ❄ | n | G | A |
| B | n | G | ✳ | ❄ | ✳ | n | r | ✳ | G | r | n | ❄ | ❄ | G | ❄ | n | ❄ | G | r | ✳ | n | ✳ | ✳ | n | G | n | B |
| C | n | n | G | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | R | ✳ | 2 | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | R | R | W | T | G | n | n | C |
| D | ❄ | ✳ | ✳ | G | ✳ | R | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | R | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | T | G | K | ❄ | ✳ | D |
| E | ✳ | ✳ | ✳ | ✳ | G | T | ✳ | R | ✳ | ✳ | ✳ | ✳ | 3 | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | S | G | B | ✳ | ✳ | ✳ | E |
| F | ✳ | n | ✳ | R | T | n | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | n | ⑩ | ✳ | R | n | ✳ | F |
| G | ✳ | ✳ | ✳ | R | ✳ | ✳ | V | ✳ | ✳ | R | ✳ | ✳ | ✳ | ✳ | ✳ | R | ✳ | ✳ | ✳ | V | ✳ | ✳ | ✳ | ✳ | ✳ | r | G |
| H | r | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | V | O | O | O | O | ✳ | ✳ | O | O | O | O | V | ✳ | ✳ | ✳ | R | ✳ | ✳ | ❄ | H |
| J | ❄ | G | ✳ | ✳ | ✳ | ✳ | ✳ | O | V | V | V | O | O | O | O | V | V | V | O | ✳ | ✳ | ✳ | ✳ | ✳ | G | ✳ | J |
| K | r | ✳ | ✳ | ✳ | ✳ | R | ✳ | O | V | G | G | G | G | G | G | G | G | V | O | R | ✳ | ② | ✳ | ① | r | ❄ | K |
| L | ❄ | n | ✳ | ✳ | ✳ | ✳ | ✳ | O | V | G | G | G | G | G | G | G | G | V | O | ✳ | ✳ | ✳ | ✳ | ✳ | n | ✳ | L |
| M | ❄ | R | ✳ | ✳ | R | ✳ | ✳ | O | O | G | G | G | G | G | G | G | G | O | O | ✳ | ✳ | ③ | R | ✳ | ❄ | R | M |
| N | ❄ | G | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | O | G | G | G | G | G | G | G | G | O | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | n | ❄ | N |
| P | ❄ | n | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | O | G | G | G | G | G | G | G | G | O | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | G | ❄ | P |
| R | R | ❄ | ✳ | R | ✳ | ✳ | ✳ | O | O | G | G | G | G | G | G | G | G | O | O | ✳ | ✳ | ✳ | R | ④ | R | ❄ | R |
| T | ❄ | n | ✳ | ✳ | ✳ | ✳ | ✳ | O | V | G | G | G | G | G | G | G | G | V | O | ✳ | ✳ | ✳ | ✳ | ✳ | n | ❄ | T |
| U | ✳ | r | ✳ | ✳ | ✳ | R | ✳ | O | V | G | G | G | G | G | G | G | G | V | O | ✳ | R | ✳ | ⑤ | ✳ | r | ❄ | U |
| V | ❄ | G | ✳ | ✳ | R | ✳ | ✳ | O | V | V | V | O | O | O | O | V | V | V | O | ✳ | ✳ | ✳ | ✳ | ⑥ | G | ✳ | V |
| W | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ❶ | V | O | O | O | O | ✳ | ✳ | O | O | O | O | V | ✳ | ✳ | R | R | ✳ | ✳ | r | W |
| Y | r | ✳ | ✳ | ✳ | ✳ | ✳ | V | + | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | V | I | ✳ | ✳ | ✳ | ✳ | ✳ | Y |
| AA | ✳ | n | ✳ | ✳ | ✳ | n | ✳ | ✳ | ✳ | R | ✳ | ✳ | ✳ | 0 | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | n | P | ✳ | ✳ | n | ✳ | AA |
| AB | ✳ | ✳ | R | ✳ | G | ❷ | - | R | ✳ | ✳ | ✳ | R | 1 | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | D | G | ⑦ | ✳ | ✳ | ✳ | AB |
| AC | ❄ | ✳ | ✳ | G | ✳ | ✳ | R | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | R | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | G | ✳ | ❄ | ✳ | AC |
| AD | n | n | G | ❿ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | R | ✳ | ✳ | R | R | ✳ | G | n | ✳ | AD |
| AE | n | G | n | ✳ | ✳ | n | ✳ | ✳ | G | r | n | ❄ | G | n | ❄ | n | ✳ | G | ✳ | ✳ | n | ✳ | ✳ | n | G | n | AE |
| AF | G | n | ❄ | ✳ | ✳ | ✳ | ✳ | r | ✳ | ❄ | ❄ | R | ❄ | ❄ | R | ❄ | r | ❄ | ✳ | r | ✳ | ✳ | ❄ | n | n | G | AF |

**FG676**
(Top view)

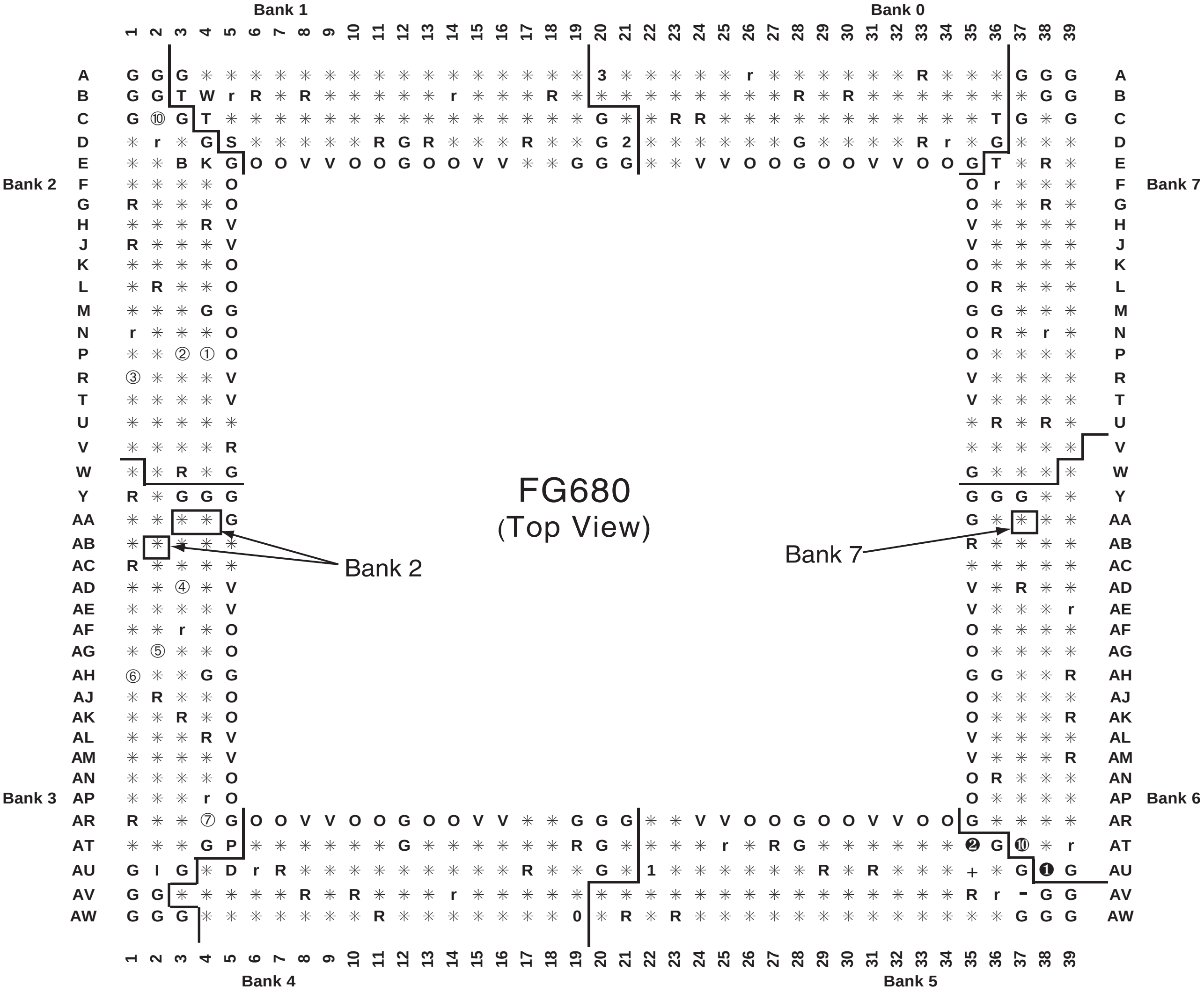
fg676a

*Figure 10:* **FG676 Pin Function Diagram**

**Notes:**

Packages FG456 and FG676 are layout compatible.

## FG680 Pin Function Diagram



| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | G | G | G | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | 3 | ✳ | ✳ | ✳ | ✳ | ✳ | r | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | R | ✳ | ✳ | ✳ | G | G | G |
| B | G | G | T | W | r | R | ✳ | R | ✳ | ✳ | ✳ | ✳ | ✳ | r | ✳ | ✳ | ✳ | R | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | R | ✳ | R | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | G | G |
| C | G | ⑩ | G | T | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | G | ✳ | ✳ | R | R | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | T | G | ✳ | G |
| D | ✳ | r | ✳ | G | S | ✳ | ✳ | ✳ | ✳ | ✳ | R | G | R | ✳ | ✳ | ✳ | R | ✳ | ✳ | G | 2 | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | G | ✳ | ✳ | ✳ | ✳ | R | r | ✳ | G | ✳ | ✳ | ✳ |
| E | ✳ | ✳ | B | K | G | O | O | V | V | O | O | G | O | O | V | V | ✳ | ✳ | G | G | G | ✳ | ✳ | V | V | O | O | G | O | O | V | V | O | O | G | T | ✳ | R | ✳ |
| F | ✳ | ✳ | ✳ | ✳ | O | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | O | r | ✳ | ✳ | ✳ |
| G | R | ✳ | ✳ | ✳ | O | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | O | ✳ | ✳ | R | ✳ |
| H | ✳ | ✳ | ✳ | R | V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | V | ✳ | ✳ | ✳ | ✳ |
| J | R | ✳ | ✳ | ✳ | V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | V | ✳ | ✳ | ✳ | ✳ |
| K | ✳ | ✳ | ✳ | ✳ | O | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | O | ✳ | ✳ | ✳ | ✳ |
| L | ✳ | R | ✳ | ✳ | O | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | O | R | ✳ | ✳ | ✳ |
| M | ✳ | ✳ | ✳ | G | G | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | G | G | ✳ | ✳ | ✳ |
| N | r | ✳ | ✳ | ✳ | O | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | O | R | ✳ | r | ✳ |
| P | ✳ | ✳ | ② | ① | O | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | O | ✳ | ✳ | ✳ | ✳ |
| R | ③ | ✳ | ✳ | ✳ | V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | V | ✳ | ✳ | ✳ | ✳ |
| T | ✳ | ✳ | ✳ | ✳ | V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | V | ✳ | ✳ | ✳ | ✳ |
| U | ✳ | ✳ | ✳ | ✳ | ✳ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | ✳ | R | ✳ | R | ✳ |
| V | ✳ | ✳ | ✳ | ✳ | R | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | ✳ | ✳ | ✳ | ✳ | ✳ |
| W | ✳ | ✳ | R | ✳ | G | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | G | ✳ | ✳ | ✳ | ✳ |
| Y | R | ✳ | G | G | G | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | G | G | G | ✳ | ✳ |
| AA | ✳ | ✳ | ✳ | ✳ | G | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | G | ✳ | ✳ | ✳ | ✳ |
| AB | ✳ | ✳ | ✳ | ✳ | ✳ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | R | ✳ | ✳ | ✳ | ✳ |
| AC | R | ✳ | ✳ | ✳ | ✳ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | ✳ | ✳ | ✳ | ✳ | ✳ |
| AD | ✳ | ✳ | ④ | ✳ | V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | V | ✳ | R | ✳ | ✳ |
| AE | ✳ | ✳ | ✳ | ✳ | V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | V | ✳ | ✳ | ✳ | r |
| AF | ✳ | ✳ | r | ✳ | O | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | O | ✳ | ✳ | ✳ | ✳ |
| AG | ✳ | ⑤ | ✳ | ✳ | O | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | O | ✳ | ✳ | ✳ | ✳ |
| AH | ⑥ | ✳ | ✳ | G | G | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | G | G | ✳ | ✳ | R |
| AJ | ✳ | R | ✳ | ✳ | O | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | O | ✳ | ✳ | ✳ | ✳ |
| AK | ✳ | ✳ | R | ✳ | O | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | O | ✳ | ✳ | ✳ | R |
| AL | ✳ | ✳ | ✳ | R | V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | V | ✳ | ✳ | ✳ | ✳ |
| AM | ✳ | ✳ | ✳ | ✳ | V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | V | ✳ | ✳ | ✳ | R |
| AN | ✳ | ✳ | ✳ | ✳ | O | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | O | R | ✳ | ✳ | ✳ |
| AP | ✳ | ✳ | ✳ | r | O | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | O | ✳ | ✳ | ✳ | ✳ |
| AR | R | ✳ | ✳ | ⑦ | G | O | O | V | V | O | O | G | O | O | V | V | ✳ | ✳ | G | G | G | ✳ | ✳ | V | V | O | O | G | O | O | V | V | O | O | G | ✳ | ✳ | ✳ | ✳ |
| AT | ✳ | ✳ | ✳ | G | P | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | G | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | R | G | ✳ | ✳ | ✳ | ✳ | r | ✳ | R | G | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ❷ | G | ⓾ | ✳ | r |
| AU | G | I | G | ✳ | D | r | R | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | R | ✳ | ✳ | G | ✳ | 1 | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | R | ✳ | R | ✳ | ✳ | ✳ | + | ✳ | G | ❶ | G |
| AV | G | G | ✳ | ✳ | ✳ | ✳ | ✳ | R | ✳ | R | ✳ | ✳ | ✳ | r | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | R | r | - | G | G |
| AW | G | G | G | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | R | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | 0 | ✳ | R | ✳ | R | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | ✳ | G | G | G |

**Note**: AA3, AA4, and AB2 are in Bank 2

**Note**: AA37 is in Bank 7

fg680_12a

*Figure 11:* **FG680 Pin Function Diagram**