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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	4704
Number of Logic Elements/Cells	21168
Total RAM Bits	114688
Number of I/O	444
Number of Gates	888439
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xcv800-4fg676i">https://www.e-xfl.com/product-detail/xilinx/xcv800-4fg676i</a>

more I/O pins convert to  $V_{REF}$  pins. Since these are always a superset of the  $V_{REF}$  pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary. All the  $V_{REF}$  pins for the largest device anticipated must be connected to the  $V_{REF}$  voltage, and not used for I/O.

In smaller devices, some  $V_{CCO}$  pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or can be connected to the  $V_{CCO}$  voltage to permit migration to a larger device if necessary.

In TQ144 and PQ/HQ240 packages, all  $V_{CCO}$  pins are bonded together internally, and consequently the same  $V_{CCO}$  voltage must be connected to all of them. In the CS144 package, bank pairs that share a side are interconnected internally, permitting four choices for  $V_{CCO}$ . In both cases, the  $V_{REF}$  pins remain internally connected as eight banks, and can be used as described previously.

## Configurable Logic Block

The basic building block of the Virtex CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and a storage element. The output from the function generator in each LC drives both the CLB output and the D input of the flip-flop. Each Virtex CLB contains four LCs, organized in two similar slices, as shown in Figure 4.

Figure 5 shows a more detailed view of a single slice.

In addition to the four basic LCs, the Virtex CLB contains logic that combines function generators to provide functions

of five or six inputs. Consequently, when estimating the number of system gates provided by a given device, each CLB counts as 4.5 LCs.

## Look-Up Tables

Virtex function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16x1-bit dual-port synchronous RAM.

The Virtex LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

## Storage Elements

The storage elements in the Virtex slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by the function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each Slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals can be configured to operate asynchronously. All of the control signals are independently invertible, and are shared by the two flip-flops within the slice.

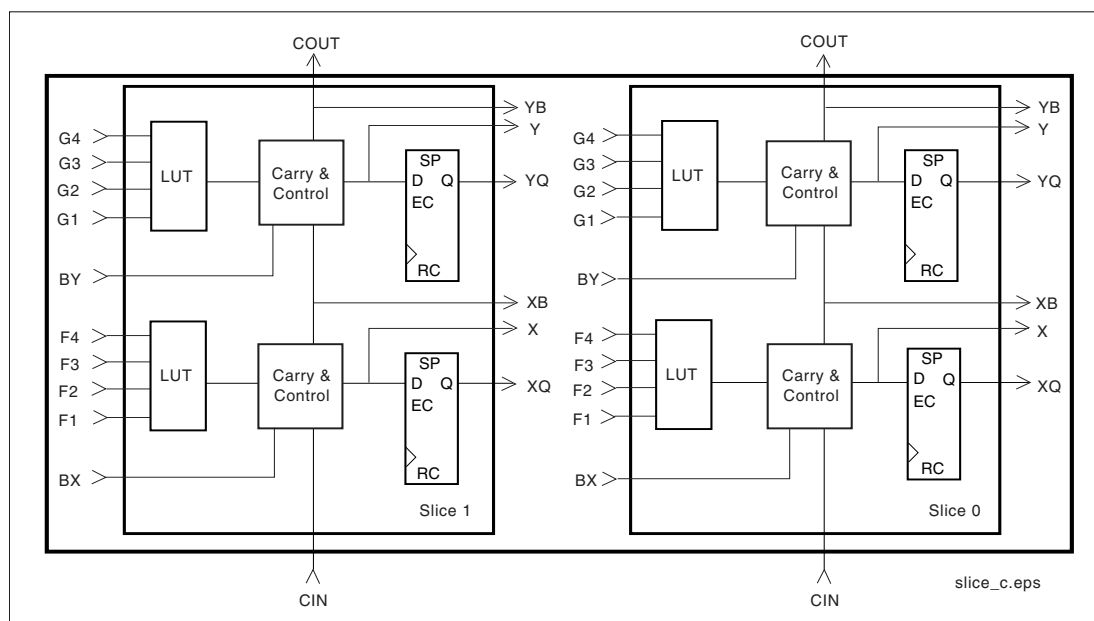


Figure 4: 2-Slice Virtex CLB

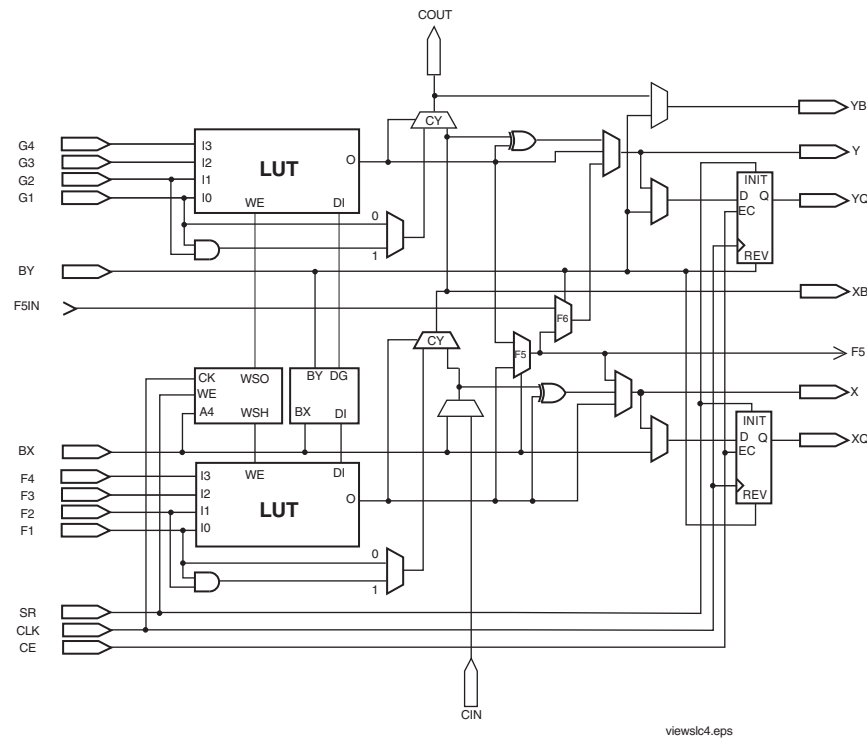


Figure 5: Detailed View of Virtex Slice

### Additional Logic

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Each CLB has four direct feedthrough paths, one per LC. These paths provide extra data input or additional local routing that does not consume logic resources.

### Arithmetic Logic

Dedicated carry logic provides fast arithmetic carry capability for high-speed arithmetic functions. The Virtex CLB supports two separate carry chains, one per Slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 1-bit full adder to be implemented within an LC. In addition, a dedicated AND gate improves the efficiency of multiplier implementation.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

### BUFTs

Each Virtex CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. See **Dedicated Routing**, page 7. Each Virtex BUFT has an independent 3-state control pin and an independent input pin.

### Block SelectRAM

Virtex FPGAs incorporate several large block SelectRAM memories. These complement the distributed LUT SelectRAMs that provide shallow RAM structures implemented in CLBs.

Block SelectRAM memory blocks are organized in columns. All Virtex devices contain two such columns, one along each vertical edge. These columns extend the full height of the chip. Each memory block is four CLBs high, and consequently, a Virtex device 64 CLBs high contains 16 memory blocks per column, and a total of 32 blocks.

**Table 3** shows the amount of block SelectRAM memory that is available in each Virtex device.

Table 3: Virtex Block SelectRAM Amounts

Device	# of Blocks	Total Block SelectRAM Bits
XCV50	8	32,768
XCV100	10	40,960
XCV150	12	49,152
XCV200	14	57,344
XCV300	16	65,536
XCV400	20	81,920
XCV600	24	98,304
XCV800	28	114,688
XCV1000	32	131,072

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

**Figure 10** is a diagram of the Virtex Series boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

### Instruction Set

The Virtex Series boundary scan instruction set also includes instructions to configure the device and read back configuration data (CFG\_IN, CFG\_OUT, and JSTART). The complete instruction set is coded as shown in **Table 5**.

### Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out, and 3-State Control. Non-IOB pins have appropriate partial bit population if input-only or output-only. Each EXTEST CAPTURED-OR state captures all In, Out, and 3-state pins.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA supports up to two additional internal scan chains that can be specified using the BSCAN macro. The macro provides two user pins (SEL1 and SEL2) which are decoded of the USER1 and USER2 instructions respectively. For these instructions, two corresponding pins (TDO1 and TDO2) allow user scan data to be shifted out of TDO.

Likewise, there are individual clock pins (DRCK1 and DRCK2) for each user register. There is a common input pin (TDI) and shared output pins that represent the state of the TAP controller (RESET, SHIFT, and UPDATE).

### Bit Sequence

The order within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

From a cavity-up view of the chip (as shown in EPIC), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in **Figure 11**.

BSDL (Boundary Scan Description Language) files for Virtex Series devices are available on the Xilinx web site in the File Download area.

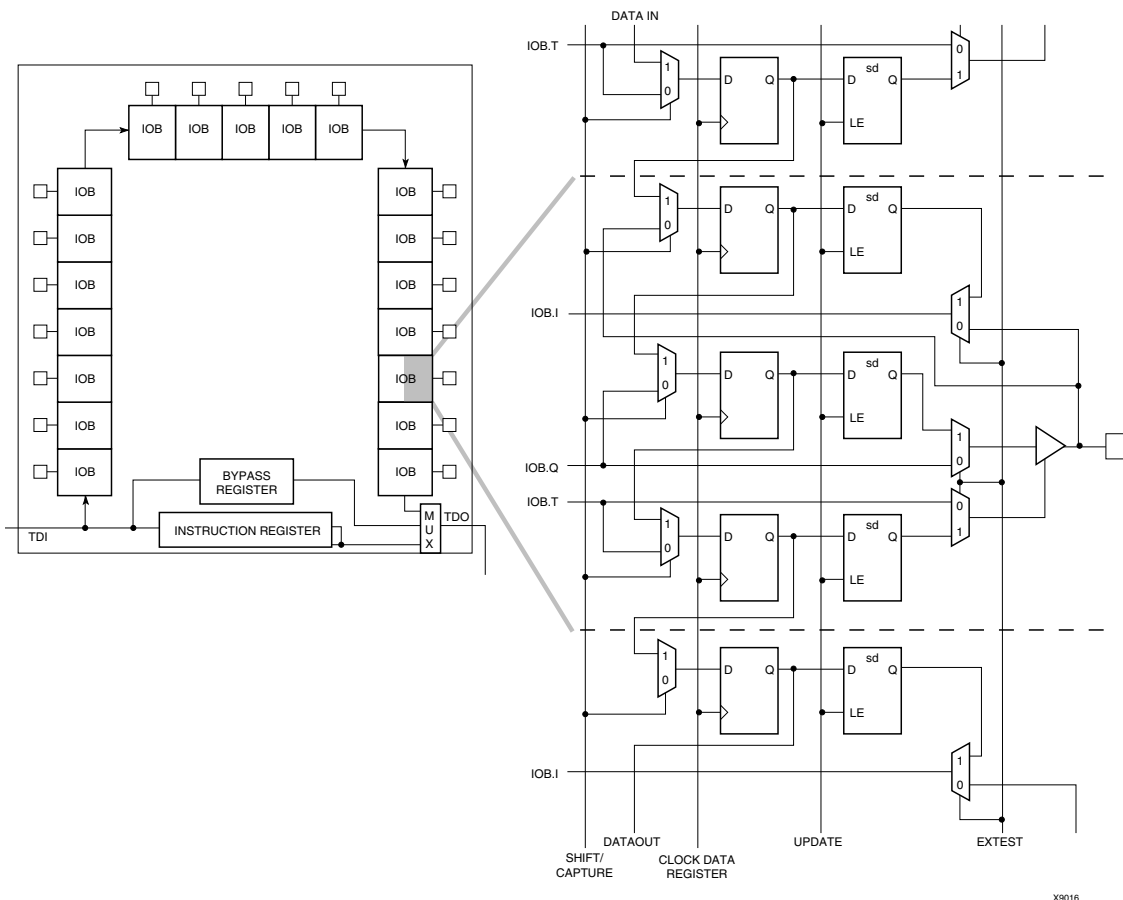
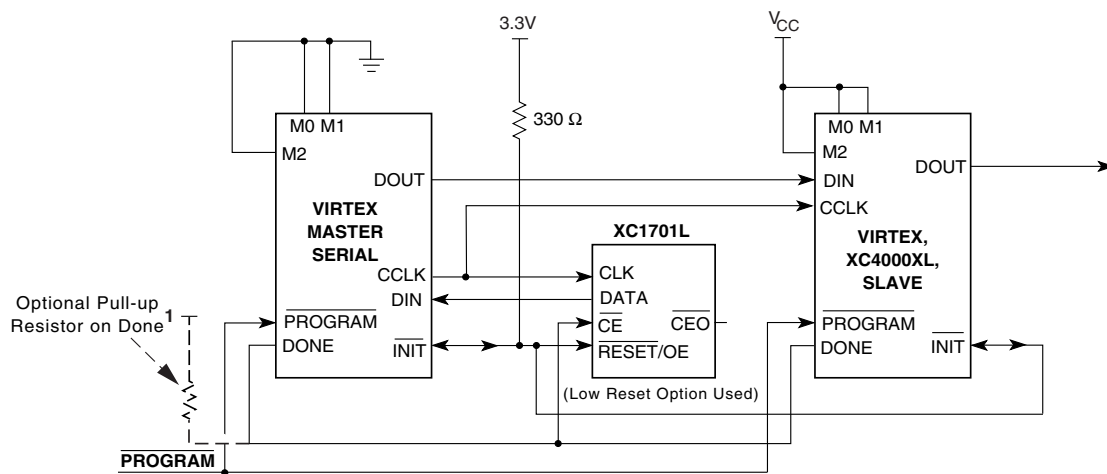


Figure 10: Virtex Series Boundary Scan Logic

Table 8: Master/Slave Serial Mode Programming Switching

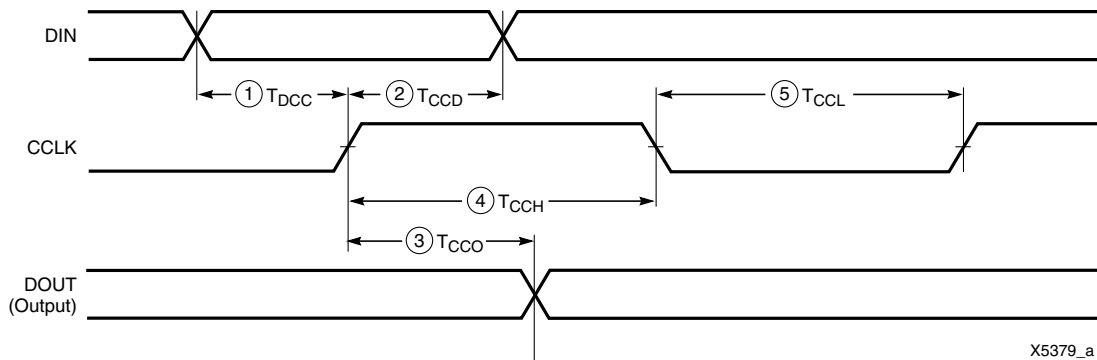
	Description	Figure References	Symbol	Values	Units
CCLK	DIN setup/hold, slave mode	1/2	$T_{DCC}/T_{CCD}$	5.0 / 0	ns, min
	DIN setup/hold, master mode	1/2	$T_{DSCK}/T_{CKDS}$	5.0 / 0	ns, min
	DOUT	3	$T_{CCO}$	12.0	ns, max
	High time	4	$T_{CCH}$	5.0	ns, min
	Low time	5	$T_{CCL}$	5.0	ns, min
	Maximum Frequency		$F_{CC}$	66	MHz, max
	Frequency Tolerance, master mode with respect to nominal			+45% -30%	



**Note 1:** If none of the Virtex FPGAs have been selected to drive DONE, an external pull-up resistor of 330 Ω should be added to the common DONE line. (For Spartan-XL devices, add a 4.7K Ω pull-up resistor.) This pull-up is not needed if the DriveDONE attribute is set. If used, DriveDONE should be selected only for the last device in the configuration chain.

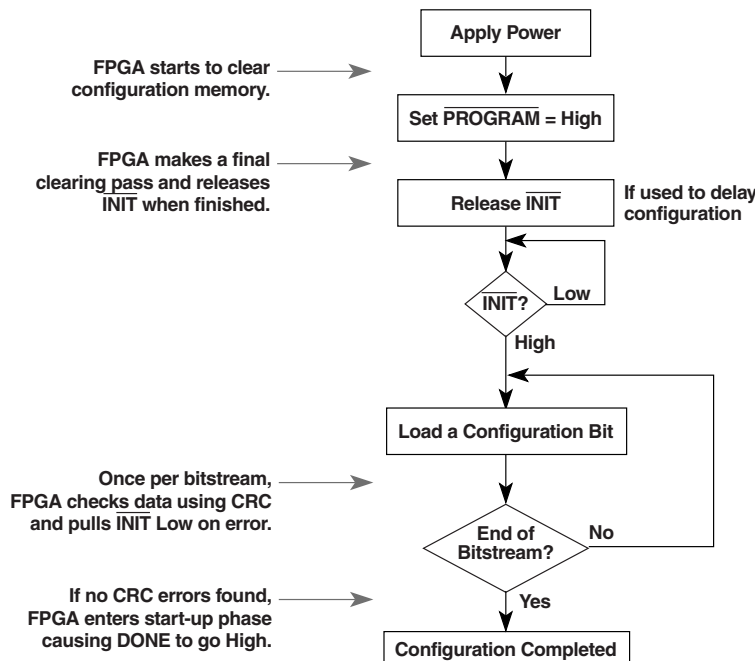
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Figure 12: Master/Slave Serial Mode Circuit Diagram



X5379\_a

Figure 13: Slave-Serial Mode Programming Switching Characteristics



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Figure 15: Serial Configuration Flowchart

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained to permit high-speed 8-bit readback.

Retention of the SelectMAP port is selectable on a design-by-design basis when the bitstream is generated. If retention is selected, PROHIBIT constraints are required to prevent the SelectMAP-port pins from being used as user I/O.

Multiple Virtex FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, WRITE, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the CS pin of each device in turn and writing the appropriate data. see Table 9 for SelectMAP Write Timing Characteristics.

Table 9: SelectMAP Write Timing Characteristics

	Description		Symbol		Units
CCLK	D <sub>0-7</sub> Setup/Hold	1/2	T <sub>SMDCC</sub> /T <sub>SMCCD</sub>	5.0 / 1.7	ns, min
	$\overline{\text{CS}}$ Setup/Hold	3/4	T <sub>SMCSCC</sub> /T <sub>SMCCCS</sub>	7.0 / 1.7	ns, min
	$\overline{\text{WRITE}}$ Setup/Hold	5/6	T <sub>SMCCW</sub> /T <sub>SMWCC</sub>	7.0 / 1.7	ns, min
	BUSY Propagation Delay	7	T <sub>SMCKBY</sub>	12.0	ns, max
	Maximum Frequency		F <sub>CC</sub>	66	MHz, max
	Maximum Frequency with no handshake		F <sub>CCNH</sub>	50	MHz, max

### Write

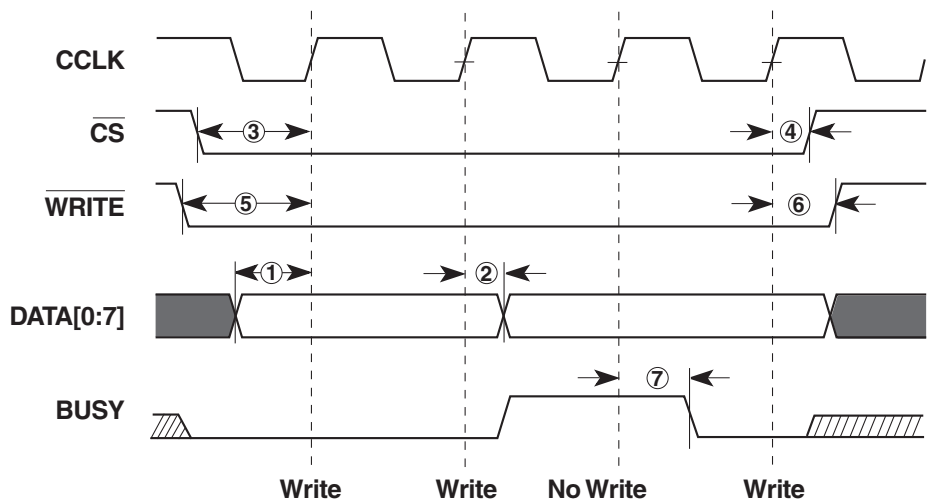
Write operations send packets of configuration data into the FPGA. The sequence of operations for a multi-cycle write operation is shown below. Note that a configuration packet can be split into many such sequences. The packet does not have to complete within one assertion of  $\overline{\text{CS}}$ , illustrated in Figure 16.

1. Assert  $\overline{\text{WRITE}}$  and  $\overline{\text{CS}}$  Low. Note that when  $\overline{\text{CS}}$  is asserted on successive CCLKs,  $\overline{\text{WRITE}}$  must remain either asserted or de-asserted. Otherwise an abort will be initiated, as described below.
2. Drive data onto D[7:0]. Note that to avoid contention, the data source should not be enabled while  $\overline{\text{CS}}$  is Low and  $\overline{\text{WRITE}}$  is High. Similarly, while  $\overline{\text{WRITE}}$  is High, no more than one  $\overline{\text{CS}}$  should be asserted.

3. At the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this has happened.
4. Repeat steps 2 and 3 until all the data has been sent.

5. De-assert  $\overline{\text{CS}}$  and  $\overline{\text{WRITE}}$ .

A flowchart for the write operation appears in [Figure 17](#). Note that if CCLK is slower than  $f_{\text{CCNH}}$ , the FPGA never asserts BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.



ds003\_16\_071902

Figure 16: Write Operations

## Data Stream Format

Virtex devices are configured by sequentially loading frames of data. Table 11 lists the total number of bits required to configure each device. For more detailed information, see application note XAPP151 “Virtex Configuration Architecture Advanced Users Guide”.

Table 11: Virtex Bit-Stream Lengths

Device	# of Configuration Bits
XCV50	559,200
XCV100	781,216
XCV150	1,040,096
XCV200	1,335,840
XCV300	1,751,808
XCV400	2,546,048
XCV600	3,607,968
XCV800	4,715,616
XCV1000	6,127,744

## Readback

The configuration data stored in the Virtex configuration memory can be readback for verification. Along with the configuration data it is possible to readback the contents all flip-flops/latches, LUTRAMs, and block RAMs. This capability is used for real-time debugging.

For more detailed information, see Application Note XAPP138: *Virtex FPGA Series Configuration and Readback*, available online at [www.xilinx.com](http://www.xilinx.com).

## Revision History

Date	Version	Revision
11/98	1.0	Initial Xilinx release.
01/99	1.2	Updated package drawings and specs.
02/99	1.3	Update of package drawings, updated specifications.
05/99	1.4	Addition of package drawings and specifications.
05/99	1.5	Replaced FG 676 & FG680 package drawings.
07/99	1.6	Changed Boundary Scan Information and changed Figure 11, Boundary Scan Bit Sequence. Updated IOB Input & Output delays. Added Capacitance info for different I/O Standards. Added 5 V tolerant information. Added DLL Parameters and waveforms and new Pin-to-pin Input and Output Parameter tables for Global Clock Input to Output and Setup and Hold. Changed Configuration Information including Figures 12, 14, 17 & 19. Added device-dependent listings for quiescent currents ICCINTQ and ICCOQ. Updated IOB Input and Output Delays based on default standard of LVTTTL, 12 mA, Fast Slew Rate. Added IOB Input Switching Characteristics Standard Adjustments.
09/99	1.7	Speed grade update to preliminary status, Power-on specification and Clock-to-Out Minimums additions, “0” hold time listing explanation, quiescent current listing update, and Figure 6 ADDRA input label correction. Added T <sub>IJITCC</sub> parameter, changed T <sub>OJIT</sub> to T <sub>OPHASE</sub> .
01/00	1.8	Update to speed.txt file 1.96. Corrections for CRs 111036, 111137, 112697, 115479, 117153, 117154, and 117612. Modified notes for Recommended Operating Conditions (voltage and temperature). Changed Bank information for V <sub>CCO</sub> in CS144 package on p.43.



## Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device<sup>(1)</sup> from 0 V. The current is highest at the fastest suggested ramp rate (0 V to nominal voltage in 2 ms) and is lowest at the slowest allowed ramp rate (0 V to nominal voltage in 50 ms). For more details on power supply requirements, see Application Note XAPP158 on [www.xilinx.com](http://www.xilinx.com).

Product	Description <sup>(2)</sup>	Current Requirement <sup>(1,3)</sup>
Virtex Family, Commercial Grade	Minimum required current supply	500 mA
Virtex Family, Industrial Grade	Minimum required current supply	2 A

### Notes:

- Ramp rate used for this specification is from 0 - 2.7 VDC. Peak current occurs on or near the internal power-on reset threshold of 1.0V and lasts for less than 3 ms.
- Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
- Larger currents can result if ramp rates are forced to be faster.

## DC Input and Output Levels

Values for  $V_{IL}$  and  $V_{IH}$  are recommended input voltages. Values for  $I_{OL}$  and  $I_{OH}$  are guaranteed output currents over the recommended operating conditions at the  $V_{OL}$  and  $V_{OH}$  test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum  $V_{CCO}$  for each standard with the respective  $V_{OL}$  and  $V_{OH}$  voltage levels shown. Other standards are sample tested.

Input/Output Standard	$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$	$I_{OH}$
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTL <sup>(1)</sup>	-0.5	0.8	2.0	5.5	0.4	2.4	24	-24
LVC MOS2	-0.5	.7	1.7	5.5	0.4	1.9	12	-12
PCI, 3.3 V	-0.5	44% $V_{CCINT}$	60% $V_{CCINT}$	$V_{CCO} + 0.5$	10% $V_{CCO}$	90% $V_{CCO}$	Note 2	Note 2
PCI, 5.0 V	-0.5	0.8	2.0	5.5	0.55	2.4	Note 2	Note 2
GTL	-0.5	$V_{REF} - 0.05$	$V_{REF} + 0.05$	3.6	0.4	n/a	40	n/a
GTL+	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.6	n/a	36	n/a
HSTL I <sup>(3)</sup>	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	8	-8
HSTL III	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	24	-8
HSTL IV	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	48	-8
SSTL3 I	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.6$	$V_{REF} + 0.6$	8	-8
SSTL3 II	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.8$	$V_{REF} + 0.8$	16	-16
SSTL2 I	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.61$	$V_{REF} + 0.61$	7.6	-7.6
SSTL2 II	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.80$	$V_{REF} + 0.80$	15.2	-15.2
CTT	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
AGP	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	10% $V_{CCO}$	90% $V_{CCO}$	Note 2	Note 2

### Notes:

- $V_{OL}$  and  $V_{OH}$  for lower drive currents are sample tested.
- Tested according to the relevant specifications.
- DC input and output levels for HSTL18 (HSTL I/O standard with  $V_{CCO}$  of 1.8 V) are provided in an HSTL white paper on [www.xilinx.com](http://www.xilinx.com).

## CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Combinatorial Delays						
4-input function: F/G inputs to X/Y outputs	T <sub>ILO</sub>	0.29	0.6	0.7	0.8	ns, max
5-input function: F/G inputs to F5 output	T <sub>IF5</sub>	0.32	0.7	0.8	0.9	ns, max
5-input function: F/G inputs to X output	T <sub>IF5X</sub>	0.36	0.8	0.8	1.0	ns, max
6-input function: F/G inputs to Y output via F6 MUX	T <sub>IF6Y</sub>	0.44	0.9	1.0	1.2	ns, max
6-input function: F5IN input to Y output	T <sub>F5INY</sub>	0.17	0.32	0.36	0.42	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T <sub>IFNCTL</sub>	0.31	0.7	0.7	0.8	ns, max
BY input to YB output	T <sub>BYYB</sub>	0.27	0.53	0.6	0.7	ns, max
Sequential Delays						
FF Clock CLK to XQ/YQ outputs	T <sub>CKO</sub>	0.54	1.1	1.2	1.4	ns, max
Latch Clock CLK to XQ/YQ outputs	T <sub>CKLO</sub>	0.6	1.2	1.4	1.6	ns, max
Setup and Hold Times before/after Clock CLK <sup>(1)</sup>	Setup Time / Hold Time					
4-input function: F/G Inputs	T <sub>ICK</sub> /T <sub>CKI</sub>	0.6 / 0	1.2 / 0	1.4 / 0	1.5 / 0	ns, min
5-input function: F/G inputs	T <sub>IF5CK</sub> /T <sub>CKIF5</sub>	0.7 / 0	1.3 / 0	1.5 / 0	1.7 / 0	ns, min
6-input function: F5IN input	T <sub>F5INCK</sub> /T <sub>CKF5IN</sub>	0.46 / 0	1.0 / 0	1.1 / 0	1.2 / 0	ns, min
6-input function: F/G inputs via F6 MUX	T <sub>IF6CK</sub> /T <sub>CKIF6</sub>	0.8 / 0	1.5 / 0	1.7 / 0	1.9 / 0	ns, min
BX/BY inputs	T <sub>DICK</sub> /T <sub>CKDI</sub>	0.30 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
CE input	T <sub>CECK</sub> /T <sub>CKCE</sub>	0.37 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
SR/BY inputs (synchronous)	T <sub>RCK</sub> T <sub>CKR</sub>	0.33 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T <sub>CH</sub>	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low	T <sub>CL</sub>	0.8	1.5	1.7	2.0	ns, min
Set/Reset						
Minimum Pulse Width, SR/BY inputs	T <sub>RPW</sub>	1.3	2.5	2.8	3.3	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T <sub>RQ</sub>	0.54	1.1	1.3	1.4	ns, max
Delay from GSR to XQ/YQ outputs	T <sub>IOGSRQ</sub>	4.9	9.7	10.9	12.5	ns, max
Toggle Frequency (MHz) (for export control)	F <sub>TOG</sub> (MHz)	625	333	294	250	MHz

### Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

## CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Combinatorial Delays						
F operand inputs to X via XOR	T <sub>OPX</sub>	0.37	0.8	0.9	1.0	ns, max
F operand input to XB output	T <sub>OPXB</sub>	0.54	1.1	1.3	1.4	ns, max
F operand input to Y via XOR	T <sub>OPY</sub>	0.8	1.5	1.7	2.0	ns, max
F operand input to YB output	T <sub>OPYB</sub>	0.8	1.5	1.7	2.0	ns, max
F operand input to COUT output	T <sub>OPCYF</sub>	0.6	1.2	1.3	1.5	ns, max
G operand inputs to Y via XOR	T <sub>OPGY</sub>	0.46	1.0	1.1	1.2	ns, max
G operand input to YB output	T <sub>OPGYB</sub>	0.8	1.6	1.8	2.1	ns, max
G operand input to COUT output	T <sub>OPCYG</sub>	0.7	1.3	1.4	1.6	ns, max
BX initialization input to COUT	T <sub>BXCY</sub>	0.41	0.9	1.0	1.1	ns, max
CIN input to X output via XOR	T <sub>CINX</sub>	0.21	0.41	0.46	0.53	ns, max
CIN input to XB	T <sub>CINXB</sub>	0.02	0.04	0.05	0.06	ns, max
CIN input to Y via XOR	T <sub>CINY</sub>	0.23	0.46	0.52	0.6	ns, max
CIN input to YB	T <sub>CINYB</sub>	0.23	0.45	0.51	0.6	ns, max
CIN input to COUT output	T <sub>BYP</sub>	0.05	0.09	0.10	0.11	ns, max
Multiplier Operation						
F1/2 operand inputs to XB output via AND	T <sub>FANDXB</sub>	0.18	0.36	0.40	0.46	ns, max
F1/2 operand inputs to YB output via AND	T <sub>FANDYB</sub>	0.40	0.8	0.9	1.1	ns, max
F1/2 operand inputs to COUT output via AND	T <sub>FANDCY</sub>	0.22	0.43	0.48	0.6	ns, max
G1/2 operand inputs to YB output via AND	T <sub>GANDYB</sub>	0.25	0.50	0.6	0.7	ns, max
G1/2 operand inputs to COUT output via AND	T <sub>GANDCY</sub>	0.07	0.13	0.15	0.17	ns, max
Setup and Hold Times before/after Clock CLK <sup>(1)</sup>	Setup Time / Hold Time					
CIN input to FFX	T <sub>CCKX</sub> /T <sub>CKCX</sub>	0.50 / 0	1.0 / 0	1.2 / 0	1.3 / 0	ns, min
CIN input to FFY	T <sub>CCKY</sub> /T <sub>CKCY</sub>	0.53 / 0	1.1 / 0	1.2 / 0	1.4 / 0	ns, min

### Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

### Virtex Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

#### Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL

Description	Symbol	Device	Speed Grade				Units
			Min	-6	-5	-4	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, <i>with</i> DLL. For data <i>output</i> with different standards, adjust delays with the values shown in Output Delay Adjustments.	$T_{ICKOFDLL}$	XCV50	1.0	3.1	3.3	3.6	ns, max
		XCV100	1.0	3.1	3.3	3.6	ns, max
		XCV150	1.0	3.1	3.3	3.6	ns, max
		XCV200	1.0	3.1	3.3	3.6	ns, max
		XCV300	1.0	3.1	3.3	3.6	ns, max
		XCV400	1.0	3.1	3.3	3.6	ns, max
		XCV600	1.0	3.1	3.3	3.6	ns, max
		XCV800	1.0	3.1	3.3	3.6	ns, max
		XCV1000	1.0	3.1	3.3	3.6	ns, max

#### Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see [Table 2](#) and [Table 3](#).
3. DLL output jitter is already included in the timing calculation.

#### Global Clock Input-to-Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL

Description	Symbol	Device	Speed Grade				Units
			Min	-6	-5	-4	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, <i>without</i> DLL. For data <i>output</i> with different standards, adjust delays with the values shown in Input and Output Delay Adjustments. For I/O standards requiring $V_{REF}$ such as GTL, GTL+, SSTL, HSTL, CTT, and AGO, an additional 600 ps must be added.	$T_{ICKOF}$	XCV50	1.5	4.6	5.1	5.7	ns, max
		XCV100	1.5	4.6	5.1	5.7	ns, max
		XCV150	1.5	4.7	5.2	5.8	ns, max
		XCV200	1.5	4.7	5.2	5.8	ns, max
		XCV300	1.5	4.7	5.2	5.9	ns, max
		XCV400	1.5	4.8	5.3	6.0	ns, max
		XCV600	1.6	4.9	5.4	6.0	ns, max
		XCV800	1.6	4.9	5.5	6.2	ns, max
		XCV1000	1.7	5.0	5.6	6.3	ns, max

#### Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see [Table 2](#) and [Table 3](#).

## Minimum Clock-to-Out for Virtex Devices

I/O Standard	With DLL	Without DLL									
	All Devices	V50	V100	V150	V200	V300	V400	V600	V800	V1000	Units
*LVTTTL_S2	5.2	6.0	6.0	6.0	6.0	6.1	6.1	6.1	6.1	6.1	ns
*LVTTTL_S4	3.5	4.3	4.3	4.3	4.3	4.4	4.4	4.4	4.4	4.4	ns
*LVTTTL_S6	2.8	3.6	3.6	3.6	3.6	3.7	3.7	3.7	3.7	3.7	ns
*LVTTTL_S8	2.2	3.1	3.1	3.1	3.1	3.1	3.1	3.2	3.2	3.2	ns
*LVTTTL_S12	2.0	2.9	2.9	2.9	2.9	2.9	2.9	3.0	3.0	3.0	ns
*LVTTTL_S16	1.9	2.8	2.8	2.8	2.8	2.8	2.8	2.9	2.9	2.9	ns
*LVTTTL_S24	1.8	2.6	2.6	2.7	2.7	2.7	2.7	2.7	2.7	2.8	ns
*LVTTTL_F2	2.9	3.8	3.8	3.8	3.8	3.8	3.8	3.9	3.9	3.9	ns
*LVTTTL_F4	1.7	2.6	2.6	2.6	2.6	2.6	2.6	2.7	2.7	2.7	ns
*LVTTTL_F6	1.2	2.0	2.0	2.0	2.1	2.1	2.1	2.1	2.1	2.2	ns
*LVTTTL_F8	1.1	1.9	1.9	1.9	1.9	2.0	2.0	2.0	2.0	2.0	ns
*LVTTTL_F12	1.0	1.8	1.8	1.8	1.8	1.9	1.9	1.9	1.9	1.9	ns
*LVTTTL_F16	0.9	1.7	1.8	1.8	1.8	1.8	1.8	1.8	1.9	1.9	ns
*LVTTTL_F24	0.9	1.7	1.7	1.7	1.8	1.8	1.8	1.8	1.8	1.9	ns
LVCMS2	1.1	1.9	1.9	1.9	2.0	2.0	2.0	2.0	2.0	2.1	ns
PCI33_3	1.5	2.4	2.4	2.4	2.4	2.4	2.4	2.5	2.5	2.5	ns
PCI33_5	1.4	2.2	2.2	2.3	2.3	2.3	2.3	2.3	2.3	2.4	ns
PCI66_3	1.1	1.9	1.9	2.0	2.0	2.0	2.0	2.0	2.1	2.1	ns
GTL	1.6	2.5	2.5	2.5	2.5	2.5	2.5	2.6	2.6	2.6	ns
GTL+	1.7	2.5	2.5	2.6	2.6	2.6	2.6	2.6	2.6	2.7	ns
HSTL I	1.1	1.9	1.9	1.9	1.9	2.0	2.0	2.0	2.0	2.0	ns
HSTL III	0.9	1.7	1.7	1.8	1.8	1.8	1.8	1.8	1.8	1.9	ns
HSTL IV	0.8	1.6	1.6	1.6	1.7	1.7	1.7	1.7	1.7	1.8	ns
SSTL2 I	0.9	1.7	1.7	1.7	1.7	1.8	1.8	1.8	1.8	1.8	ns
SSTL2 II	0.8	1.6	1.6	1.6	1.6	1.7	1.7	1.7	1.7	1.7	ns
SSTL3 I	0.8	1.6	1.7	1.7	1.7	1.7	1.7	1.7	1.8	1.8	ns
SSTL3 II	0.7	1.5	1.5	1.6	1.6	1.6	1.6	1.6	1.6	1.7	ns
CTT	1.0	1.8	1.8	1.8	1.9	1.9	1.9	1.9	1.9	2.0	ns
AGP	1.0	1.8	1.8	1.9	1.9	1.9	1.9	1.9	1.9	2.0	ns

\*S = Slow Slew Rate, F = Fast Slew Rate

### Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Input and output timing is measured at 1.4 V for LVTTTL. For other I/O standards, see [Table 3](#). In all cases, an 8 pF external capacitive load is used.

## Global Clock Set-Up and Hold for LVTTL Standard, *without* DLL

Description	Symbol	Device	Speed Grade				Units
			Min	-6	-5	-4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. <sup>(2)</sup> For data input with different standards, adjust the setup time delay by the values shown in Input Delay Adjustments.							
Full Delay Global Clock and IFF, without DLL	T <sub>PSFD</sub> /T <sub>PHFD</sub>	XCV50	0.6 / 0	2.3 / 0	2.6 / 0	2.9 / 0	ns, min
		XCV100	0.6 / 0	2.3 / 0	2.6 / 0	3.0 / 0	ns, min
		XCV150	0.6 / 0	2.4 / 0	2.7 / 0	3.1 / 0	ns, min
		XCV200	0.7 / 0	2.5 / 0	2.8 / 0	3.2 / 0	ns, min
		XCV300	0.7 / 0	2.5 / 0	2.8 / 0	3.2 / 0	ns, min
		XCV400	0.7 / 0	2.6 / 0	2.9 / 0	3.3 / 0	ns, min
		XCV600	0.7 / 0	2.6 / 0	2.9 / 0	3.3 / 0	ns, min
		XCV800	0.7 / 0	2.7 / 0	3.1 / 0	3.5 / 0	ns, min
		XCV1000	0.7 / 0	2.8 / 0	3.1 / 0	3.6 / 0	ns, min

IFF = Input Flip-Flop or Latch

**Notes: Notes:**

1. Set-up time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
2. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

### DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Description	Symbol	Speed Grade						Units
		-6		-5		-4		
		Min	Max	Min	Max	Min	Max	
Input Clock Frequency (CLKDLLHF)	FCLKINHF	60	200	60	180	60	180	MHz
Input Clock Frequency (CLKDLL)	FCLKINLF	25	100	25	90	25	90	MHz
Input Clock Pulse Width (CLKDLLHF)	T <sub>DLLPWHF</sub>	2.0	-	2.4	-	2.4	-	ns
Input Clock Pulse Width (CLKDLL)	T <sub>DLLPWLF</sub>	2.5	-	3.0		3.0	-	ns

#### Notes:

1. All specifications correspond to Commercial Operating Temperatures (0°C to +85°C).

### DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

Description	Symbol	F <sub>CLKIN</sub>	CLKDLLHF		CLKDLL		Units
			Min	Max	Min	Max	
Input Clock Period Tolerance	T <sub>IP</sub> TOL		-	1.0	-	1.0	ns
Input Clock Jitter Tolerance (Cycle to Cycle)	T <sub>IJ</sub> TCC		-	± 150	-	± 300	ps
Time Required for DLL to Acquire Lock	T <sub>LOCK</sub>	> 60 MHz	-	20	-	20	μs
		50 - 60 MHz	-	-	-	25	μs
		40 - 50 MHz	-	-	-	50	μs
		30 - 40 MHz	-	-	-	90	μs
		25 - 30 MHz	-	-	-	120	μs
Output Jitter (cycle-to-cycle) for any DLL Clock Output <sup>(1)</sup>	T <sub>OJ</sub> TCC			± 60		± 60	ps
Phase Offset between CLKIN and CLKO <sup>(2)</sup>	T <sub>PHIO</sub>			± 100		± 100	ps
Phase Offset between Clock Outputs on the DLL <sup>(3)</sup>	T <sub>PHOO</sub>			± 140		± 140	ps
Maximum Phase Difference between CLKIN and CLKO <sup>(4)</sup>	T <sub>PHIOM</sub>			± 160		± 160	ps
Maximum Phase Difference between Clock Outputs on the DLL <sup>(5)</sup>	T <sub>PHOOM</sub>			± 200		± 200	ps

#### Notes:

1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* Output Jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN and CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of Output Jitter and Phase Offset between any two DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).
6. All specifications correspond to Commercial Operating Temperatures (0°C to +85°C).





Table 4: Virtex Pinout Tables (Fine-Pitch BGA) (Continued)

Pin Name	Device	FG256	FG456	FG676	FG680
<b>V<sub>REF</sub> Bank 7</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	C1, H3	N/A	N/A	N/A
	XCV100/150	... + D1	E2, H4, K3	N/A	N/A
	XCV200/300	... + B1	... + D2	N/A	N/A
	XCV400	N/A	N/A	F4, G4, K6, M2, M5	N/A
	XCV600	N/A	N/A	... + H1	E38, G38, L36, N36, U36, U38
	XCV800	N/A	N/A	... + K1	... + N38
	XCV1000	N/A	N/A	N/A	... + F36
GND	All	A1, A16, B2, B15, F6, F7, F10, F11, G6, G7, G8, G9, G10, G11, H7, H8, H9, H10, J7, J8, J9, J10, K6, K7, K8, K9, K10, K11, L6, L7, L10, L11, R2, R15, T1, T16	A1, A22, B2, B21, C3, C20, J9, J10, J11, J12, J13, J14, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N9, N10, N11, N12, N13, N14, P9, P10, P11, P12, P13, P14, Y3, Y20, AA2, AA21, AB1, AB22	A1, A26, B2, B9, B14, B18, B25, C3, C24, D4, D23, E5, E22, J2, J25, K10, K11, K12, K13, K14, K15, K16, K17, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N2, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, P25, R10, R11, R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17, V2, V25, AB5, AB22, AC4, AC23, AD3, AD24, AE2, AE9, AE13, AE18, AE25, AF1, AF26	A1, A2, A3, A37, A38, A39, AA5, AA35, AH4, AH5, AH35, AH36, AR5, AR12, AR19, AR20, AR21, AR28, AR35, AT4, AT12, AT20, AT28, AT36, AU1, AU3, AU20, AU37, AU39, AV1, AV2, AV38, AV39, AW1, AW2, AW3, AW37, AW38, AW39, B1, B2, B38, B39, C1, C3, C20, C37, C39, D4, D12, D20, D28, D36, E5, E12, E19, E20, E21, E28, E35, M4, M5, M35, M36, W5, W35, Y3, Y4, Y5, Y35, Y36, Y37

## Pinout Diagrams

The following diagrams, **CS144 Pin Function Diagram**, page 17 through **FG680 Pin Function Diagram**, page 27, illustrate the locations of special-purpose pins on Virtex FPGAs. Table 5 lists the symbols used in these diagrams. The diagrams also show I/O-bank boundaries.

Table 5: Pinout Diagram Symbols

Symbol	Pin Function
*	General I/O
*	Device-dependent general I/O, n/c on smaller devices
V	V <sub>CCINT</sub>
v	Device-dependent V <sub>CCINT</sub> , n/c on smaller devices
O	V <sub>CCO</sub>
R	V <sub>REF</sub>
r	Device-dependent V <sub>REF</sub> , remains I/O on smaller devices
G	Ground
Ø, 1, 2, 3	Global Clocks

Table 5: Pinout Diagram Symbols (Continued)

Symbol	Pin Function
⑩, ①, ②	M0, M1, M2
⑩, ①, ②, ③, ④, ⑤, ⑥, ⑦	D0/DIN, D1, D2, D3, D4, D5, D6, D7
B	DOUT/BUSY
D	DONE
P	PROGRAM
I	INIT
K	CCLK
W	WRITE
S	CS
T	Boundary-scan Test Access Port
+	Temperature diode, anode
–	Temperature diode, cathode
n	No connect

## CS144 Pin Function Diagram

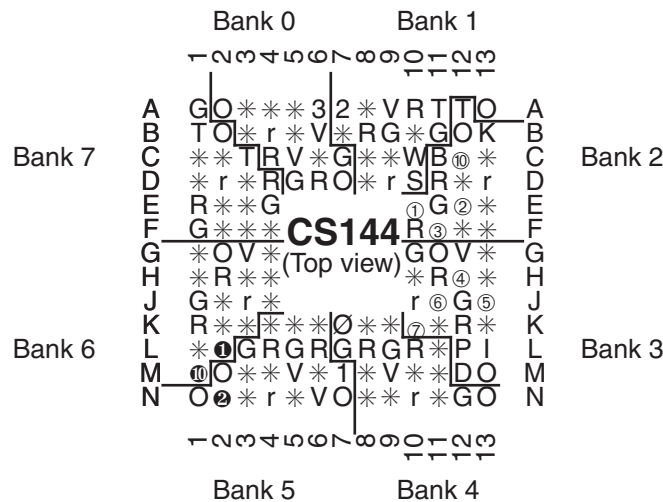


Figure 1: CS144 Pin Function Diagram

## TQ144 Pin Function Diagram

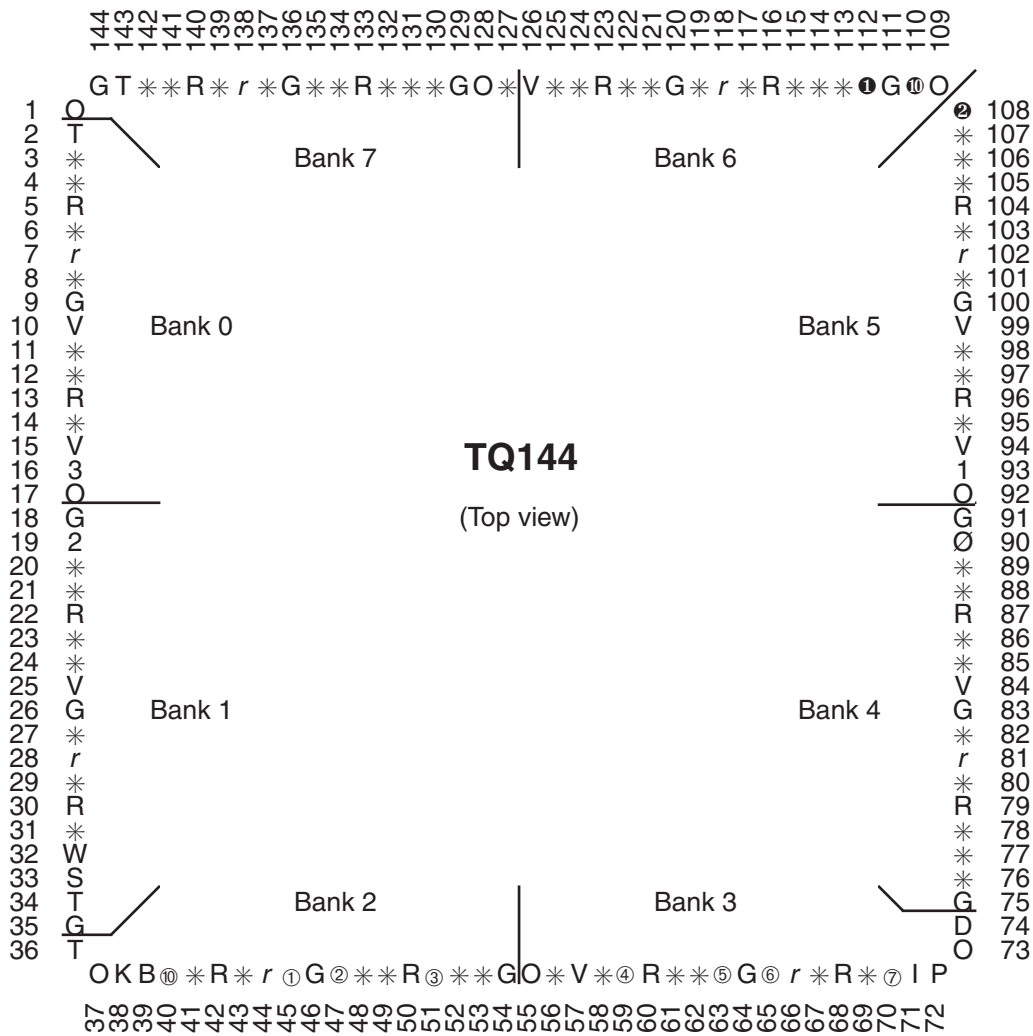
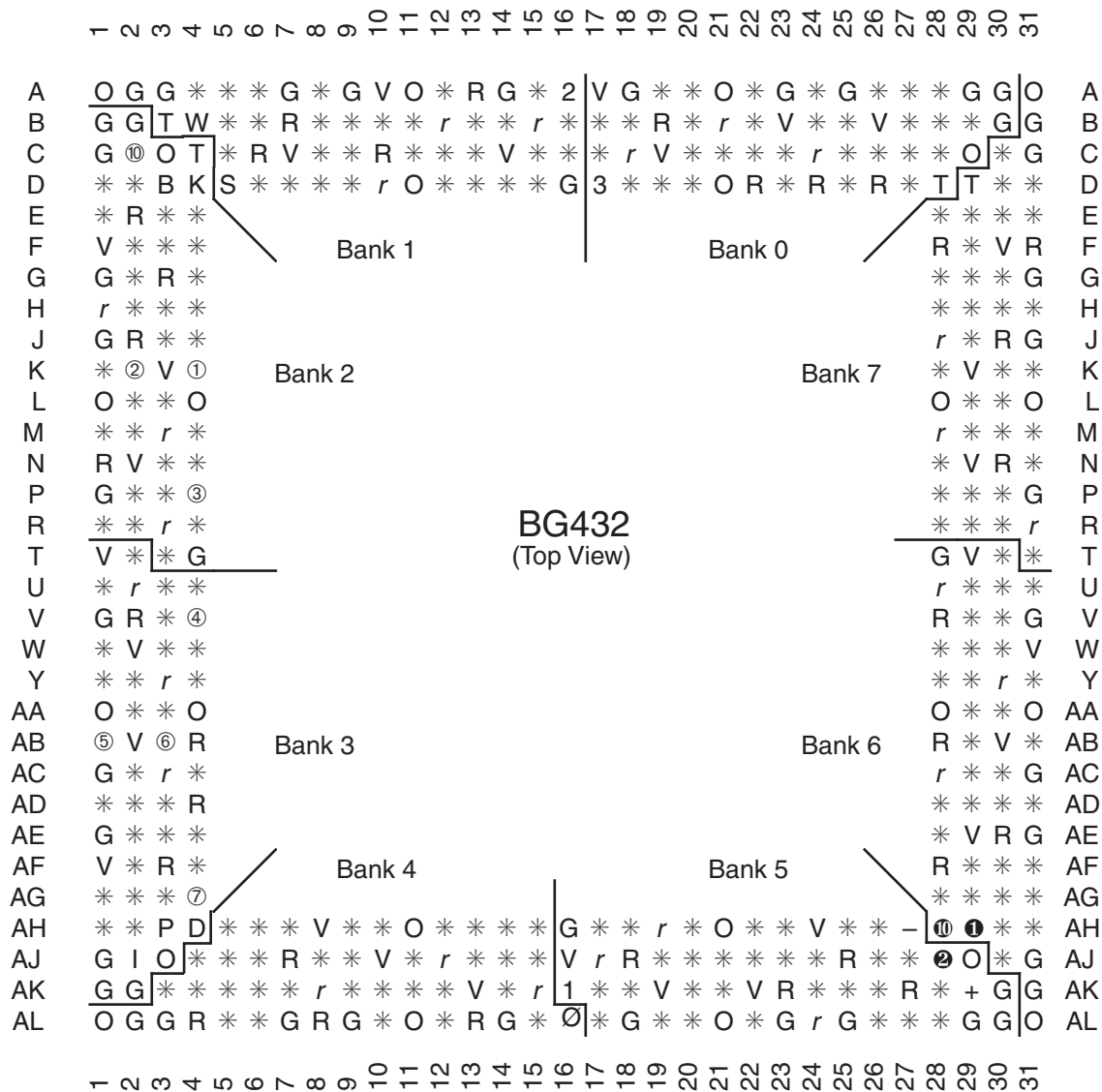


Figure 2: TQ144 Pin Function Diagram

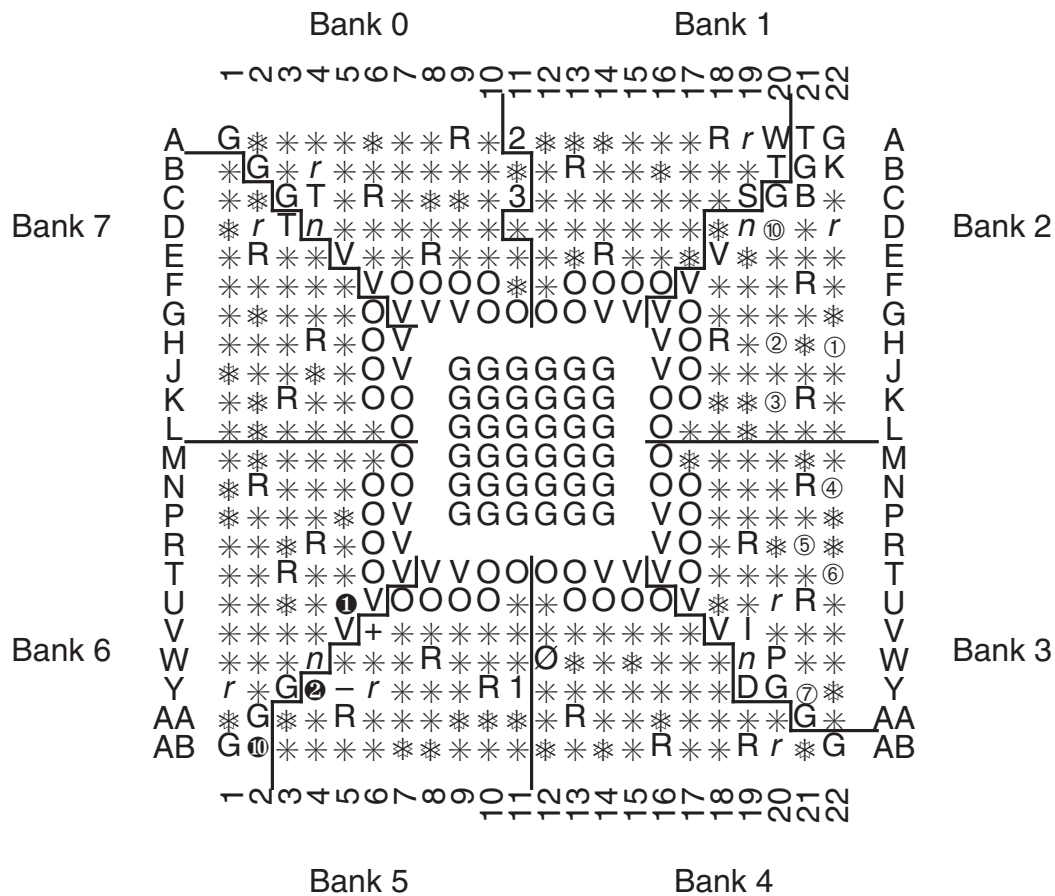
## BG432 Pin Function Diagram



DS003\_21\_100300

Figure 6: BG432 Pin Function Diagram

## FG456 Pin Function Diagram



### FG456 (Top view)

Figure 9: FG456 Pin Function Diagram

#### Notes:

Packages FG456 and FG676 are layout compatible.