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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	4704
Number of Logic Elements/Cells	21168
Total RAM Bits	114688
Number of I/O	166
Number of Gates	888439
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv800-4hq240i

Virtex™ 2.5 V
Field Programmable Gate Arrays

DS003-2 (v4.0) March 1, 2013   **Product Specification**

Architectural Description

Virtex Array

The Virtex user-programmable gate array, shown in Figure 1, comprises two major configurable elements: configurable logic blocks (CLBs) and input/output blocks (IOBs).

- CLBs provide the functional elements for constructing logic
- IOBs provide the interface between the package pins and the CLBs

CLBs interconnect through a general routing matrix (GRM). The GRM comprises an array of routing switches located at the intersections of horizontal and vertical routing channels. Each CLB nests into a VersaBlock™ that also provides local routing resources to connect the CLB to the GRM.

The VersaRing™ I/O interface provides additional routing resources around the periphery of the device. This routing improves I/O routability and facilitates pin locking.

The Virtex architecture also includes the following circuits that connect to the GRM.

- Dedicated block memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- 3-State buffers (BUFTs) associated with each CLB that drive dedicated segmentable horizontal routing resources

Values stored in static memory cells control the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

Input/Output Block

The Virtex IOB, Figure 2, features SelectIO™ inputs and outputs that support a wide variety of I/O signalling standards, see Table 1.

The three IOB storage elements function either as edge-triggered D-type flip-flops or as level sensitive latches. Each IOB has a clock signal (CLK) shared by the three flip-flops and independent clock enable signals for each flip-flop.

In addition to the CLK and CE control signals, the three flip-flops share a Set/Reset (SR). For each flip-flop, this signal can be independently configured as a synchronous Set, a synchronous Reset, an asynchronous Preset, or an asynchronous Clear.

The output buffer and all of the IOB control signals have independent polarity controls.
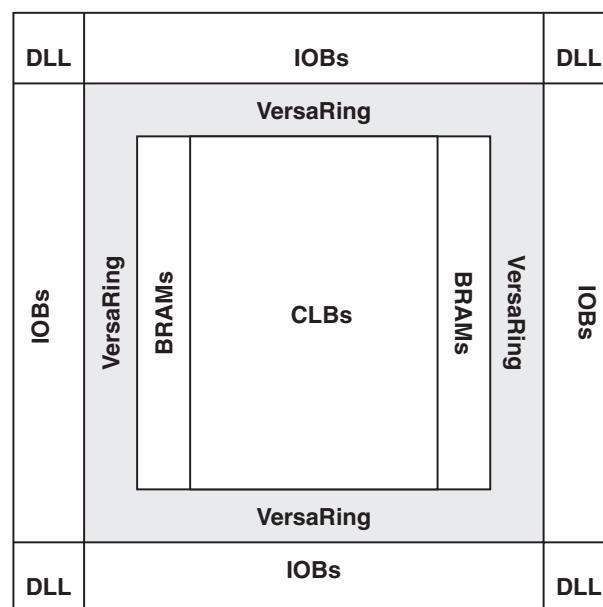
vao_b.eps

Figure 1: **Virtex Architecture Overview**

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Two forms of over-voltage protection are provided, one that permits 5 V compliance, and one that does not. For 5 V compliance, a Zener-like structure connected to ground turns on when the output rises to approximately 6.5 V. When PCI 3.3 V compliance is required, a conventional clamp diode is connected to the output supply voltage, V_{CCO}.

Optional pull-up and pull-down resistors and an optional weak-keeper circuit are attached to each pad. Prior to configuration, all pins not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but inputs can optionally be pulled up.

The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins will float. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All Virtex IOBs support IEEE 1149.1-compatible boundary scan testing.

Input Path

A buffer In the Virtex IOB input path routes the input signal either directly to internal logic or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signalling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can used in close proximity to each other. See **I/O Banking**, page 3.

There are optional pull-up and pull-down resistors at each user I/O input for use after configuration. Their value is in the range 50 kΩ – 100 kΩ.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signalling standards. Each output buffer can source up to 24 mA and sink up to 48mA. Drive strength and slew rate controls minimize bus transients.

In most signalling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See **I/O Banking**, page 3.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signalling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages externally and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks, as shown in Figure 3. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.
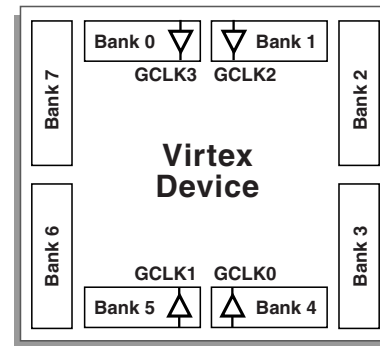
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Figure 3: **Virtex I/O Banks**

Within a bank, output standards can be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 2. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}.

Table 2: **Compatible Output Standards**

V_{CCO}	Compatible Standards
3.3 V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+
2.5 V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+
1.5 V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, V_{REF}. In this case, certain user-I/O pins are automatically configured as inputs for the V_{REF} voltage. Approximately one in six of the I/O pins in the bank assume this role.

The V_{REF} pins within a bank are interconnected internally and consequently only one V_{REF} voltage can be used within each bank. All V_{REF} pins in the bank, however, must be connected to the external voltage source for correct operation.

Within a bank, inputs that require V_{REF} can be mixed with those that do not. However, only one V_{REF} voltage can be used within a bank. Input buffers that use V_{REF} are not 5 V tolerant. LVTTL, LVCMOS2, and PCI 33 MHz 5 V, are 5 V tolerant.

The V_{CCO} and V_{REF} pins for each bank appear in the device Pinout tables and diagrams. The diagrams also show the bank affiliation of each I/O.

Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices,

ers with a common user interface regardless of their choice of entry and verification tools. The XDM software simplifies the selection of implementation options with pull-down menus and on-line help.

Application programs ranging from schematic capture to Placement and Routing (PAR) can be accessed through the XDM software. The program command sequence is generated prior to execution, and stored for documentation.

Several advanced software features facilitate Virtex design. RPMs, for example, are schematic-based macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the Xilinx FPGA Foundation development system provides interfaces to the following synthesis design environments.

*   Synopsys (FPGA Compiler, FPGA Express)
*   Exemplar (Spectrum)
*   Synplicity (Synplify)

For schematic design entry, the Xilinx FPGA Foundation and alliance development system provides interfaces to the following schematic-capture design environments.

*   Mentor Graphics V8 (Design Architect, QuickSim II)
*   Viewlogic Systems (Viewdraw)

Third-party vendors support many other environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Virtex FPGAs supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The "soft macro" portion of the library contains detailed descriptions of common logic functions, but does not contain any partitioning or placement information. The performance of these macros depends, therefore, on the partitioning and placement obtained during implementation.

RPMs, on the other hand, do contain predetermined partitioning and placement information that permits optimal implementation of these functions. Users can create their own library of soft macros or RPMs based on the macros and primitives in the standard library.

The design environment supports hierarchical design entry, with high-level schematics that comprise major functional blocks, while lower-level schematics define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical

design, thus allowing the most convenient entry method to be used for each portion of the design.

Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF net list for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floor planning.

The implementation software incorporates Timing Wizard® timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered on a schematic in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the net list for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the TRACE® static timing analyzer.

For in-circuit debugging, the development system includes a download and readback cable. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

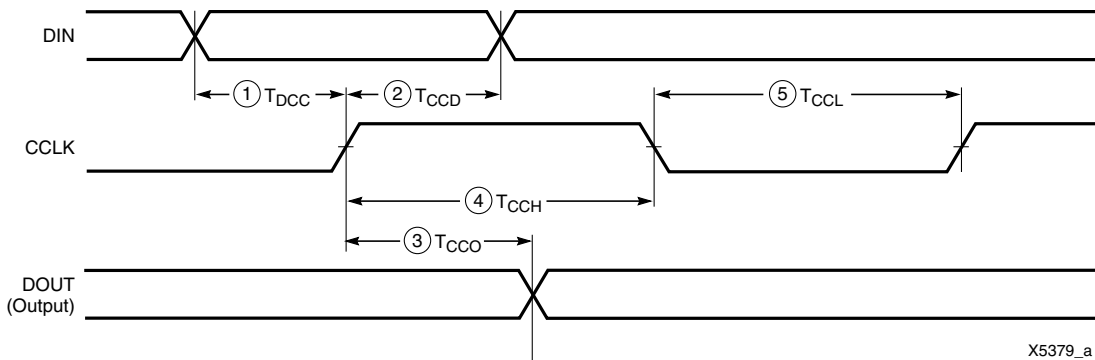*Table 8:* **Master/Slave Serial Mode Programming Switching**

	Description	Figure References	Symbol	Values	Units
CCLK	DIN setup/hold, slave mode	1/2	T_{DCC}/T_{CCD}	5.0 / 0	ns, min
	DIN setup/hold, master mode	1/2	T_{DSCK}/T_{CKDS}	5.0 / 0	ns, min
	DOUT	3	T_{CCO}	12.0	ns, max
	High time	4	T_{CCH}	5.0	ns, min
	Low time	5	T_{CCL}	5.0	ns, min
	Maximum Frequency		F_{CC}	66	MHz, max
	Frequency Tolerance, master mode with respect to nominal			+45% −30%	
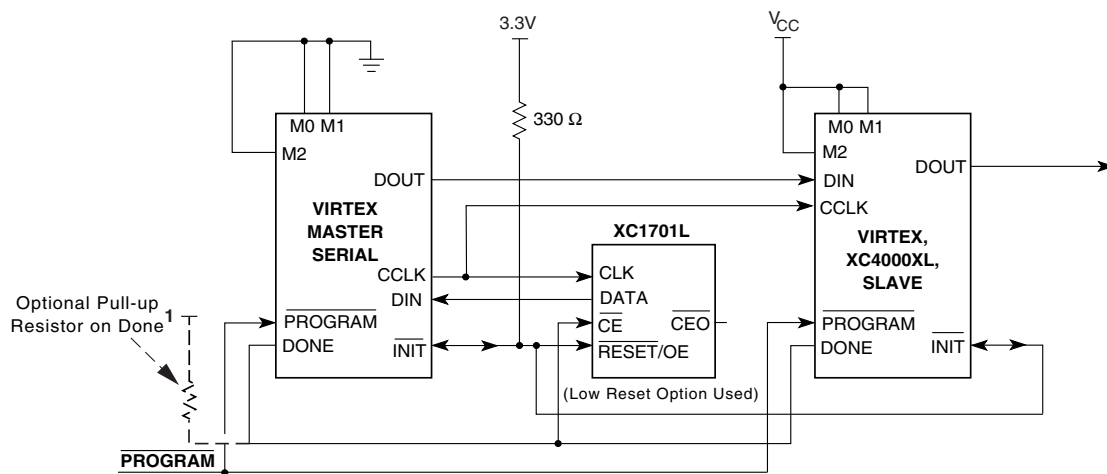
Note 1: If none of the Virtex FPGAs have been selected to drive DONE, an external pull-up resistor of 330 Ω should be added to the common DONE line. (For Spartan-XL devices, add a 4.7K Ω pull-up resistor.) This pull-up is not needed if the DriveDONE attribute is set. If used, DriveDONE should be selected only for the last device in the configuration chain.

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Figure 12: **Master/Slave Serial Mode Circuit Diagram**

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Figure 13: **Slave-Serial Mode Programming Switching Characteristics**

Date	Version	Revision
01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
03/00	2.0	New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration.
05/00	2.1	Modified "Pins not listed..." statement. Speed grade update to Final status.
05/00	2.2	Modified Table 18.
09/00	2.3	• Added XCV400 values to table under **Minimum Clock-to-Out for Virtex Devices**. • Corrected Units column in table under **IOB Input Switching Characteristics**. • Added values to table under **CLB SelectRAM Switching Characteristics**.
10/00	2.4	• Corrected Pinout information for devices in the BG256, BG432, and BG560 packages in Table 18. • Corrected **BG256 Pin Function Diagram**.
04/01	2.5	• Revised minimums for **Global Clock Set-Up and Hold for LVTTL Standard, with DLL**. • Updated SelectMAP Write Timing Characteristics values in Table 9. • Converted file to modularized format. See the **Virtex Data Sheet** section.
07/19/01	2.6	• Made minor edits to text under **Configuration**.
07/19/02	2.7	• Made minor edit to Figure 16 and Figure 18.
09/10/02	2.8	• Added clarifications in the **Configuration**, **Boundary-Scan Mode**, and **Block SelectRAM** sections. Revised Figure 17.
12/09/02	2.8.1	• Added clarification in the **Boundary Scan** section. • Corrected number of buffered Hex lines listed in **General Purpose Routing** section.
03/01/13	4.0	The products listed in this data sheet are obsolete. See **XCN10016** for further information.

Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

- DS003-1, Virtex 2.5V FPGAs:
  Introduction and Ordering Information (Module 1)

- DS003-2, Virtex 2.5V FPGAs:
  Functional Description (Module 2)

- DS003-3, Virtex 2.5V FPGAs:
  DC and Switching Characteristics (Module 3)

- DS003-4, Virtex 2.5V FPGAs:
  Pinout Tables (Module 4)

DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Device	Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage (below which configuration data can be lost)		All	2.0		V
V_{DRIO}	Data Retention V_{CCO} Voltage (below which configuration data can be lost)		All	1.2		V
I_{CCINTQ}	Quiescent V_{CCINT} supply current[1,3]		XCV50		50	mA
			XCV100		50	mA
			XCV150		50	mA
			XCV200		75	mA
			XCV300		75	mA
			XCV400		75	mA
			XCV600		100	mA
			XCV800		100	mA
			XCV1000		100	mA
I_{CCOQ}	Quiescent V_{CCO} supply current[1]		XCV50		2	mA
			XCV100		2	mA
			XCV150		2	mA
			XCV200		2	mA
			XCV300		2	mA
			XCV400		2	mA
			XCV600		2	mA
			XCV800		2	mA
			XCV1000		2	mA
I_{REF}	V_{REF} current per V_{REF} pin		All		20	µA
I_L	Input or output leakage current		All	−10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, PQ, HQ, packages	All		8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V, V_{CCO} = 3.3 V (sample tested)		All	Note (2)	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)			Note (2)	0.15	mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.
3. Multiply I_{CCINTQ} limit by two for industrial grade.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device[1] from 0 V. The current is highest at the fastest suggested ramp rate (0 V to nominal voltage in 2 ms) and is lowest at the slowest allowed ramp rate (0 V to nominal voltage in 50 ms). For more details on power supply requirements, see Application Note XAPP158 on **www.xilinx.com**.

Product	Description[2]	Current Requirement[1,3]
Virtex Family, Commercial Grade	Minimum required current supply	500 mA
Virtex Family, Industrial Grade	Minimum required current supply	2 A

Notes:
1. Ramp rate used for this specification is from 0 - 2.7 VDC. Peak current occurs on or near the internal power-on reset threshold of 1.0V and lasts for less than 3 ms.
2. Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
3. Larger currents can result if ramp rates are forced to be faster.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed output currents over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} for each standard with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTL[1]	-0.5	0.8	2.0	5.5	0.4	2.4	24	-24
LVCMOS2	-0.5	.7	1.7	5.5	0.4	1.9	12	-12
PCI, 3.3 V	-0.5	44% V_{CCINT}	60% V_{CCINT}	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI, 5.0 V	-0.5	0.8	2.0	5.5	0.55	2.4	Note 2	Note 2
GTL	-0.5	$V_{REF} - 0.05$	$V_{REF} + 0.05$	3.6	0.4	n/a	40	n/a
GTL+	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.6	n/a	36	n/a
HSTL I[3]	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	8	-8
HSTL III	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	24	-8
HSTL IV	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	48	-8
SSTL3 I	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.6$	$V_{REF} + 0.6$	8	-8
SSTL3 II	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.8$	$V_{REF} + 0.8$	16	-16
SSTL2 I	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.61$	$V_{REF} + 0.61$	7.6	-7.6
SSTL2 II	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.80$	$V_{REF} + 0.80$	15.2	-15.2
CTT	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
AGP	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested.
2. Tested according to the relevant specifications.
3. DC input and output levels for HSTL18 (HSTL I/O standard with V_{CCO} of 1.8 V) are provided in an HSTL white paper on **www.xilinx.com**.

Virtex Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Virtex devices unless otherwise noted.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in , page 6.

Description	Device	Symbol	Min	-6	-5	-4	Units
				Speed Grade			
Propagation Delays							
Pad to I output, no delay	All	T_{IOPI}	0.39	0.8	0.9	1.0	ns, max
Pad to I output, with delay	XCV50	T_{IOPID}	0.8	1.5	1.7	1.9	ns, max
	XCV100		0.8	1.5	1.7	1.9	ns, max
	XCV150		0.8	1.5	1.7	1.9	ns, max
	XCV200		0.8	1.5	1.7	1.9	ns, max
	XCV300		0.8	1.5	1.7	1.9	ns, max
	XCV400		0.9	1.8	2.0	2.3	ns, max
	XCV600		0.9	1.8	2.0	2.3	ns, max
	XCV800		1.1	2.1	2.4	2.7	ns, max
	XCV1000		1.1	2.1	2.4	2.7	ns, max
Pad to output IQ via transparent latch, no delay	All	T_{IOPLI}	0.8	1.6	1.8	2.0	ns, max
Pad to output IQ via transparent latch, with delay	XCV50	T_{IOPLID}	1.9	3.7	4.2	4.8	ns, max
	XCV100		1.9	3.7	4.2	4.8	ns, max
	XCV150		2.0	3.9	4.3	4.9	ns, max
	XCV200		2.0	4.0	4.4	5.1	ns, max
	XCV300		2.0	4.0	4.4	5.1	ns, max
	XCV400		2.1	4.1	4.6	5.3	ns, max
	XCV600		2.1	4.2	4.7	5.4	ns, max
	XCV800		2.2	4.4	4.9	5.6	ns, max
	XCV1000		2.3	4.5	5.1	5.8	ns, max
Sequential Delays							
Clock CLK	All						
Minimum Pulse Width, High		T_{CH}	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low		T_{CL}	0.8	1.5	1.7	2.0	ns, min
Clock CLK to output IQ		T_{IOCKIQ}	0.2	0.7	0.7	0.8	ns, max

| Description | Device | Symbol | Speed Grade | | | | Units |
			Min	-6	-5	-4	
Setup and Hold Times with respect to Clock CLK at IOB input register[1]			**Setup Time / Hold Time**				
Pad, no delay	All	T_{IOPICK}/T_{IOICKP}	0.8 / 0	1.6 / 0	1.8 / 0	2.0 / 0	ns, min
Pad, with delay	XCV50	$T_{IOPICKD}/T_{IOICKPD}$	1.9 / 0	3.7 / 0	4.1 / 0	4.7 / 0	ns, min
	XCV100		1.9 / 0	3.7 / 0	4.1 / 0	4.7 / 0	ns, min
	XCV150		1.9 / 0	3.8 / 0	4.3 / 0	4.9 / 0	ns, min
	XCV200		2.0 / 0	3.9 / 0	4.4 / 0	5.0 / 0	ns, min
	XCV300		2.0 / 0	3.9 / 0	4.4 / 0	5.0 / 0	ns, min
	XCV400		2.1 / 0	4.1 / 0	4.6 / 0	5.3 / 0	ns, min
	XCV600		2.1 / 0	4.2 / 0	4.7 / 0	5.4 / 0	ns, min
	XCV800		2.2 / 0	4.4 / 0	4.9 / 0	5.6 / 0	ns, min
	XCV1000		2.3 / 0	4.5 / 0	5.0 / 0	5.8 / 0	ns, min
ICE input	All	$T_{IOICECK}/T_{IOCKICE}$	0.37/ 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, max
Set/Reset Delays							
SR input (IFF, synchronous)	All	$T_{IOSRCKI}$	0.49	1.0	1.1	1.3	ns, max
SR input to IQ (asynchronous)	All	T_{IOSRIQ}	0.70	1.4	1.6	1.8	ns, max
GSR to output IQ	All	T_{GSRQ}	4.9	9.7	10.9	12.5	ns, max

Notes:
1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see Table 3.

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Description	Symbol	Standard[1]	Speed Grade				Units
			Min	-6	-5	-4	
Output Delay Adjustments							
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T_{OLVTTL_S2}	LVTTL, Slow, 2 mA	4.2	14.7	15.8	17.0	ns
	T_{OLVTTL_S4}	4 mA	2.5	7.5	8.0	8.6	ns
	T_{OLVTTL_S6}	6 mA	1.8	4.8	5.1	5.6	ns
	T_{OLVTTL_S8}	8 mA	1.2	3.0	3.3	3.5	ns
	T_{OLVTTL_S12}	12 mA	1.0	1.9	2.1	2.2	ns
	T_{OLVTTL_S16}	16 mA	0.9	1.7	1.9	2.0	ns
	T_{OLVTTL_S24}	24 mA	0.8	1.3	1.4	1.6	ns
	T_{OLVTTL_F2}	LVTTL, Fast, 2mA	1.9	13.1	14.0	15.1	ns
	T_{OLVTTL_F4}	4 mA	0.7	5.3	5.7	6.1	ns
	T_{OLVTTL_F6}	6 mA	0.2	3.1	3.3	3.6	ns
	T_{OLVTTL_F8}	8 mA	0.1	1.0	1.1	1.2	ns
	T_{OLVTTL_F12}	12 mA	0	0	0	0	ns
	T_{OLVTTL_F16}	16 mA	−0.10	−0.05	−0.05	−0.05	ns
	T_{OLVTTL_F24}	24 mA	−0.10	−0.20	−0.21	−0.23	ns
	$T_{OLVCMOS2}$	LVCMOS2	0.10	0.10	0.11	0.12	ns
	T_{OPCI33_3}	PCI, 33 MHz, 3.3 V	0.50	2.3	2.5	2.7	ns
	T_{OPCI33_5}	PCI, 33 MHz, 5.0 V	0.40	2.8	3.0	3.3	ns
	T_{OPCI66_3}	PCI, 66 MHz, 3.3 V	0.10	−0.40	−0.42	−0.46	ns
	T_{OGTL}	GTL	0.6	0.50	0.54	0.6	ns
	T_{OGTLP}	GTL+	0.7	0.8	0.9	1.0	ns
	T_{OHSTL_I}	HSTL I	0.10	−0.50	−0.53	−0.5	ns
	T_{OHSTL_III}	HSTL III	−0.10	−0.9	−0.9	−1.0	ns
	T_{OHSTL_IV}	HSTL IV	−0.20	−1.0	−1.0	−1.1	ns
	T_{OSSTL2_I}	SSTL2 I	−0.10	−0.50	−0.53	−0.5	ns
	T_{OSSLT2_II}	SSTL2 II	−0.20	−0.9	−0.9	−1.0	ns
	T_{OSSTL3_I}	SSTL3 I	−0.20	−0.50	−0.53	−0.5	ns
	T_{OSSTL3_II}	SSTL3 II	−0.30	−1.0	−1.0	−1.1	ns
	T_{OCTT}	CTT	0	−0.6	−0.6	−0.6	ns
	T_{OAGP}	AGP	0	−0.9	−0.9	−1.0	ns

Notes:
1. Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see Table 2 and Table 3.

CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

Description	Symbol	Min	-6	-5	-4	Units
Combinatorial Delays						
F operand inputs to X via XOR	T_{OPX}	0.37	0.8	0.9	1.0	ns, max
F operand input to XB output	T_{OPXB}	0.54	1.1	1.3	1.4	ns, max
F operand input to Y via XOR	T_{OPY}	0.8	1.5	1.7	2.0	ns, max
F operand input to YB output	T_{OPYB}	0.8	1.5	1.7	2.0	ns, max
F operand input to COUT output	T_{OPCYF}	0.6	1.2	1.3	1.5	ns, max
G operand inputs to Y via XOR	T_{OPGY}	0.46	1.0	1.1	1.2	ns, max
G operand input to YB output	T_{OPGYB}	0.8	1.6	1.8	2.1	ns, max
G operand input to COUT output	T_{OPCYG}	0.7	1.3	1.4	1.6	ns, max
BX initialization input to COUT	T_{BXCY}	0.41	0.9	1.0	1.1	ns, max
CIN input to X output via XOR	T_{CINX}	0.21	0.41	0.46	0.53	ns, max
CIN input to XB	T_{CINXB}	0.02	0.04	0.05	0.06	ns, max
CIN input to Y via XOR	T_{CINY}	0.23	0.46	0.52	0.6	ns, max
CIN input to YB	T_{CINYB}	0.23	0.45	0.51	0.6	ns, max
CIN input to COUT output	T_{BYP}	0.05	0.09	0.10	0.11	ns, max
Multiplier Operation						
F1/2 operand inputs to XB output via AND	T_{FANDXB}	0.18	0.36	0.40	0.46	ns, max
F1/2 operand inputs to YB output via AND	T_{FANDYB}	0.40	0.8	0.9	1.1	ns, max
F1/2 operand inputs to COUT output via AND	T_{FANDCY}	0.22	0.43	0.48	0.6	ns, max
G1/2 operand inputs to YB output via AND	T_{GANDYB}	0.25	0.50	0.6	0.7	ns, max
G1/2 operand inputs to COUT output via AND	T_{GANDCY}	0.07	0.13	0.15	0.17	ns, max
Setup and Hold Times before/after Clock CLK[1]	Setup Time / Hold Time					
CIN input to FFX	T_{CCKX}/T_{CKCX}	0.50 / 0	1.0 / 0	1.2 / 0	1.3 / 0	ns, min
CIN input to FFY	T_{CCKY}/T_{CKCY}	0.53 / 0	1.1 / 0	1.2 / 0	1.4 / 0	ns, min

Notes:
1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Minimum Clock-to-Out for Virtex Devices

I/O Standard	With DLL All Devices	Without DLL									Units
		V50	V100	V150	V200	V300	V400	V600	V800	V1000	
*LVTTL_S2	5.2	6.0	6.0	6.0	6.0	6.1	6.1	6.1	6.1	6.1	ns
*LVTTL_S4	3.5	4.3	4.3	4.3	4.3	4.4	4.4	4.4	4.4	4.4	ns
*LVTTL_S6	2.8	3.6	3.6	3.6	3.6	3.7	3.7	3.7	3.7	3.7	ns
*LVTTL_S8	2.2	3.1	3.1	3.1	3.1	3.1	3.1	3.2	3.2	3.2	ns
*LVTTL_S12	2.0	2.9	2.9	2.9	2.9	2.9	2.9	3.0	3.0	3.0	ns
*LVTTL_S16	1.9	2.8	2.8	2.8	2.8	2.8	2.8	2.9	2.9	2.9	ns
*LVTTL_S24	1.8	2.6	2.6	2.7	2.7	2.7	2.7	2.7	2.7	2.8	ns
*LVTTL_F2	2.9	3.8	3.8	3.8	3.8	3.8	3.8	3.9	3.9	3.9	ns
*LVTTL_F4	1.7	2.6	2.6	2.6	2.6	2.6	2.6	2.7	2.7	2.7	ns
*LVTTL_F6	1.2	2.0	2.0	2.0	2.1	2.1	2.1	2.1	2.1	2.2	ns
*LVTTL_F8	1.1	1.9	1.9	1.9	1.9	2.0	2.0	2.0	2.0	2.0	ns
*LVTTL_F12	1.0	1.8	1.8	1.8	1.8	1.9	1.9	1.9	1.9	1.9	ns
*LVTTL_F16	0.9	1.7	1.8	1.8	1.8	1.8	1.8	1.8	1.9	1.9	ns
*LVTTL_F24	0.9	1.7	1.7	1.7	1.8	1.8	1.8	1.8	1.8	1.9	ns
LVCMOS2	1.1	1.9	1.9	1.9	2.0	2.0	2.0	2.0	2.0	2.1	ns
PCI33_3	1.5	2.4	2.4	2.4	2.4	2.4	2.4	2.5	2.5	2.5	ns
PCI33_5	1.4	2.2	2.2	2.3	2.3	2.3	2.3	2.3	2.3	2.4	ns
PCI66_3	1.1	1.9	1.9	2.0	2.0	2.0	2.0	2.0	2.1	2.1	ns
GTL	1.6	2.5	2.5	2.5	2.5	2.5	2.5	2.6	2.6	2.6	ns
GTL+	1.7	2.5	2.5	2.6	2.6	2.6	2.6	2.6	2.6	2.7	ns
HSTL I	1.1	1.9	1.9	1.9	1.9	2.0	2.0	2.0	2.0	2.0	ns
HSTL III	0.9	1.7	1.7	1.8	1.8	1.8	1.8	1.8	1.8	1.9	ns
HSTL IV	0.8	1.6	1.6	1.6	1.7	1.7	1.7	1.7	1.7	1.8	ns
SSTL2 I	0.9	1.7	1.7	1.7	1.7	1.8	1.8	1.8	1.8	1.8	ns
SSTL2 II	0.8	1.6	1.6	1.6	1.6	1.7	1.7	1.7	1.7	1.7	ns
SSTL3 I	0.8	1.6	1.7	1.7	1.7	1.7	1.7	1.7	1.8	1.8	ns
SSTL3 II	0.7	1.5	1.5	1.6	1.6	1.6	1.6	1.6	1.6	1.7	ns
CTT	1.0	1.8	1.8	1.8	1.9	1.9	1.9	1.9	1.9	2.0	ns
AGP	1.0	1.8	1.8	1.9	1.9	1.9	1.9	1.9	1.9	2.0	ns

*S = Slow Slew Rate, F = Fast Slew Rate

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Input and output timing is measured at 1.4 V for LVTTL. For other I/O standards, see Table 3. In all cases, an 8 pF external capacitive load is used.

Period Tolerance: the allowed input clock period change in nanoseconds.

T_{CLKIN} $\qquad$ $T_{CLKIN} \pm T_{IPTOL}$
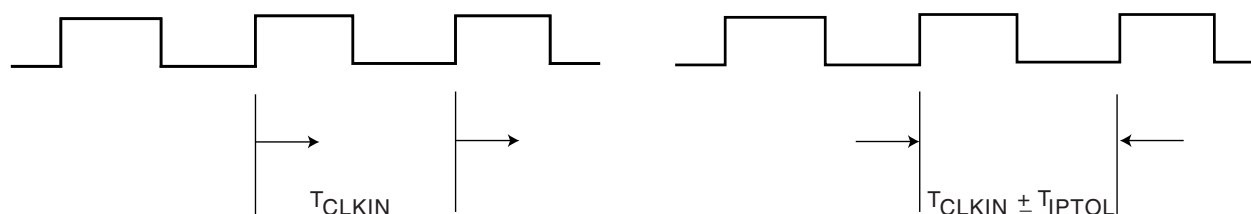
Output Jitter: the difference between an ideal reference clock edge and the actual design.

Phase Offset and Maximum Phase Difference

Ideal Period

Actual Period

+ Jitter

+/- Jitter

+ Maximum Phase Difference

+ Phase Offset
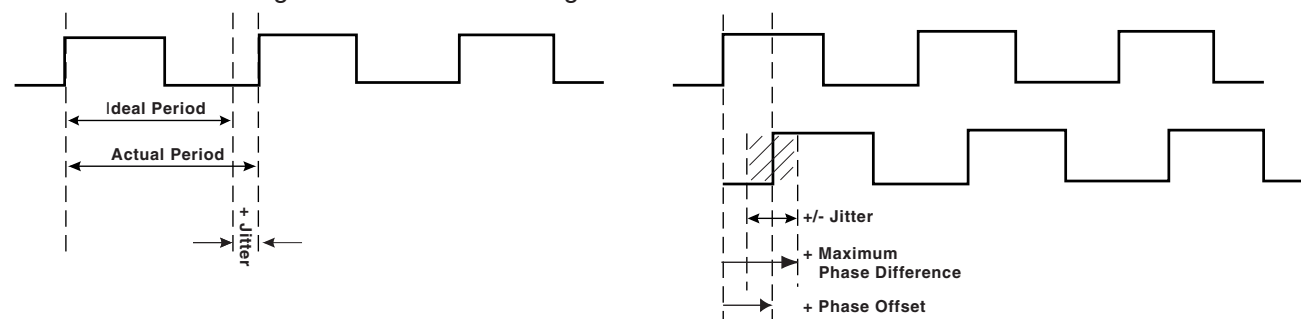
ds003_20c_110399

Figure 1: **Frequency Tolerance and Clock Jitter**

Revision History

Date	Version	Revision
11/98	1.0	Initial Xilinx release.
01/99	1.2	Updated package drawings and specs.
02/99	1.3	Update of package drawings, updated specifications.
05/99	1.4	Addition of package drawings and specifications.
05/99	1.5	Replaced FG 676 & FG680 package drawings.
07/99	1.6	Changed Boundary Scan Information and changed Figure 11, Boundary Scan Bit Sequence. Updated IOB Input & Output delays. Added Capacitance info for different I/O Standards. Added 5 V tolerant information. Added DLL Parameters and waveforms and new Pin-to-pin Input and Output Parameter tables for Global Clock Input to Output and Setup and Hold. Changed Configuration Information including Figures 12, 14, 17 & 19. Added device-dependent listings for quiescent currents ICCINTQ and ICCOQ. Updated IOB Input and Output Delays based on default standard of LVTTL, 12 mA, Fast Slew Rate. Added IOB Input Switching Characteristics Standard Adjustments.
09/99	1.7	Speed grade update to preliminary status, Power-on specification and Clock-to-Out Minimums additions, "0" hold time listing explanation, quiescent current listing update, and Figure 6 ADDRA input label correction. Added T_{IJITCC} parameter, changed T_{OJIT} to T_{OPHASE}.
01/00	1.8	Update to speed.txt file 1.96. Corrections for CRs 111036,111137, 112697, 115479, 117153, 117154, and 117612. Modified notes for Recommended Operating Conditions (voltage and temperature). Changed Bank information for V_{CCO} in CS144 package on p.43.

Date	Version	Revision
01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
03/00	2.0	New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration.
05/00	2.1	Modified "Pins not listed..." statement. Speed grade update to Final status.
05/00	2.2	Modified Table 18.
09/00	2.3	• Added XCV400 values to table under **Minimum Clock-to-Out for Virtex Devices**. • Corrected Units column in table under **IOB Input Switching Characteristics**. • Added values to table under **CLB SelectRAM Switching Characteristics**.
10/00	2.4	• Corrected Pinout information for devices in the BG256, BG432, and BG560 packages in Table 18. • Corrected **BG256 Pin Function Diagram**.
04/02/01	2.5	• Revised minimums for **Global Clock Set-Up and Hold for LVTTL Standard, with DLL**. • Converted file to modularized format. See the **Virtex Data Sheet** section.
04/19/01	2.6	• Clarified TIOCKP and TIOCKON **IOB Output Switching Characteristics** descriptors.
07/19/01	2.7	• Under **Absolute Maximum Ratings**, changed (T_{SOL}) to 220 °C.
07/26/01	2.8	• Removed T_{SOL} parameter and added footnote to **Absolute Maximum Ratings** table.
10/29/01	2.9	• Updated the speed grade designations used in data sheets, and added Table 1, which shows the current speed grade designation for each device.
02/01/02	3.0	• Added footnote to **DC Input and Output Levels** table.
07/19/02	3.1	• Removed mention of MIL-M-38510/605 specification. • Added link to xapp158 from the **Power-On Power Supply Requirements** section.
09/10/02	3.2	• Added Clock CLK to **IOB Input Switching Characteristics** and **IOB Output Switching Characteristics**.
03/01/13	4.0	The products listed in this data sheet are obsolete. See **XCN10016** for further information.

Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

- DS003-1, Virtex 2.5V FPGAs:
  Introduction and Ordering Information (Module 1)

- DS003-2, Virtex 2.5V FPGAs:
  Functional Description (Module 2)

- DS003-3, Virtex 2.5V FPGAs:
  DC and Switching Characteristics (Module 3)

- DS003-4, Virtex 2.5V FPGAs:
  Pinout Tables (Module 4)

![Xilinx logo] ®

Virtex™ 2.5 V
Field Programmable Gate Arrays

DS003-4 (v4.0) March 1, 2013   **Production Product Specification**

Virtex Pin Definitions

Table 1: **Special Purpose Pins**

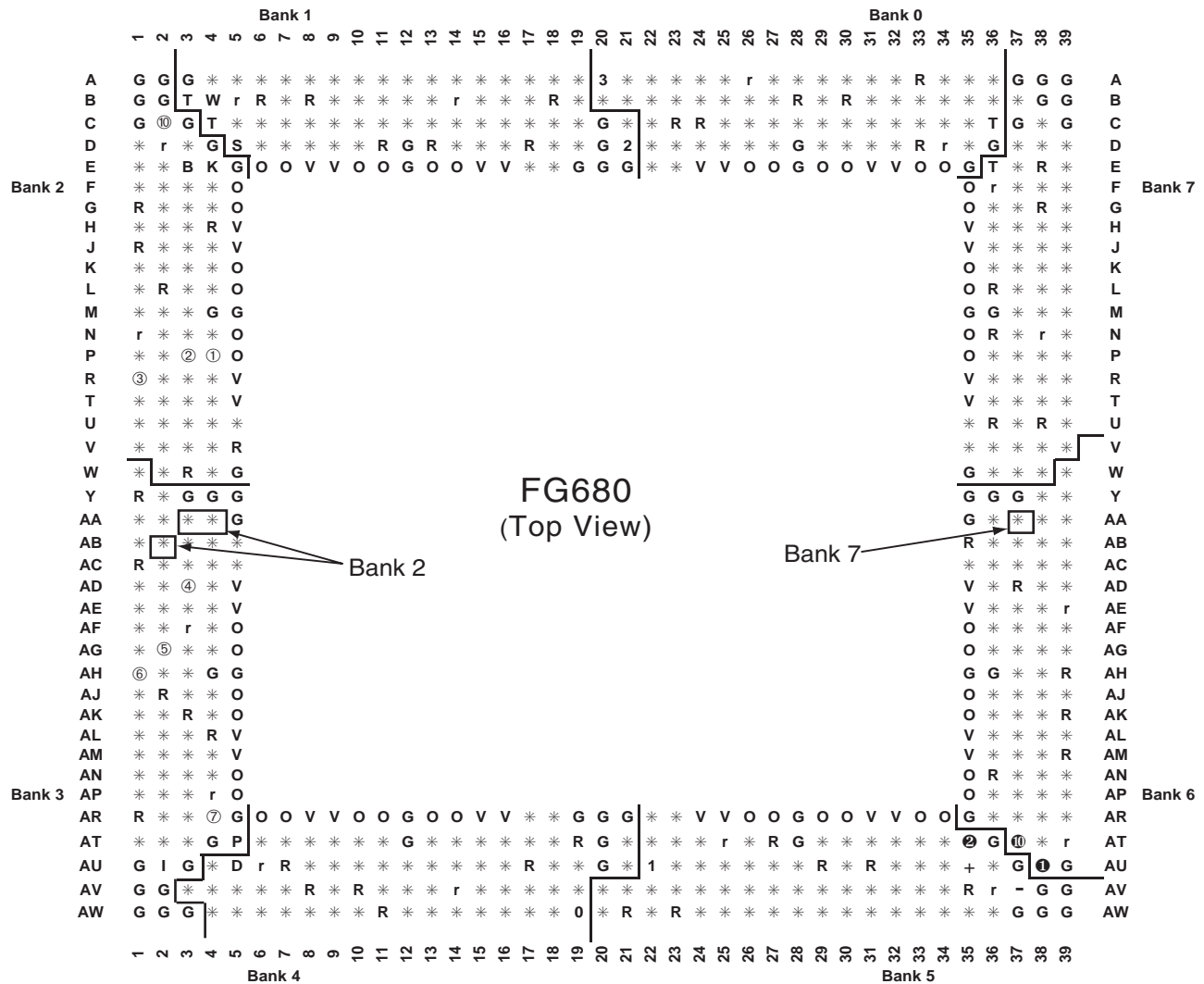| Pin Name	Dedicated Pin	Direction	Description
GCK0, GCK1, GCK2, GCK3	Yes	Input	Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin: it is an input for SelectMAP and slave-serial modes, and output in master-serial mode. After configuration, it is input only, logic level = Don't Care.
PROGRAM	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output can be open drain.
INIT	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. The pin becomes a user I/O after configuration.
BUSY/ DOUT	No	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration unless the SelectMAP port is retained. In bit-serial modes, DOUT provides header information to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In SelectMAP mode, D0 - D7 are configuration data pins. These pins become user I/Os after configuration unless the SelectMAP port is retained. In bit-serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
WRITE	No	Input	In SelectMAP mode, the active-low Write Enable signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
CS	No	Input	In SelectMAP mode, the active-low Chip Select signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary-scan Test-Access-Port pins, as defined in IEEE 1149.1.
DXN, DXP	Yes	N/A	Temperature-sensing diode pins. (Anode: DXP, cathode: DXN)
V_{CCINT}	Yes	Input	Power-supply pins for the internal core logic.
V_{CCO}	Yes	Input	Power-supply pins for the output drivers (subject to banking rules)
V_{REF}	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground

Table 3: **Virtex Pinout Tables (BGA)**

Pin Name	Device	BG256	BG352	BG432	BG560
GCK0	All	Y11	AE13	AL16	AL17
GCK1	All	Y10	AF14	AK16	AJ17
GCK2	All	A10	B14	A16	D17
GCK3	All	B10	D14	D17	A17
M0	All	Y1	AD24	AH28	AJ29
M1	All	U3	AB23	AH29	AK30
M2	All	W2	AC23	AJ28	AN32
CCLK	All	B19	C3	D4	C4
PROGRAM	All	Y20	AC4	AH3	AM1
DONE	All	W19	AD3	AH4	AJ5
INIT	All	U18	AD2	AJ2	AH5
BUSY/DOUT	All	D18	E4	D3	D4
D0/DIN	All	C19	D3	C2	E4
D1	All	E20	G1	K4	K3
D2	All	G19	J3	K2	L4
D3	All	J19	M3	P4	P3
D4	All	M19	R3	V4	W4
D5	All	P19	U4	AB1	AB5
D6	All	T20	V3	AB3	AC4
D7	All	V19	AC3	AG4	AJ4
WRITE	All	A19	D5	B4	D6
CS	All	B18	C4	D5	A2
TDI	All	C17	B3	B3	D5
TDO	All	A20	D4	C4	E6
TMS	All	D3	D23	D29	B33
TCK	All	A1	C24	D28	E29
DXN	All	W3	AD23	AH27	AK29
DXP	All	V4	AE24	AK29	AJ28

Table 3: **Virtex Pinout Tables (BGA)** *(Continued)*

Pin Name	Device	BG256	BG352	BG432	BG560
V_{CCINT} **Notes:** • Superset includes all pins, including the ones in **bold** type. Subset excludes pins in **bold** type. • In BG352, for XCV300 all the V_{CCINT} pins in the superset must be connected. For XCV150/200, V_{CCINT} pins in the subset must be connected, and pins in **bold** type can be left unconnected (these unconnected pins cannot be used as user I/O.) • In BG432, for XCV400/600/800 all V_{CCINT} pins in the superset must be connected. For XCV300, V_{CCINT} pins in the subset must be connected, and pins in **bold** type can be left unconnected (these unconnected pins cannot be used as user I/O.) • In BG560, for XCV800/1000 all V_{CCINT} pins in the superset must be connected. For XCV400/600, V_{CCINT} pins in the subset must be connected, and pins in **bold** type can be left unconnected (these unconnected pins cannot be used as user I/O.)	XCV50/100	C10, D6, D15, F4, F17, L3, L18, R4, R17, U6, U15, V10	N/A	N/A	N/A
	XCV150/200/300	Same as above	A20, C14, D10, J24, K4, P2, P25, V24, W2, AC10, AE14, AE19, **B16, D12, L1, L25, R23, T1, AF11, AF16**	A10, A17, B23, C14, C19, K3, K29, N2, N29, T1, T29, W2, W31, AB2, AB30, AJ10, AJ16, AK13, AK19, AK22, **B26, C7, F1, F30, AE29, AF1, AH8, AH24**	N/A
	XCV400/600/800/1000	N/A	N/A	Same as above	A21, B14, B18, B28, C24, E9, E12, F2, H30, J1, K32, N1, N33, U5, U30, Y2, Y31, AD2, AD32, AG3, AG31, AK8, AK11, AK17, AK20, AL14, AL27, AN25, **B12, C22, M3, N29, AB2, AB32, AJ13, AL22**
V_{CCO}, Bank 0	All	D7, D8	A17, B25, D19	A21, C29, D21	A22, A26, A30, B19, B32
V_{CCO}, Bank 1	All	D13, D14	A10, D7, D13	A1, A11, D11	A10, A16, B13, C3, E5
V_{CCO}, Bank 2	All	G17, H17	B2, H4, K1	C3, L1, L4	B2, D1, H1, M1, R2
V_{CCO}, Bank 3	All	N17, P17	P4, U1, Y4	AA1, AA4, AJ3	V1, AA2, AD1, AK1, AL2
V_{CCO}, Bank 4	All	U13, U14	AC8, AE2, AF10	AH11, AL1, AL11	AM2, AM15, AN4, AN8, AN12
V_{CCO}, Bank 5	All	U7, U8	AC14, AC20, AF17	AH21, AJ29, AL21	AL31, AM21, AN18, AN24, AN30
V_{CCO}, Bank 6	All	N4, P4	U26, W23, AE25	AA28, AA31, AL31	W32, AB33, AF33, AK33, AM32

FG680 Pin Function Diagram

Note: AA3, AA4, and AB2 are in Bank 2   **Note**: AA37 is in Bank 7   fg680_12a

Figure 11: **FG680 Pin Function Diagram**

Revision History

Date	Version	Revision
11/98	1.0	Initial Xilinx release.
01/99-02/99	1.2-1.3	Both versions updated package drawings and specs.
05/99	1.4	Addition of package drawings and specifications.
05/99	1.5	Replaced FG 676 & FG680 package drawings.
07/99	1.6	Changed Boundary Scan Information and changed Figure 11, Boundary Scan Bit Sequence. Updated IOB Input & Output delays. Added Capacitance info for different I/O Standards. Added 5 V tolerant information. Added DLL Parameters and waveforms and new Pin-to-pin Input and Output Parameter tables for Global Clock Input to Output and Setup and Hold. Changed Configuration Information including Figures 12, 14, 17 & 19. Added device-dependent listings for quiescent currents ICCINTQ and ICCOQ. Updated IOB Input and Output Delays based on default standard of LVTTL, 12 mA, Fast Slew Rate. Added IOB Input Switching Characteristics Standard Adjustments.
09/99	1.7	Speed grade update to preliminary status, Power-on specification and Clock-to-Out Minimums additions, "0" hold time listing explanation, quiescent current listing update, and Figure 6 ADDRA input label correction. Added T_{IJITCC} parameter, changed T_{OJIT} to T_{OPHASE}.
01/00	1.8	Update to speed.txt file 1.96. Corrections for CRs 111036,111137, 112697, 115479, 117153, 117154, and 117612. Modified notes for Recommended Operating Conditions (voltage and temperature). Changed Bank information for V_{CCO} in CS144 package on p.43.
01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
03/00	2.0	New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration.
05/00	2.1	Modified "Pins not listed..." statement. Speed grade update to Final status.
05/00	2.2	Modified Table 18.
09/00	2.3	• Added XCV400 values to table under **Minimum Clock-to-Out for Virtex Devices**. • Corrected Units column in table under **IOB Input Switching Characteristics**. • Added values to table under **CLB SelectRAM Switching Characteristics**.
10/00	2.4	• Corrected pinout info for devices in the BG256, BG432, and BG560 pkgs in Table 18. • Corrected **BG256 Pin Function Diagram**.
04/02/01	2.5	• Revised minimums for **Global Clock Set-Up and Hold for LVTTL Standard, with DLL**. • Converted file to modularized format. See section **Virtex Data Sheet**, below.
04/19/01	2.6	• Corrected pinout information for FG676 device in Table 4. (Added AB22 pin.)
07/19/01	2.7	• Clarified V_{CCINT} pinout information and added AE19 pin for BG352 devices in Table 3. • Changed pinouts listed for BG352 XCV400 devices in banks 0 thru 7.
07/19/02	2.8	• Changed pinouts listed for GND in TQ144 devices (see Table 2).
03/01/13	4.0	The products listed in this data sheet are obsolete. See **XCN10016** for further information.

Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

- DS003-1, Virtex 2.5V FPGAs:
  Introduction and Ordering Information (Module 1)
- DS003-2, Virtex 2.5V FPGAs:
  Functional Description (Module 2)
- DS003-3, Virtex 2.5V FPGAs:
  DC and Switching Characteristics (Module 3)
- DS003-4, Virtex 2.5V FPGAs:
  Pinout Tables (Module 4)