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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	4704
Number of Logic Elements/Cells	21168
Total RAM Bits	114688
Number of I/O	444
Number of Gates	888439
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xcv800-5fg676c">https://www.e-xfl.com/product-detail/xilinx/xcv800-5fg676c</a>

### Virtex Device/Package Combinations and Maximum I/O

Table 3: Virtex Family Maximum User I/O by Device/Package (Excluding Dedicated Clock Pins)

Package	XCV50	XCV100	XCV150	XCV200	XCV300	XCV400	XCV600	XCV800	XCV1000
CS144	94	94							
TQ144	98	98							
PQ240	166	166	166	166	166				
HQ240						166	166	166	
BG256	180	180	180	180					
BG352			260	260	260				
BG432					316	316	316	316	
BG560						404	404	404	404
FG256	176	176	176	176					
FG456			260	284	312				
FG676						404	444	444	
FG680							512	512	512

### Virtex Ordering Information



Figure 1: Virtex Ordering Information

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

**Figure 10** is a diagram of the Virtex Series boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

### Instruction Set

The Virtex Series boundary scan instruction set also includes instructions to configure the device and read back configuration data (CFG\_IN, CFG\_OUT, and JSTART). The complete instruction set is coded as shown in **Table 5**.

### Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out, and 3-State Control. Non-IOB pins have appropriate partial bit population if input-only or output-only. Each EXTEST CAPTURED-OR state captures all In, Out, and 3-state pins.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA supports up to two additional internal scan chains that can be specified using the BSCAN macro. The macro provides two user pins (SEL1 and SEL2) which are decoded of the USER1 and USER2 instructions respectively. For these instructions, two corresponding pins (TDO1 and TDO2) allow user scan data to be shifted out of TDO.

Likewise, there are individual clock pins (DRCK1 and DRCK2) for each user register. There is a common input pin (TDI) and shared output pins that represent the state of the TAP controller (RESET, SHIFT, and UPDATE).

### Bit Sequence

The order within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

From a cavity-up view of the chip (as shown in EPIC), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in **Figure 11**.

BSDL (Boundary Scan Description Language) files for Virtex Series devices are available on the Xilinx web site in the File Download area.

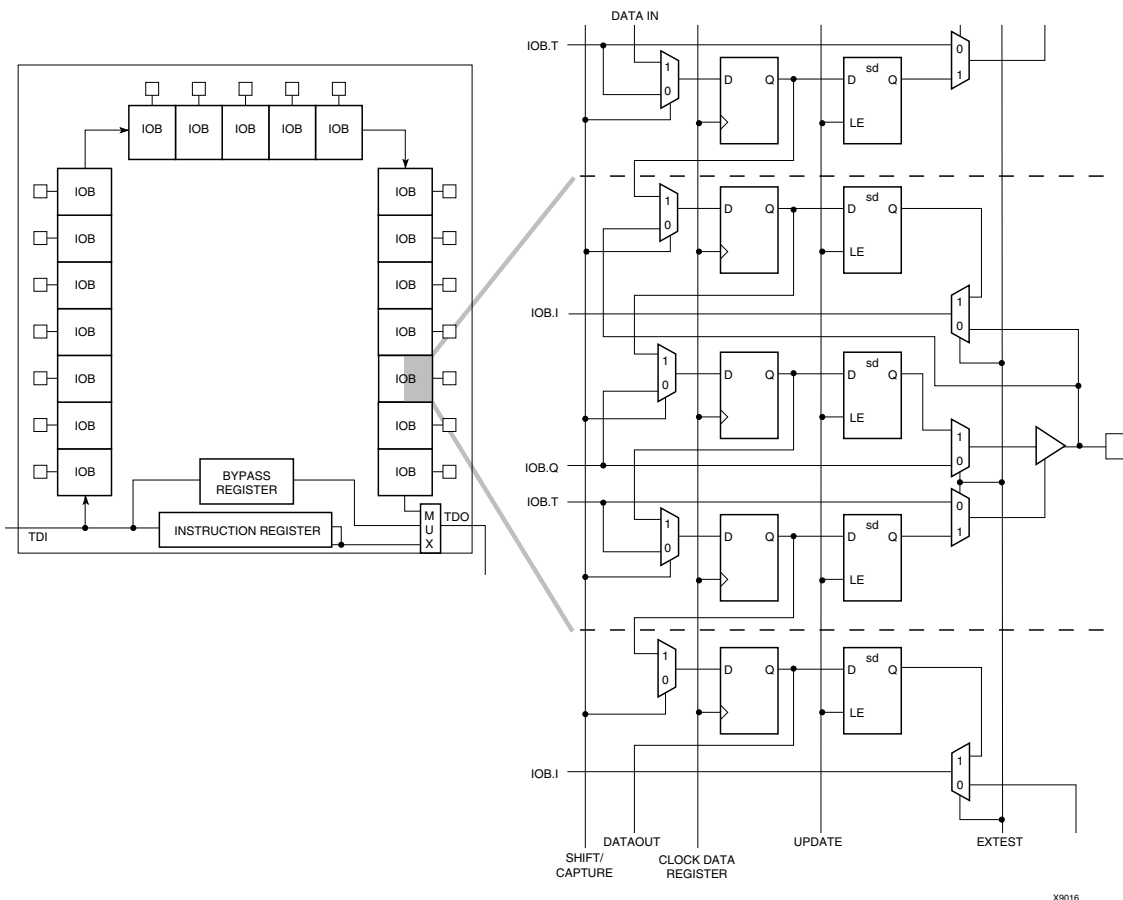


Figure 10: Virtex Series Boundary Scan Logic

ers with a common user interface regardless of their choice of entry and verification tools. The XDM software simplifies the selection of implementation options with pull-down menus and on-line help.

Application programs ranging from schematic capture to Placement and Routing (PAR) can be accessed through the XDM software. The program command sequence is generated prior to execution, and stored for documentation.

Several advanced software features facilitate Virtex design. RPMs, for example, are schematic-based macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the Xilinx FPGA Foundation development system provides interfaces to the following synthesis design environments.

- Synopsys (FPGA Compiler, FPGA Express)
- Exemplar (Spectrum)
- Synplicity (Synplify)

For schematic design entry, the Xilinx FPGA Foundation and alliance development system provides interfaces to the following schematic-capture design environments.

- Mentor Graphics V8 (Design Architect, QuickSim II)
- Viewlogic Systems (Viewdraw)

Third-party vendors support many other environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Virtex FPGAs supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The “soft macro” portion of the library contains detailed descriptions of common logic functions, but does not contain any partitioning or placement information. The performance of these macros depends, therefore, on the partitioning and placement obtained during implementation.

RPMs, on the other hand, do contain predetermined partitioning and placement information that permits optimal implementation of these functions. Users can create their own library of soft macros or RPMs based on the macros and primitives in the standard library.

The design environment supports hierarchical design entry, with high-level schematics that comprise major functional blocks, while lower-level schematics define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical

design, thus allowing the most convenient entry method to be used for each portion of the design.

## Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF net list for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floor planning.

The implementation software incorporates Timing Wizard® timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered on a schematic in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

## Design Verification

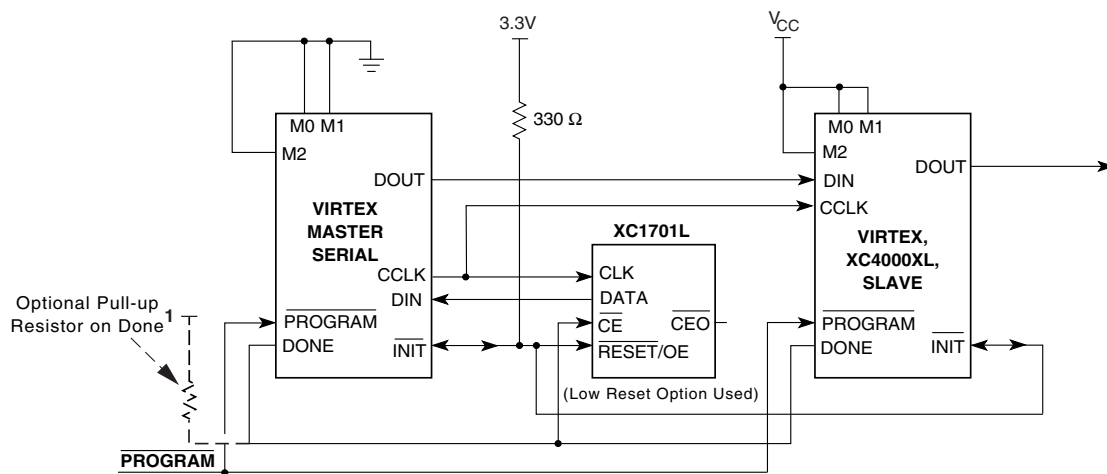
In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the net list for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the TRACE® static timing analyzer.

For in-circuit debugging, the development system includes a download and readback cable. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

Table 8: Master/Slave Serial Mode Programming Switching

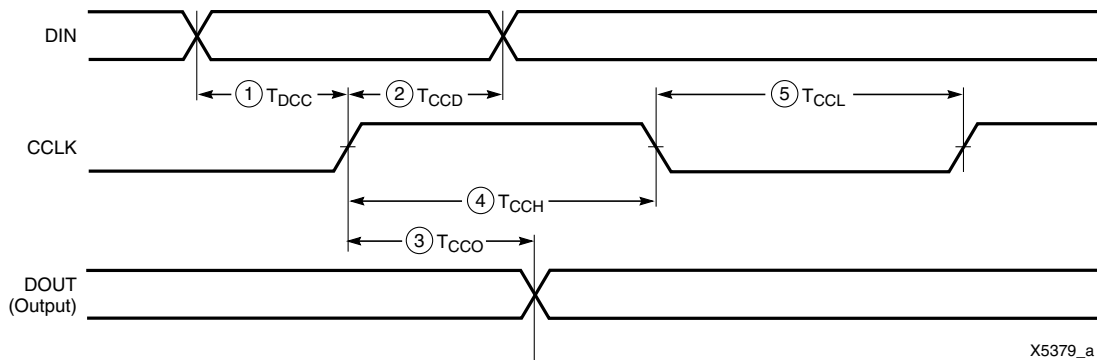
	Description	Figure References	Symbol	Values	Units
CCLK	DIN setup/hold, slave mode	1/2	$T_{DCC}/T_{CCD}$	5.0 / 0	ns, min
	DIN setup/hold, master mode	1/2	$T_{DSCK}/T_{CKDS}$	5.0 / 0	ns, min
	DOUT	3	$T_{CCO}$	12.0	ns, max
	High time	4	$T_{CCH}$	5.0	ns, min
	Low time	5	$T_{CCL}$	5.0	ns, min
	Maximum Frequency		$F_{CC}$	66	MHz, max
	Frequency Tolerance, master mode with respect to nominal			+45% -30%	



**Note 1:** If none of the Virtex FPGAs have been selected to drive DONE, an external pull-up resistor of 330 Ω should be added to the common DONE line. (For Spartan-XL devices, add a 4.7K Ω pull-up resistor.) This pull-up is not needed if the DriveDONE attribute is set. If used, DriveDONE should be selected only for the last device in the configuration chain.

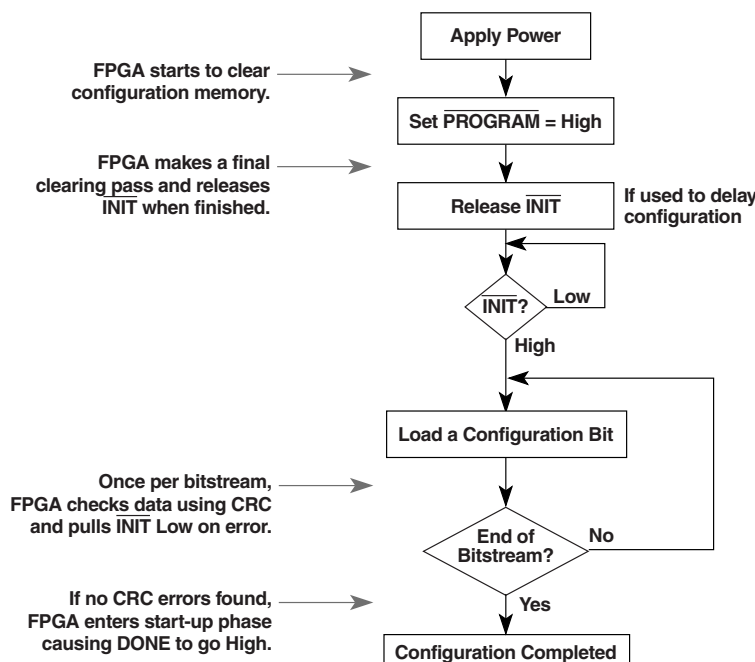
xcv\_12\_050103

Figure 12: Master/Slave Serial Mode Circuit Diagram



X5379\_a

Figure 13: Slave-Serial Mode Programming Switching Characteristics



ds003\_154\_111799

Figure 15: Serial Configuration Flowchart

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained to permit high-speed 8-bit readback.

Retention of the SelectMAP port is selectable on a design-by-design basis when the bitstream is generated. If retention is selected, PROHIBIT constraints are required to prevent the SelectMAP-port pins from being used as user I/O.

Multiple Virtex FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, WRITE, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the CS pin of each device in turn and writing the appropriate data. see Table 9 for SelectMAP Write Timing Characteristics.

Table 9: SelectMAP Write Timing Characteristics

	Description		Symbol		Units
CCLK	D <sub>0-7</sub> Setup/Hold	1/2	T <sub>SMDCC</sub> /T <sub>SMCCD</sub>	5.0 / 1.7	ns, min
	$\overline{\text{CS}}$ Setup/Hold	3/4	T <sub>SMCSCC</sub> /T <sub>SMCCCS</sub>	7.0 / 1.7	ns, min
	$\overline{\text{WRITE}}$ Setup/Hold	5/6	T <sub>SMCCW</sub> /T <sub>SMWCC</sub>	7.0 / 1.7	ns, min
	BUSY Propagation Delay	7	T <sub>SMCKBY</sub>	12.0	ns, max
	Maximum Frequency		F <sub>CC</sub>	66	MHz, max
	Maximum Frequency with no handshake		F <sub>CCNH</sub>	50	MHz, max

### Write

Write operations send packets of configuration data into the FPGA. The sequence of operations for a multi-cycle write operation is shown below. Note that a configuration packet can be split into many such sequences. The packet does not have to complete within one assertion of  $\overline{\text{CS}}$ , illustrated in Figure 16.

1. Assert  $\overline{\text{WRITE}}$  and  $\overline{\text{CS}}$  Low. Note that when  $\overline{\text{CS}}$  is asserted on successive CCLKs,  $\overline{\text{WRITE}}$  must remain either asserted or de-asserted. Otherwise an abort will be initiated, as described below.
2. Drive data onto D[7:0]. Note that to avoid contention, the data source should not be enabled while  $\overline{\text{CS}}$  is Low and  $\overline{\text{WRITE}}$  is High. Similarly, while  $\overline{\text{WRITE}}$  is High, no more than one  $\overline{\text{CS}}$  should be asserted.

Date	Version	Revision
01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
03/00	2.0	New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration.
05/00	2.1	Modified “Pins not listed...” statement. Speed grade update to Final status.
05/00	2.2	Modified Table 18.
09/00	2.3	<ul style="list-style-type: none"> <li>Added XCV400 values to table under <b>Minimum Clock-to-Out for Virtex Devices</b>.</li> <li>Corrected Units column in table under <b>IOB Input Switching Characteristics</b>.</li> <li>Added values to table under <b>CLB SelectRAM Switching Characteristics</b>.</li> </ul>
10/00	2.4	<ul style="list-style-type: none"> <li>Corrected Pinout information for devices in the BG256, BG432, and BG560 packages in Table 18.</li> <li>Corrected <b>BG256 Pin Function Diagram</b>.</li> </ul>
04/01	2.5	<ul style="list-style-type: none"> <li>Revised minimums for <b>Global Clock Set-Up and Hold for LVTTTL Standard, with DLL</b>.</li> <li>Updated SelectMAP Write Timing Characteristics values in <b>Table 9</b>.</li> <li>Converted file to modularized format. See the <b>Virtex Data Sheet</b> section.</li> </ul>
07/19/01	2.6	<ul style="list-style-type: none"> <li>Made minor edits to text under <b>Configuration</b>.</li> </ul>
07/19/02	2.7	<ul style="list-style-type: none"> <li>Made minor edit to <b>Figure 16</b> and <b>Figure 18</b>.</li> </ul>
09/10/02	2.8	<ul style="list-style-type: none"> <li>Added clarifications in the <b>Configuration</b>, <b>Boundary-Scan Mode</b>, and <b>Block SelectRAM</b> sections. Revised <b>Figure 17</b>.</li> </ul>
12/09/02	2.8.1	<ul style="list-style-type: none"> <li>Added clarification in the <b>Boundary Scan</b> section.</li> <li>Corrected number of buffered Hex lines listed in <b>General Purpose Routing</b> section.</li> </ul>
03/01/13	4.0	The products listed in this data sheet are obsolete. See <a href="#">XCN10016</a> for further information.

## Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

- DS003-1, Virtex 2.5V FPGAs:  
Introduction and Ordering Information (Module 1)
- DS003-2, Virtex 2.5V FPGAs:  
Functional Description (Module 2)
- DS003-3, Virtex 2.5V FPGAs:  
DC and Switching Characteristics (Module 3)
- DS003-4, Virtex 2.5V FPGAs:  
Pinout Tables (Module 4)





## Virtex™ 2.5 V Field Programmable Gate Arrays

DS003-3 (v4.0) March 1, 2013

Production Product Specification

### Virtex Electrical Characteristics

#### Definition of Terms

Electrical and switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

**Advance:** These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

**Preliminary:** These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

**Production:** These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. Contact the factory for design considerations requiring more detailed information.

**Table 1** correlates the current status of each Virtex device with a corresponding speed file designation.

**Table 1: Virtex Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XCV50			–6, –5, –4
XCV100			–6, –5, –4
XCV150			–6, –5, –4
XCV200			–6, –5, –4
XCV300			–6, –5, –4
XCV400			–6, –5, –4
XCV600			–6, –5, –4
XCV800			–6, –5, –4
XCV1000			–6, –5, –4

All specifications are subject to change without notice.



## Virtex DC Characteristics

### Absolute Maximum Ratings

Symbol	Description <sup>(1)</sup>			Units
$V_{CCINT}$	Supply voltage relative to GND <sup>(2)</sup>		–0.5 to 3.0	V
$V_{CCO}$	Supply voltage relative to GND <sup>(2)</sup>		–0.5 to 4.0	V
$V_{REF}$	Input Reference Voltage		–0.5 to 3.6	V
$V_{IN}$	Input voltage relative to GND <sup>(3)</sup>	Using $V_{REF}$	–0.5 to 3.6	V
		Internal threshold	–0.5 to 5.5	V
$V_{TS}$	Voltage applied to 3-state output		–0.5 to 5.5	V
$V_{CC}$	Longest Supply Voltage Rise Time from 1V-2.375V		50	ms
$T_{STG}$	Storage temperature (ambient)		–65 to +150	°C
$T_J$	Junction temperature <sup>(4)</sup>	Plastic Packages	+125	°C

**Notes:**

- Stresses beyond those listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time can affect device reliability.
- Power supplies can turn on in any order.
- For protracted periods (e.g., longer than a day),  $V_{IN}$  should not exceed  $V_{CCO}$  by more than 3.6 V.
- For soldering guidelines and thermal considerations, see the "Device Packaging" information on [www.xilinx.com](http://www.xilinx.com).

### Recommended Operating Conditions

Symbol	Description		Min	Max	Units
$V_{CCINT}^{(1)}$	Input Supply voltage relative to GND, $T_J = 0\text{ °C to }+85\text{ °C}$	Commercial	2.5 – 5%	2.5 + 5%	V
	Input Supply voltage relative to GND, $T_J = -40\text{ °C to }+100\text{ °C}$	Industrial	2.5 – 5%	2.5 + 5%	V
$V_{CCO}^{(4)}$	Supply voltage relative to GND, $T_J = 0\text{ °C to }+85\text{ °C}$	Commercial	1.4	3.6	V
	Supply voltage relative to GND, $T_J = -40\text{ °C to }+100\text{ °C}$	Industrial	1.4	3.6	V
$T_{IN}$	Input signal transition time			250	ns

**Notes:**

- Correct operation is guaranteed with a minimum  $V_{CCINT}$  of 2.375 V (Nominal  $V_{CCINT}$  –5%). Below the minimum value, all delay parameters increase by 3% for each 50-mV reduction in  $V_{CCINT}$  below the specified range.
- At junction temperatures above those listed as Operating Conditions, delay parameters do increase. Please refer to the TRCE report.
- Input and output measurement threshold is ~50% of  $V_{CC}$ .
- Min and Max values for  $V_{CCO}$  are I/O Standard dependant.

## Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device<sup>(1)</sup> from 0 V. The current is highest at the fastest suggested ramp rate (0 V to nominal voltage in 2 ms) and is lowest at the slowest allowed ramp rate (0 V to nominal voltage in 50 ms). For more details on power supply requirements, see Application Note XAPP158 on [www.xilinx.com](http://www.xilinx.com).

Product	Description <sup>(2)</sup>	Current Requirement <sup>(1,3)</sup>
Virtex Family, Commercial Grade	Minimum required current supply	500 mA
Virtex Family, Industrial Grade	Minimum required current supply	2 A

### Notes:

1. Ramp rate used for this specification is from 0 - 2.7 VDC. Peak current occurs on or near the internal power-on reset threshold of 1.0V and lasts for less than 3 ms.
2. Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
3. Larger currents can result if ramp rates are forced to be faster.

## DC Input and Output Levels

Values for  $V_{IL}$  and  $V_{IH}$  are recommended input voltages. Values for  $I_{OL}$  and  $I_{OH}$  are guaranteed output currents over the recommended operating conditions at the  $V_{OL}$  and  $V_{OH}$  test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum  $V_{CCO}$  for each standard with the respective  $V_{OL}$  and  $V_{OH}$  voltage levels shown. Other standards are sample tested.

Input/Output Standard	$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$	$I_{OH}$
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTL <sup>(1)</sup>	-0.5	0.8	2.0	5.5	0.4	2.4	24	-24
LVC MOS2	-0.5	.7	1.7	5.5	0.4	1.9	12	-12
PCI, 3.3 V	-0.5	44% $V_{CCINT}$	60% $V_{CCINT}$	$V_{CCO} + 0.5$	10% $V_{CCO}$	90% $V_{CCO}$	Note 2	Note 2
PCI, 5.0 V	-0.5	0.8	2.0	5.5	0.55	2.4	Note 2	Note 2
GTL	-0.5	$V_{REF} - 0.05$	$V_{REF} + 0.05$	3.6	0.4	n/a	40	n/a
GTL+	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.6	n/a	36	n/a
HSTL I <sup>(3)</sup>	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	8	-8
HSTL III	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	24	-8
HSTL IV	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	48	-8
SSTL3 I	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.6$	$V_{REF} + 0.6$	8	-8
SSTL3 II	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.8$	$V_{REF} + 0.8$	16	-16
SSTL2 I	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.61$	$V_{REF} + 0.61$	7.6	-7.6
SSTL2 II	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.80$	$V_{REF} + 0.80$	15.2	-15.2
CTT	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
AGP	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	10% $V_{CCO}$	90% $V_{CCO}$	Note 2	Note 2

### Notes:

1.  $V_{OL}$  and  $V_{OH}$  for lower drive currents are sample tested.
2. Tested according to the relevant specifications.
3. DC input and output levels for HSTL18 (HSTL I/O standard with  $V_{CCO}$  of 1.8 V) are provided in an HSTL white paper on [www.xilinx.com](http://www.xilinx.com).

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Clock CLK to Pad delay with OBUFT enabled (non-3-state)	$T_{IOCKP}$	1.0	2.9	3.2	3.5	ns, max
Clock CLK to Pad high-impedance (synchronous) <sup>(1)</sup>	$T_{IOCKHZ}$	1.1	2.3	2.5	2.9	ns, max
Clock CLK to valid data on Pad delay, plus enable delay for OBUFT	$T_{IOCKON}$	1.5	3.4	3.7	4.1	ns, max
<b>Setup and Hold Times before/after Clock CLK<sup>(2)</sup></b>		<b>Setup Time / Hold Time</b>				
O input	$T_{IOOCK}/T_{IOCKO}$	0.51 / 0	1.1 / 0	1.2 / 0	1.3 / 0	ns, min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$	0.37 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
SR input (OFF)	$T_{IOSRCKO}/T_{IOCKOSR}$	0.52 / 0	1.1 / 0	1.2 / 0	1.4 / 0	ns, min
3-State Setup Times, T input	$T_{IOTCK}/T_{IOCKT}$	0.34 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$	0.41 / 0	0.9 / 0	0.9 / 0	1.1 / 0	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$	0.49 / 0	1.0 / 0	1.1 / 0	1.3 / 0	ns, min
<b>Set/Reset Delays</b>						
SR input to Pad (asynchronous)	$T_{IOSRP}$	1.6	3.8	4.1	4.6	ns, max
SR input to Pad high-impedance (asynchronous) <sup>(1)</sup>	$T_{IOSRHZ}$	1.6	3.1	3.4	3.9	ns, max
SR input to valid data on Pad (asynchronous)	$T_{IOSRON}$	2.0	4.2	4.6	5.1	ns, max
GSR to Pad	$T_{IOGSRQ}$	4.9	9.7	10.9	12.5	ns, max

**Notes:**

1. 3-state turn-off delays should not be adjusted.
2. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

## I/O Standard Global Clock Input Adjustments

Description	Symbol	Standard <sup>(1)</sup>	Speed Grade				Units
			Min	-6	-5	-4	
Data Input Delay Adjustments							
Standard-specific global clock input delay adjustments	T <sub>GPLVTTL</sub>	LVTTL	0	0	0	0	ns, max
	T <sub>GPLVCMOS2</sub>	LVC MOS2	−0.02	−0.04	−0.04	−0.05	ns, max
	T <sub>GP PCI33_3</sub>	PCI, 33 MHz, 3.3 V	−0.05	−0.11	−0.12	−0.14	ns, max
	T <sub>GP PCI33_5</sub>	PCI, 33 MHz, 5.0 V	0.13	0.25	0.28	0.33	ns, max
	T <sub>GP PCI66_3</sub>	PCI, 66 MHz, 3.3 V	−0.05	−0.11	−0.12	−0.14	ns, max
	T <sub>GPGTL</sub>	GTL	0.7	0.8	0.9	0.9	ns, max
	T <sub>GPGTLP</sub>	GTL+	0.7	0.8	0.8	0.8	ns, max
	T <sub>GPHSTL</sub>	HSTL	0.7	0.7	0.7	0.7	ns, max
	T <sub>GPSSTL2</sub>	SSTL2	0.6	0.52	0.51	0.50	ns, max
	T <sub>GPSSTL3</sub>	SSTL3	0.6	0.6	0.55	0.54	ns, max
	T <sub>GPCTT</sub>	CTT	0.7	0.7	0.7	0.7	ns, max
	T <sub>GPAGP</sub>	AGP	0.6	0.54	0.53	0.52	ns, max

### Notes:

1. Input timing for GPLVTTL is measured at 1.4 V. For other I/O standards, see [Table 3](#).

## CLB SelectRAM Switching Characteristics

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Sequential Delays						
Clock CLK to X/Y outputs (WE active) 16 x 1 mode	T <sub>SHCKO16</sub>	1.2	2.3	2.6	3.0	ns, max
Clock CLK to X/Y outputs (WE active) 32 x 1 mode	T <sub>SHCKO32</sub>	1.2	2.7	3.1	3.5	ns, max
Shift-Register Mode						
Clock CLK to X/Y outputs	T <sub>REG</sub>	1.2	3.7	4.1	4.7	ns, max
Setup and Hold Times before/after Clock CLK <sup>(1)</sup>	Setup Time / Hold Time					
F/G address inputs	T <sub>AS</sub> /T <sub>AH</sub>	0.25 / 0	0.5 / 0	0.6 / 0	0.7 / 0	ns, min
BX/BY data inputs (DIN)	T <sub>DS</sub> /T <sub>DH</sub>	0.34 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
CE input (WE)	T <sub>WS</sub> /T <sub>WH</sub>	0.38 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
Shift-Register Mode						
BX/BY data inputs (DIN)	T <sub>SHDICK</sub>	0.34	0.7	0.8	0.9	ns, min
CE input (WS)	T <sub>SHCECK</sub>	0.38	0.8	0.9	1.0	ns, min
Clock CLK						
Minimum Pulse Width, High	T <sub>WPH</sub>	1.2	2.4	2.7	3.1	ns, min
Minimum Pulse Width, Low	T <sub>WPL</sub>	1.2	2.4	2.7	3.1	ns, min
Minimum clock period to meet address write cycle time	T <sub>WC</sub>	2.4	4.8	5.4	6.2	ns, min
Shift-Register Mode						
Minimum Pulse Width, High	T <sub>SRPH</sub>	1.2	2.4	2.7	3.1	ns, min
Minimum Pulse Width, Low	T <sub>SRPL</sub>	1.2	2.4	2.7	3.1	ns, min

**Notes:**

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

### Virtex Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

#### Global Clock Set-Up and Hold for LVTTL Standard, *with DLL*

Description	Symbol	Device	Speed Grade				Units
			Min	-6	-5	-4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in Input Delay Adjustments.							
No Delay Global Clock and IFF, with DLL	$T_{PSDLL}/T_{PHDLL}$	XCV50	0.40 / -0.4	1.7 / -0.4	1.8 / -0.4	2.1 / -0.4	ns, min
		XCV100	0.40 / -0.4	1.7 / -0.4	1.9 / -0.4	2.1 / -0.4	ns, min
		XCV150	0.40 / -0.4	1.7 / -0.4	1.9 / -0.4	2.1 / -0.4	ns, min
		XCV200	0.40 / -0.4	1.7 / -0.4	1.9 / -0.4	2.1 / -0.4	ns, min
		XCV300	0.40 / -0.4	1.7 / -0.4	1.9 / -0.4	2.1 / -0.4	ns, min
		XCV400	0.40 / -0.4	1.7 / -0.4	1.9 / -0.4	2.1 / -0.4	ns, min
		XCV600	0.40 / -0.4	1.7 / -0.4	1.9 / -0.4	2.1 / -0.4	ns, min
		XCV800	0.40 / -0.4	1.7 / -0.4	1.9 / -0.4	2.1 / -0.4	ns, min
		XCV1000	0.40 / -0.4	1.7 / -0.4	1.9 / -0.4	2.1 / -0.4	ns, min

IFF = Input Flip-Flop or Latch

#### Notes:

1. Set-up time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
2. DLL output jitter is already included in the timing calculation.
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Date	Version	Revision
01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
03/00	2.0	New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration.
05/00	2.1	Modified "Pins not listed..." statement. Speed grade update to Final status.
05/00	2.2	Modified Table 18.
09/00	2.3	<ul style="list-style-type: none"> <li>Added XCV400 values to table under <b>Minimum Clock-to-Out for Virtex Devices</b>.</li> <li>Corrected Units column in table under <b>IOB Input Switching Characteristics</b>.</li> <li>Added values to table under <b>CLB SelectRAM Switching Characteristics</b>.</li> </ul>
10/00	2.4	<ul style="list-style-type: none"> <li>Corrected Pinout information for devices in the BG256, BG432, and BG560 packages in Table 18.</li> <li>Corrected <b>BG256 Pin Function Diagram</b>.</li> </ul>
04/02/01	2.5	<ul style="list-style-type: none"> <li>Revised minimums for <b>Global Clock Set-Up and Hold for LVTTTL Standard, with DLL</b>.</li> <li>Converted file to modularized format. See the <b>Virtex Data Sheet</b> section.</li> </ul>
04/19/01	2.6	<ul style="list-style-type: none"> <li>Clarified TIOCKP and TIOCKON <b>IOB Output Switching Characteristics</b> descriptors.</li> </ul>
07/19/01	2.7	<ul style="list-style-type: none"> <li>Under <b>Absolute Maximum Ratings</b>, changed (<math>T_{SOL}</math>) to 220 °C.</li> </ul>
07/26/01	2.8	<ul style="list-style-type: none"> <li>Removed <math>T_{SOL}</math> parameter and added footnote to <b>Absolute Maximum Ratings</b> table.</li> </ul>
10/29/01	2.9	<ul style="list-style-type: none"> <li>Updated the speed grade designations used in data sheets, and added <b>Table 1</b>, which shows the current speed grade designation for each device.</li> </ul>
02/01/02	3.0	<ul style="list-style-type: none"> <li>Added footnote to <b>DC Input and Output Levels</b> table.</li> </ul>
07/19/02	3.1	<ul style="list-style-type: none"> <li>Removed mention of MIL-M-38510/605 specification.</li> <li>Added link to xapp158 from the <b>Power-On Power Supply Requirements</b> section.</li> </ul>
09/10/02	3.2	<ul style="list-style-type: none"> <li>Added Clock CLK to <b>IOB Input Switching Characteristics</b> and <b>IOB Output Switching Characteristics</b>.</li> </ul>
03/01/13	4.0	The products listed in this data sheet are obsolete. See <a href="#">XCN10016</a> for further information.

## Virtex Data Sheet

The Virtex Data Sheet contains the following modules:

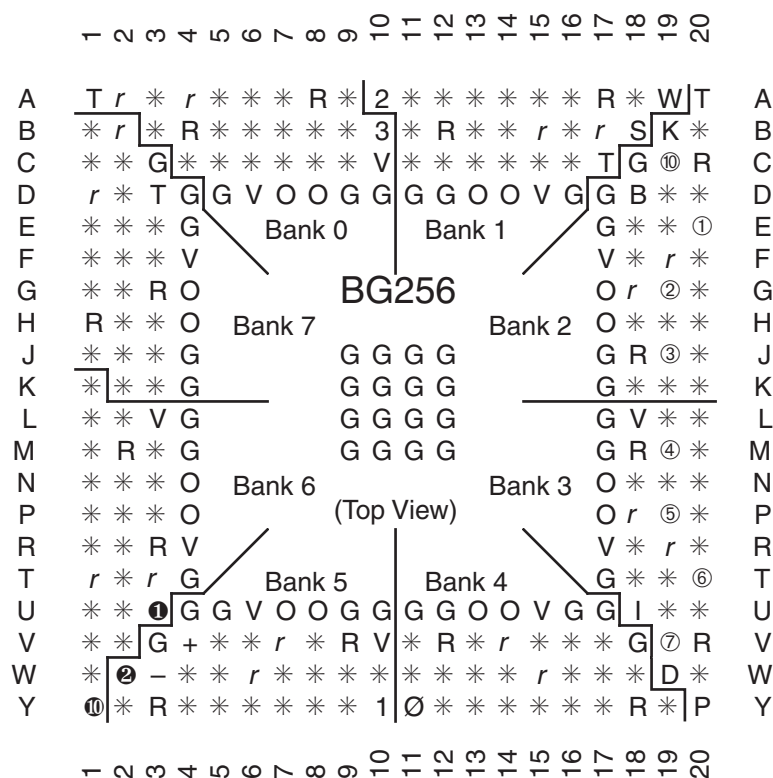
- DS003-1, Virtex 2.5V FPGAs:  
Introduction and Ordering Information (Module 1)
- DS003-2, Virtex 2.5V FPGAs:  
Functional Description (Module 2)
- DS003-3, Virtex 2.5V FPGAs:  
DC and Switching Characteristics (Module 3)
- DS003-4, Virtex 2.5V FPGAs:  
Pinout Tables (Module 4)



Table 3: Virtex Pinout Tables (BGA)

Pin Name	Device	BG256	BG352	BG432	BG560
GCK0	All	Y11	AE13	AL16	AL17
GCK1	All	Y10	AF14	AK16	AJ17
GCK2	All	A10	B14	A16	D17
GCK3	All	B10	D14	D17	A17
M0	All	Y1	AD24	AH28	AJ29
M1	All	U3	AB23	AH29	AK30
M2	All	W2	AC23	AJ28	AN32
CCLK	All	B19	C3	D4	C4
PROGRAM	All	Y20	AC4	AH3	AM1
DONE	All	W19	AD3	AH4	AJ5
INIT	All	U18	AD2	AJ2	AH5
BUSY/DOUT	All	D18	E4	D3	D4
D0/DIN	All	C19	D3	C2	E4
D1	All	E20	G1	K4	K3
D2	All	G19	J3	K2	L4
D3	All	J19	M3	P4	P3
D4	All	M19	R3	V4	W4
D5	All	P19	U4	AB1	AB5
D6	All	T20	V3	AB3	AC4
D7	All	V19	AC3	AG4	AJ4
WRITE	All	A19	D5	B4	D6
CS	All	B18	C4	D5	A2
TDI	All	C17	B3	B3	D5
TDO	All	A20	D4	C4	E6
TMS	All	D3	D23	D29	B33
TCK	All	A1	C24	D28	E29
DXN	All	W3	AD23	AH27	AK29
DXP	All	V4	AE24	AK29	AJ28

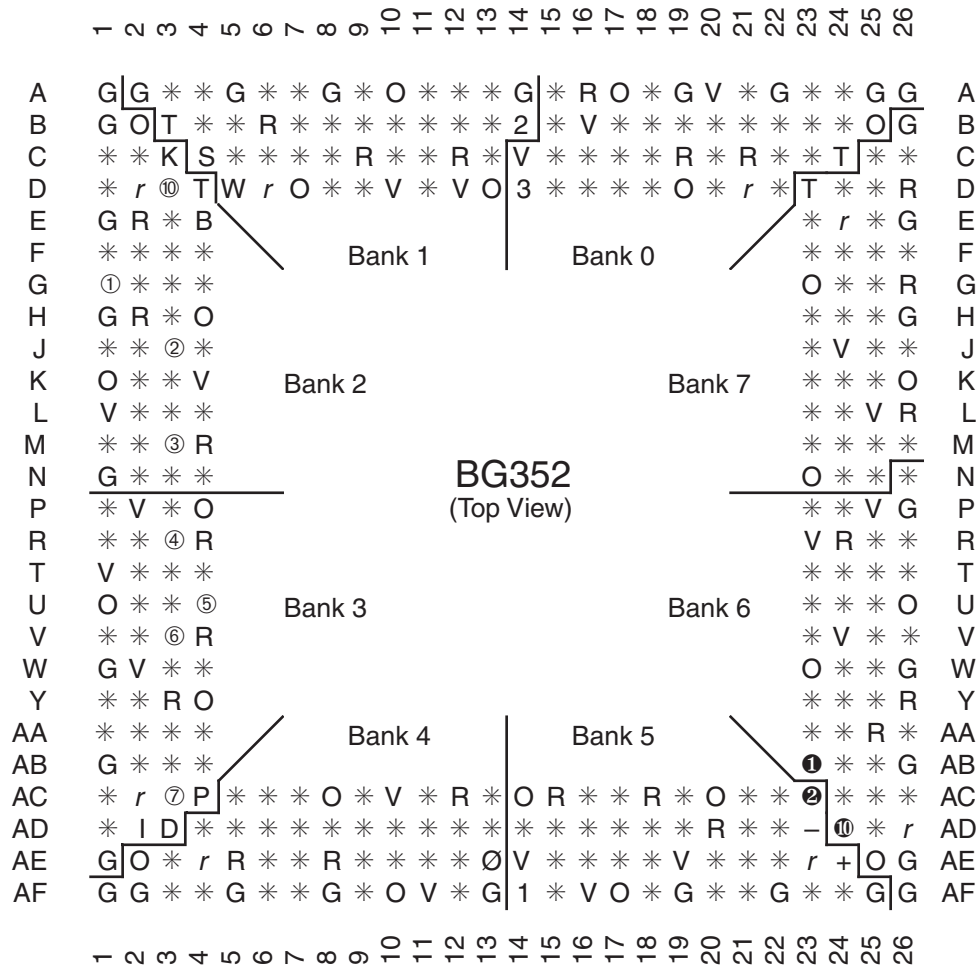
## BG256 Pin Function Diagram



DS003\_18\_100300

Figure 4: BG256 Pin Function Diagram

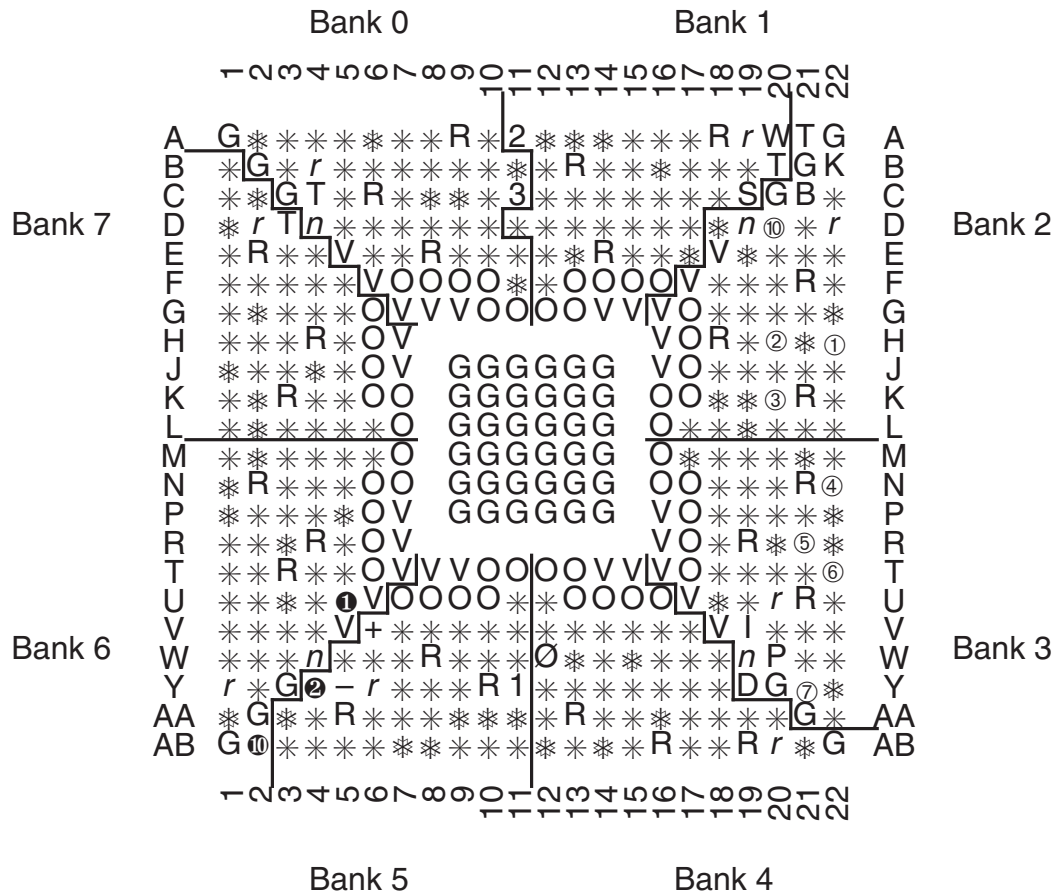
## BG352 Pin Function Diagram



DS003\_19\_100600

Figure 5: BG352 Pin Function Diagram

## FG456 Pin Function Diagram



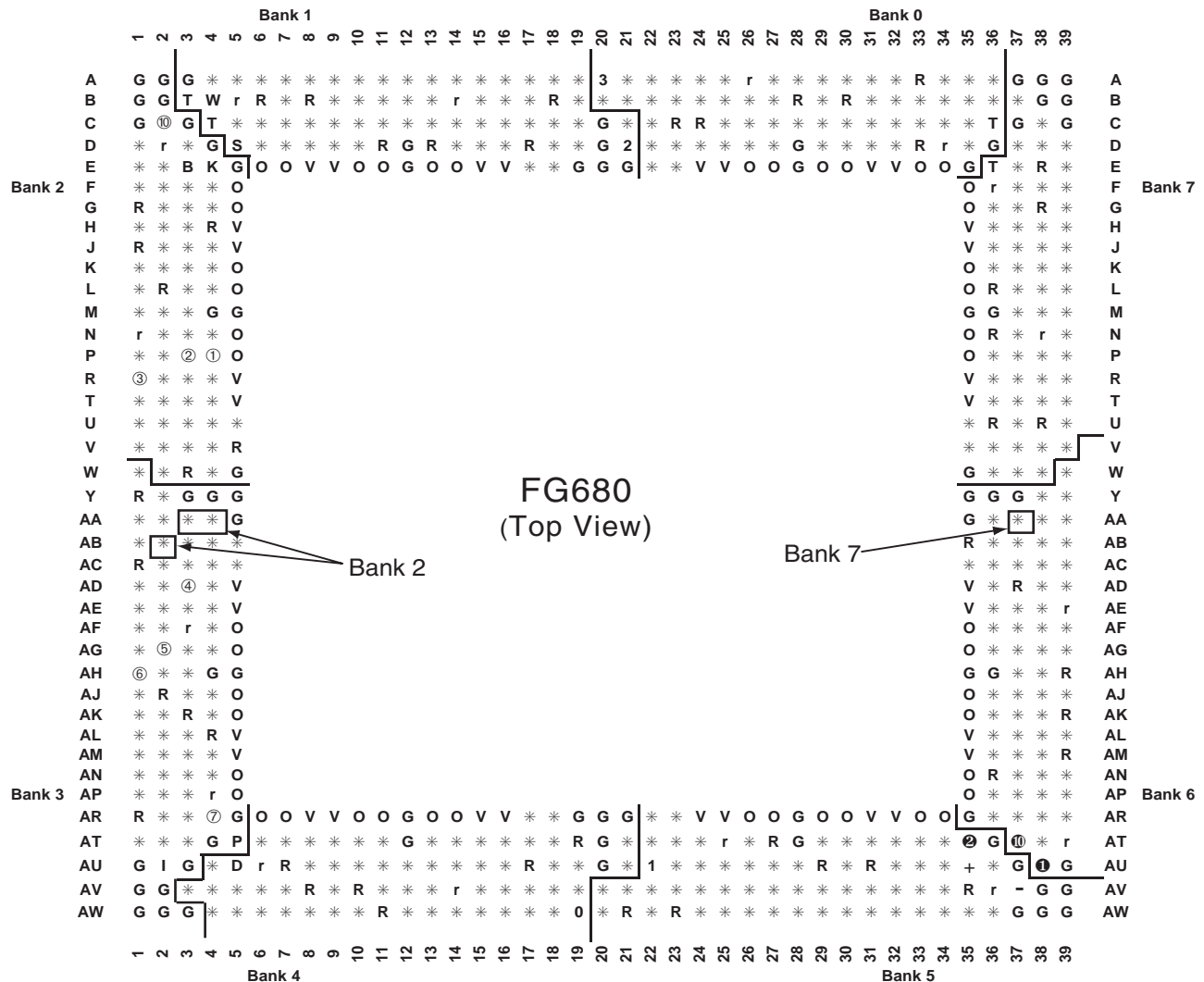
## FG456 (Top view)

Figure 9: FG456 Pin Function Diagram

### Notes:

Packages FG456 and FG676 are layout compatible.

# FG680 Pin Function Diagram



Note: AA3, AA4, and AB2 are in Bank 2

Note: AA37 is in Bank 7

fg680\_12a

Figure 11: FG680 Pin Function Diagram

## Revision History

Date	Version	Revision
11/98	1.0	Initial Xilinx release.
01/99-02/99	1.2-1.3	Both versions updated package drawings and specs.
05/99	1.4	Addition of package drawings and specifications.
05/99	1.5	Replaced FG 676 & FG680 package drawings.
07/99	1.6	Changed Boundary Scan Information and changed Figure 11, Boundary Scan Bit Sequence. Updated IOB Input & Output delays. Added Capacitance info for different I/O Standards. Added 5 V tolerant information. Added DLL Parameters and waveforms and new Pin-to-pin Input and Output Parameter tables for Global Clock Input to Output and Setup and Hold. Changed Configuration Information including Figures 12, 14, 17 & 19. Added device-dependent listings for quiescent currents ICCINTQ and ICCOQ. Updated IOB Input and Output Delays based on default standard of LVTTTL, 12 mA, Fast Slew Rate. Added IOB Input Switching Characteristics Standard Adjustments.
09/99	1.7	Speed grade update to preliminary status, Power-on specification and Clock-to-Out Minimums additions, "0" hold time listing explanation, quiescent current listing update, and Figure 6 ADDRA input label correction. Added $T_{IJITCC}$ parameter, changed $T_{OJIT}$ to $T_{OPHASE}$ .
01/00	1.8	Update to speed.txt file 1.96. Corrections for CRs 111036, 111137, 112697, 115479, 117153, 117154, and 117612. Modified notes for Recommended Operating Conditions (voltage and temperature). Changed Bank information for $V_{CCO}$ in CS144 package on p.43.
01/00	1.9	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.
03/00	2.0	New TBCKO values; corrected FG680 package connection drawing; new note about status of CCLK pin after configuration.
05/00	2.1	Modified "Pins not listed..." statement. Speed grade update to Final status.
05/00	2.2	Modified Table 18.
09/00	2.3	<ul style="list-style-type: none"> <li>Added XCV400 values to table under <b>Minimum Clock-to-Out for Virtex Devices</b>.</li> <li>Corrected Units column in table under <b>IOB Input Switching Characteristics</b>.</li> <li>Added values to table under <b>CLB SelectRAM Switching Characteristics</b>.</li> </ul>
10/00	2.4	<ul style="list-style-type: none"> <li>Corrected pinout info for devices in the BG256, BG432, and BG560 pkgs in Table 18.</li> <li>Corrected <b>BG256 Pin Function Diagram</b>.</li> </ul>
04/02/01	2.5	<ul style="list-style-type: none"> <li>Revised minimums for <b>Global Clock Set-Up and Hold for LVTTTL Standard, with DLL</b>.</li> <li>Converted file to modularized format. See section <b>Virtex Data Sheet</b>, below.</li> </ul>
04/19/01	2.6	<ul style="list-style-type: none"> <li>Corrected pinout information for FG676 device in <b>Table 4</b>. (Added AB22 pin.)</li> </ul>
07/19/01	2.7	<ul style="list-style-type: none"> <li>Clarified <math>V_{CCINT}</math> pinout information and added AE19 pin for BG352 devices in <b>Table 3</b>.</li> <li>Changed pinouts listed for BG352 XCV400 devices in banks 0 thru 7.</li> </ul>
07/19/02	2.8	<ul style="list-style-type: none"> <li>Changed pinouts listed for GND in TQ144 devices (see <b>Table 2</b>).</li> </ul>
03/01/13	4.0	The products listed in this data sheet are obsolete. See <b>XCN10016</b> for further information.

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- DS003-4, Virtex 2.5V FPGAs:  
Pinout Tables (Module 4)