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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	4704
Number of Logic Elements/Cells	21168
Total RAM Bits	114688
Number of I/O	512
Number of Gates	888439
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	680-LBGA Exposed Pad
Supplier Device Package	680-FTEBGA (40x40)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xcv800-6fg680c">https://www.e-xfl.com/product-detail/xilinx/xcv800-6fg680c</a>

### Virtex Device/Package Combinations and Maximum I/O

Table 3: Virtex Family Maximum User I/O by Device/Package (Excluding Dedicated Clock Pins)

Package	XCV50	XCV100	XCV150	XCV200	XCV300	XCV400	XCV600	XCV800	XCV1000
CS144	94	94							
TQ144	98	98							
PQ240	166	166	166	166	166				
HQ240						166	166	166	
BG256	180	180	180	180					
BG352			260	260	260				
BG432					316	316	316	316	
BG560						404	404	404	404
FG256	176	176	176	176					
FG456			260	284	312				
FG676						404	444	444	
FG680							512	512	512

### Virtex Ordering Information



Figure 1: Virtex Ordering Information

Each block SelectRAM cell, as illustrated in Figure 6, is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

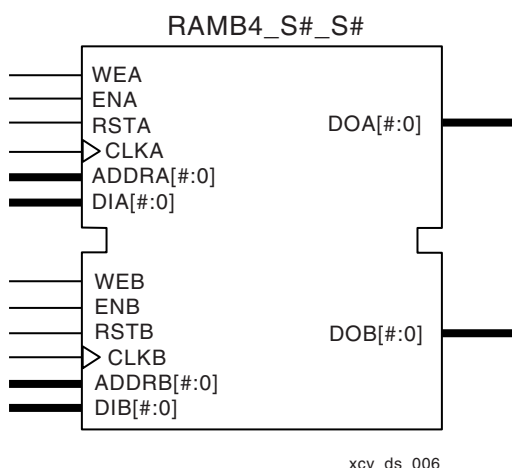


Figure 6: Dual-Port Block SelectRAM

Table 4 shows the depth and width aspect ratios for the block SelectRAM.

Table 4: Block SelectRAM Port Aspect Ratios

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

The Virtex block SelectRAM also includes dedicated routing to provide an efficient interface with both CLBs and other block SelectRAMs. Refer to XAPP130 for block SelectRAM timing waveforms.

## Programmable Routing Matrix

It is the longest delay path that limits the speed of any worst-case design. Consequently, the Virtex routing architecture and its place-and-route software were defined in a single optimization process. This joint optimization minimizes long-path delays, and consequently, yields the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.



Figure 7: Virtex Local Routing

## Local Routing

The VersaBlock provides local routing resources, as shown in Figure 7, providing the following three types of connections.

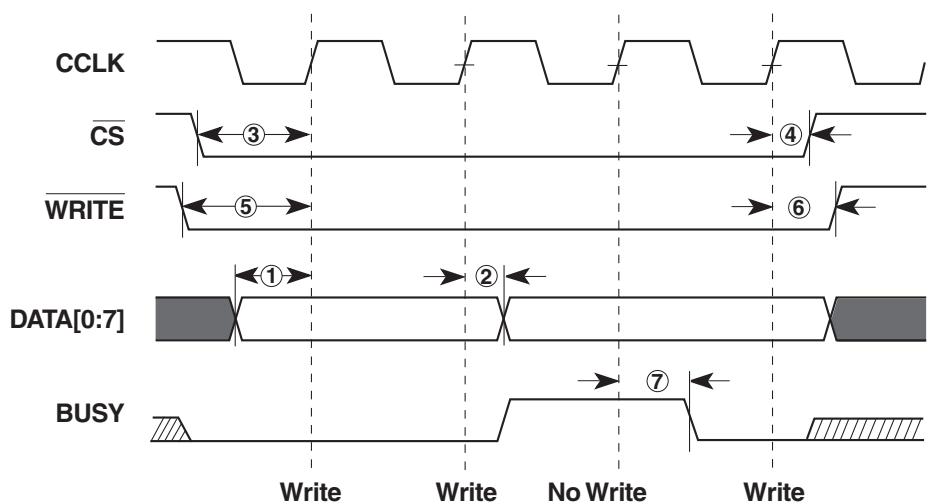
- Interconnections among the LUTs, flip-flops, and GRM

- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM.

3. At the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this has happened.
4. Repeat steps 2 and 3 until all the data has been sent.

5. De-assert  $\overline{\text{CS}}$  and  $\overline{\text{WRITE}}$ .

A flowchart for the write operation appears in [Figure 17](#). Note that if CCLK is slower than  $f_{\text{CCNH}}$ , the FPGA never asserts BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.



ds003\_16\_071902

Figure 16: Write Operations

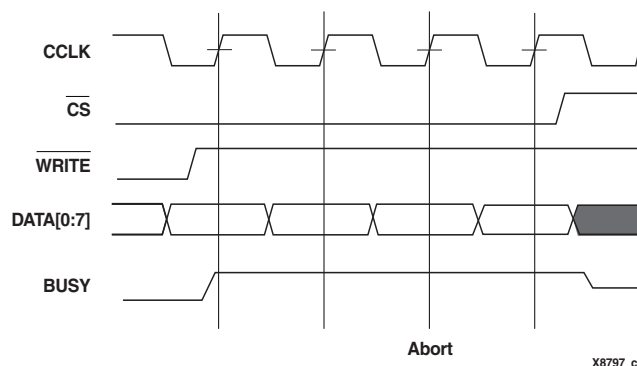


Figure 18: SelectMAP Write Abort Waveforms

## Boundary-Scan Mode

In the boundary-scan mode, configuration is done through the IEEE 1149.1 Test Access Port. Note that the **PROGRAM** pin must be pulled High prior to reconfiguration. A Low on the **PROGRAM** pin resets the TAP controller and no JTAG operations can be performed.

Configuration through the TAP uses the **CFG\_IN** instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port (when using TCK as a start-up clock).

1. Load the **CFG\_IN** instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the **JSTART** instruction into IR
6. Enter the SDR state
7. Clock TCK through the startup sequence
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode is selected by a <101> or 001> on the mode pins (M2, M1, M0). For details on TAP characteristics, refer to XAPP139.

## Configuration Sequence

The configuration of Virtex devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user, as described below. The configuration process can also be initiated by asserting **PROGRAM**.

The end of the memory-clearing phase is signalled by **INIT** going High, and the completion of the entire process is signalled by **DONE** going High.

The power-up timing of configuration signals is shown in Figure 19. The corresponding timing characteristics are listed in Table 10.

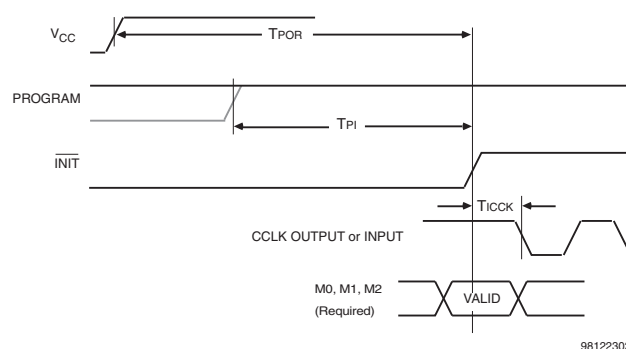


Figure 19: Power-Up Timing Configuration Signals

Table 10: Power-up Timing Characteristics

Description	Symbol	Value	Units
Power-on Reset	T <sub>POR</sub>	2.0	ms, max
Program Latency	T <sub>PL</sub>	100.0	μs, max
CCLK (output) Delay	T <sub>ICCK</sub>	0.5	μs, min
		4.0	μs, max
Program Pulse Width	T <sub>PROGRAM</sub>	300	ns, min

## Delaying Configuration

**INIT** can be held Low using an open-drain driver. An open-drain is required since **INIT** is a bidirectional open-drain pin that is held Low by the FPGA while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

## Start-Up Sequence

The default Start-up sequence is that one CCLK cycle after **DONE** goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed. In addition, the GTS, GSR, and GWE events can be made dependent on the **DONE** pins of multiple devices all going High, forcing the devices to start in synchronism. The sequence can also be paused at any stage until lock has been achieved on any or all DLLs.

### Virtex Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation net list. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Virtex devices unless otherwise noted.

### IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTTL levels. For other standards, adjust the delays with the values shown in , page 6.

Description	Device	Symbol	Speed Grade				Units
			Min	-6	-5	-4	
Propagation Delays							
Pad to I output, no delay	All	T <sub>IOPI</sub>	0.39	0.8	0.9	1.0	ns, max
Pad to I output, with delay	XCV50	T <sub>IOPID</sub>	0.8	1.5	1.7	1.9	ns, max
	XCV100		0.8	1.5	1.7	1.9	ns, max
	XCV150		0.8	1.5	1.7	1.9	ns, max
	XCV200		0.8	1.5	1.7	1.9	ns, max
	XCV300		0.8	1.5	1.7	1.9	ns, max
	XCV400		0.9	1.8	2.0	2.3	ns, max
	XCV600		0.9	1.8	2.0	2.3	ns, max
	XCV800		1.1	2.1	2.4	2.7	ns, max
	XCV1000		1.1	2.1	2.4	2.7	ns, max
Pad to output IQ via transparent latch, no delay	All	T <sub>IOPLI</sub>	0.8	1.6	1.8	2.0	ns, max
Pad to output IQ via transparent latch, with delay	XCV50	T <sub>IOPLID</sub>	1.9	3.7	4.2	4.8	ns, max
	XCV100		1.9	3.7	4.2	4.8	ns, max
	XCV150		2.0	3.9	4.3	4.9	ns, max
	XCV200		2.0	4.0	4.4	5.1	ns, max
	XCV300		2.0	4.0	4.4	5.1	ns, max
	XCV400		2.1	4.1	4.6	5.3	ns, max
	XCV600		2.1	4.2	4.7	5.4	ns, max
	XCV800		2.2	4.4	4.9	5.6	ns, max
	XCV1000		2.3	4.5	5.1	5.8	ns, max
Sequential Delays							
Clock CLK	All						
Minimum Pulse Width, High		T <sub>CH</sub>	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low		T <sub>CL</sub>	0.8	1.5	1.7	2.0	ns, min
Clock CLK to output IQ		T <sub>IOCKIQ</sub>	0.2	0.7	0.7	0.8	ns, max

Description	Device	Symbol	Speed Grade				Units
			Min	-6	-5	-4	
Setup and Hold Times with respect to Clock CLK at IOB input register <sup>(1)</sup>			Setup Time / Hold Time				
Pad, no delay	All	T <sub>IOPICK</sub> /T <sub>IOICKP</sub>	0.8 / 0	1.6 / 0	1.8 / 0	2.0 / 0	ns, min
Pad, with delay	XCV50	T <sub>IOPICKD</sub> /T <sub>IOICKPD</sub>	1.9 / 0	3.7 / 0	4.1 / 0	4.7 / 0	ns, min
	XCV100		1.9 / 0	3.7 / 0	4.1 / 0	4.7 / 0	ns, min
	XCV150		1.9 / 0	3.8 / 0	4.3 / 0	4.9 / 0	ns, min
	XCV200		2.0 / 0	3.9 / 0	4.4 / 0	5.0 / 0	ns, min
	XCV300		2.0 / 0	3.9 / 0	4.4 / 0	5.0 / 0	ns, min
	XCV400		2.1 / 0	4.1 / 0	4.6 / 0	5.3 / 0	ns, min
	XCV600		2.1 / 0	4.2 / 0	4.7 / 0	5.4 / 0	ns, min
	XCV800		2.2 / 0	4.4 / 0	4.9 / 0	5.6 / 0	ns, min
	XCV1000		2.3 / 0	4.5 / 0	5.0 / 0	5.8 / 0	ns, min
ICE input	All	T <sub>IOICECK</sub> /T <sub>IOCKICE</sub>	0.37/ 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, max
Set/Reset Delays							
SR input (IFF, synchronous)	All	T <sub>IOSRCKI</sub>	0.49	1.0	1.1	1.3	ns, max
SR input to IQ (asynchronous)	All	T <sub>IOSRIQ</sub>	0.70	1.4	1.6	1.8	ns, max
GSR to output IQ	All	T <sub>GSRQ</sub>	4.9	9.7	10.9	12.5	ns, max

**Notes:**

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. Input timing for LVTTTL is measured at 1.4 V. For other I/O standards, see [Table 3](#).

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Clock CLK to Pad delay with OBUFT enabled (non-3-state)	$T_{IOCKP}$	1.0	2.9	3.2	3.5	ns, max
Clock CLK to Pad high-impedance (synchronous) <sup>(1)</sup>	$T_{IOCKHZ}$	1.1	2.3	2.5	2.9	ns, max
Clock CLK to valid data on Pad delay, plus enable delay for OBUFT	$T_{IOCKON}$	1.5	3.4	3.7	4.1	ns, max
<b>Setup and Hold Times before/after Clock CLK<sup>(2)</sup></b>		<b>Setup Time / Hold Time</b>				
O input	$T_{IOOCK}/T_{IOCKO}$	0.51 / 0	1.1 / 0	1.2 / 0	1.3 / 0	ns, min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$	0.37 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
SR input (OFF)	$T_{IOSRCKO}/T_{IOCKOSR}$	0.52 / 0	1.1 / 0	1.2 / 0	1.4 / 0	ns, min
3-State Setup Times, T input	$T_{IOTCK}/T_{IOCKT}$	0.34 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$	0.41 / 0	0.9 / 0	0.9 / 0	1.1 / 0	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$	0.49 / 0	1.0 / 0	1.1 / 0	1.3 / 0	ns, min
<b>Set/Reset Delays</b>						
SR input to Pad (asynchronous)	$T_{IOSRP}$	1.6	3.8	4.1	4.6	ns, max
SR input to Pad high-impedance (asynchronous) <sup>(1)</sup>	$T_{IOSRHZ}$	1.6	3.1	3.4	3.9	ns, max
SR input to valid data on Pad (asynchronous)	$T_{IOSRON}$	2.0	4.2	4.6	5.1	ns, max
GSR to Pad	$T_{IOGSRQ}$	4.9	9.7	10.9	12.5	ns, max

**Notes:**

1. 3-state turn-off delays should not be adjusted.
2. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.



## I/O Standard Global Clock Input Adjustments

Description	Symbol	Standard <sup>(1)</sup>	Speed Grade				Units
			Min	-6	-5	-4	
Data Input Delay Adjustments							
Standard-specific global clock input delay adjustments	T <sub>GPLVTTL</sub>	LVTTL	0	0	0	0	ns, max
	T <sub>GPLVCMOS2</sub>	LVC MOS2	−0.02	−0.04	−0.04	−0.05	ns, max
	T <sub>GP PCI33_3</sub>	PCI, 33 MHz, 3.3 V	−0.05	−0.11	−0.12	−0.14	ns, max
	T <sub>GP PCI33_5</sub>	PCI, 33 MHz, 5.0 V	0.13	0.25	0.28	0.33	ns, max
	T <sub>GP PCI66_3</sub>	PCI, 66 MHz, 3.3 V	−0.05	−0.11	−0.12	−0.14	ns, max
	T <sub>GPGTL</sub>	GTL	0.7	0.8	0.9	0.9	ns, max
	T <sub>GPGTLP</sub>	GTL+	0.7	0.8	0.8	0.8	ns, max
	T <sub>GPHSTL</sub>	HSTL	0.7	0.7	0.7	0.7	ns, max
	T <sub>GPSSTL2</sub>	SSTL2	0.6	0.52	0.51	0.50	ns, max
	T <sub>GPSSTL3</sub>	SSTL3	0.6	0.6	0.55	0.54	ns, max
	T <sub>GPCTT</sub>	CTT	0.7	0.7	0.7	0.7	ns, max
	T <sub>GPAGP</sub>	AGP	0.6	0.54	0.53	0.52	ns, max

**Notes:**

1. Input timing for GPLVTTL is measured at 1.4 V. For other I/O standards, see [Table 3](#).

## CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade				Units
		Min	-6	-5	-4	
Combinatorial Delays						
F operand inputs to X via XOR	T <sub>OPX</sub>	0.37	0.8	0.9	1.0	ns, max
F operand input to XB output	T <sub>OPXB</sub>	0.54	1.1	1.3	1.4	ns, max
F operand input to Y via XOR	T <sub>OPY</sub>	0.8	1.5	1.7	2.0	ns, max
F operand input to YB output	T <sub>OPYB</sub>	0.8	1.5	1.7	2.0	ns, max
F operand input to COUT output	T <sub>OPCYF</sub>	0.6	1.2	1.3	1.5	ns, max
G operand inputs to Y via XOR	T <sub>OPGY</sub>	0.46	1.0	1.1	1.2	ns, max
G operand input to YB output	T <sub>OPGYB</sub>	0.8	1.6	1.8	2.1	ns, max
G operand input to COUT output	T <sub>OPCYG</sub>	0.7	1.3	1.4	1.6	ns, max
BX initialization input to COUT	T <sub>BXCY</sub>	0.41	0.9	1.0	1.1	ns, max
CIN input to X output via XOR	T <sub>CINX</sub>	0.21	0.41	0.46	0.53	ns, max
CIN input to XB	T <sub>CINXB</sub>	0.02	0.04	0.05	0.06	ns, max
CIN input to Y via XOR	T <sub>CINY</sub>	0.23	0.46	0.52	0.6	ns, max
CIN input to YB	T <sub>CINYB</sub>	0.23	0.45	0.51	0.6	ns, max
CIN input to COUT output	T <sub>BYP</sub>	0.05	0.09	0.10	0.11	ns, max
Multiplier Operation						
F1/2 operand inputs to XB output via AND	T <sub>FANDXB</sub>	0.18	0.36	0.40	0.46	ns, max
F1/2 operand inputs to YB output via AND	T <sub>FANDYB</sub>	0.40	0.8	0.9	1.1	ns, max
F1/2 operand inputs to COUT output via AND	T <sub>FANDCY</sub>	0.22	0.43	0.48	0.6	ns, max
G1/2 operand inputs to YB output via AND	T <sub>GANDYB</sub>	0.25	0.50	0.6	0.7	ns, max
G1/2 operand inputs to COUT output via AND	T <sub>GANDCY</sub>	0.07	0.13	0.15	0.17	ns, max
Setup and Hold Times before/after Clock CLK <sup>(1)</sup>	Setup Time / Hold Time					
CIN input to FFX	T <sub>CCKX</sub> /T <sub>CKCX</sub>	0.50 / 0	1.0 / 0	1.2 / 0	1.3 / 0	ns, min
CIN input to FFY	T <sub>CCKY</sub> /T <sub>CKCY</sub>	0.53 / 0	1.1 / 0	1.2 / 0	1.4 / 0	ns, min

### Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

### Virtex Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

#### Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL

Description	Symbol	Device	Speed Grade				Units
			Min	-6	-5	-4	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, <i>with</i> DLL. For data <i>output</i> with different standards, adjust delays with the values shown in Output Delay Adjustments.	T <sub>ICKOFDLL</sub>	XCV50	1.0	3.1	3.3	3.6	ns, max
		XCV100	1.0	3.1	3.3	3.6	ns, max
		XCV150	1.0	3.1	3.3	3.6	ns, max
		XCV200	1.0	3.1	3.3	3.6	ns, max
		XCV300	1.0	3.1	3.3	3.6	ns, max
		XCV400	1.0	3.1	3.3	3.6	ns, max
		XCV600	1.0	3.1	3.3	3.6	ns, max
		XCV800	1.0	3.1	3.3	3.6	ns, max
		XCV1000	1.0	3.1	3.3	3.6	ns, max

#### Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see [Table 2](#) and [Table 3](#).
3. DLL output jitter is already included in the timing calculation.

#### Global Clock Input-to-Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL

Description	Symbol	Device	Speed Grade				Units
			Min	-6	-5	-4	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, <i>without</i> DLL. For data <i>output</i> with different standards, adjust delays with the values shown in Input and Output Delay Adjustments. For I/O standards requiring V <sub>REF</sub> such as GTL, GTL+, SSTL, HSTL, CTT, and AGO, an additional 600 ps must be added.	T <sub>ICKOF</sub>	XCV50	1.5	4.6	5.1	5.7	ns, max
		XCV100	1.5	4.6	5.1	5.7	ns, max
		XCV150	1.5	4.7	5.2	5.8	ns, max
		XCV200	1.5	4.7	5.2	5.8	ns, max
		XCV300	1.5	4.7	5.2	5.9	ns, max
		XCV400	1.5	4.8	5.3	6.0	ns, max
		XCV600	1.6	4.9	5.4	6.0	ns, max
		XCV800	1.6	4.9	5.5	6.2	ns, max
		XCV1000	1.7	5.0	5.6	6.3	ns, max

#### Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see [Table 2](#) and [Table 3](#).

### DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Description	Symbol	Speed Grade						Units
		-6		-5		-4		
		Min	Max	Min	Max	Min	Max	
Input Clock Frequency (CLKDLLHF)	FCLKINHF	60	200	60	180	60	180	MHz
Input Clock Frequency (CLKDLL)	FCLKINLF	25	100	25	90	25	90	MHz
Input Clock Pulse Width (CLKDLLHF)	T <sub>DLLPWHF</sub>	2.0	-	2.4	-	2.4	-	ns
Input Clock Pulse Width (CLKDLL)	T <sub>DLLPWLF</sub>	2.5	-	3.0		3.0	-	ns

#### Notes:

1. All specifications correspond to Commercial Operating Temperatures (0°C to +85°C).

### DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

Description	Symbol	F <sub>CLKIN</sub>	CLKDLLHF		CLKDLL		Units
			Min	Max	Min	Max	
Input Clock Period Tolerance	T <sub>IP</sub> TOL		-	1.0	-	1.0	ns
Input Clock Jitter Tolerance (Cycle to Cycle)	T <sub>IJ</sub> TCC		-	± 150	-	± 300	ps
Time Required for DLL to Acquire Lock	T <sub>LOCK</sub>	> 60 MHz	-	20	-	20	μs
		50 - 60 MHz	-	-	-	25	μs
		40 - 50 MHz	-	-	-	50	μs
		30 - 40 MHz	-	-	-	90	μs
		25 - 30 MHz	-	-	-	120	μs
Output Jitter (cycle-to-cycle) for any DLL Clock Output <sup>(1)</sup>	T <sub>OJ</sub> TCC			± 60		± 60	ps
Phase Offset between CLKIN and CLKO <sup>(2)</sup>	T <sub>PHIO</sub>			± 100		± 100	ps
Phase Offset between Clock Outputs on the DLL <sup>(3)</sup>	T <sub>PHOO</sub>			± 140		± 140	ps
Maximum Phase Difference between CLKIN and CLKO <sup>(4)</sup>	T <sub>PHIOM</sub>			± 160		± 160	ps
Maximum Phase Difference between Clock Outputs on the DLL <sup>(5)</sup>	T <sub>PHOOM</sub>			± 200		± 200	ps

#### Notes:

1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* Output Jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN and CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of Output Jitter and Phase Offset between any two DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).
6. All specifications correspond to Commercial Operating Temperatures (0°C to +85°C).



## Virtex™ 2.5 V Field Programmable Gate Arrays

DS003-4 (v4.0) March 1, 2013

Production Product Specification

### Virtex Pin Definitions

Table 1: Special Purpose Pins

Pin Name	Dedicated Pin	Direction	Description
GCK0, GCK1, GCK2, GCK3	Yes	Input	Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin: it is an input for SelectMAP and slave-serial modes, and output in master-serial mode. After configuration, it is input only, logic level = Don't Care.
PROGRAM	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output can be open drain.
INIT	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. The pin becomes a user I/O after configuration.
BUSY/ DOUT	No	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.  In bit-serial modes, DOUT provides header information to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In SelectMAP mode, D0 - D7 are configuration data pins. These pins become user I/Os after configuration unless the SelectMAP port is retained.  In bit-serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
WRITE	No	Input	In SelectMAP mode, the active-low Write Enable signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
CS	No	Input	In SelectMAP mode, the active-low Chip Select signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary-scan Test-Access-Port pins, as defined in IEEE 1149.1.
DXN, DXP	Yes	N/A	Temperature-sensing diode pins. (Anode: DXP, cathode: DXN)
V <sub>CCINT</sub>	Yes	Input	Power-supply pins for the internal core logic.
V <sub>CCO</sub>	Yes	Input	Power-supply pins for the output drivers (subject to banking rules)
V <sub>REF</sub>	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground

## Virtex Pinout Information

### Pinout Tables

See [www.xilinx.com](http://www.xilinx.com) for updates or additional pinout information. For convenience, [Table 2](#), [Table 3](#) and [Table 4](#) list the locations of special-purpose and power-supply pins. Pins not listed are either user I/Os or not connected, depending on the device/package combination. See the Pinout Diagrams starting on [page 17](#) for any pins not listed for a particular part/package combination.

*Table 2: Virtex Pinout Tables (Chip-Scale and QFP Packages)*

Pin Name	Device	CS144	TQ144	PQ/HQ240
GCK0	All	K7	90	92
GCK1	All	M7	93	89
GCK2	All	A7	19	210
GCK3	All	A6	16	213
M0	All	M1	110	60
M1	All	L2	112	58
M2	All	N2	108	62
CCLK	All	B13	38	179
PROGRAM	All	L12	72	122
DONE	All	M12	74	120
INIT	All	L13	71	123
BUSY/DOUT	All	C11	39	178
D0/DIN	All	C12	40	177
D1	All	E10	45	167
D2	All	E12	47	163
D3	All	F11	51	156
D4	All	H12	59	145
D5	All	J13	63	138
D6	All	J11	65	134
D7	All	K10	70	124
WRITE	All	C10	32	185
CS	All	D10	33	184
TDI	All	A11	34	183
TDO	All	A12	36	181
TMS	All	B1	143	2
TCK	All	C3	2	239
V <sub>CCINT</sub>	All	A9, B6, C5, G3, G12, M5, M9, N6	10, 15, 25, 57, 84, 94, 99, 126	16, 32, 43, 77, 88, 104, 137, 148, 164, 198, 214, 225

Table 2: Virtex Pinout Tables (Chip-Scale and QFP Packages) (Continued)

Pin Name	Device	CS144	TQ144	PQ/HQ240
<b>V<sub>REF</sub> Bank 3</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	H11, K12	60, 68	130, 144
	XCV100/150	... + J10	... + 66	... + 133
	XCV200/300	N/A	N/A	... + 126
	XCV400	N/A	N/A	... + 147
	XCV600	N/A	N/A	... + 132
	XCV800	N/A	N/A	... + 140
<b>V<sub>REF</sub> Bank 4</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	L8, L10	79, 87	97, 111
	XCV100/150	... + N10	... + 81	... + 108
	XCV200/300	N/A	N/A	... + 115
	XCV400	N/A	N/A	... + 94
	XCV600	N/A	N/A	... + 109
	XCV800	N/A	N/A	... + 101
<b>V<sub>REF</sub> Bank 5</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	L4, L6	96, 104	70, 84
	XCV100/150	... + N4	... + 102	... + 73
	XCV200/300	N/A	N/A	... + 66
	XCV400	N/A	N/A	... + 87
	XCV600	N/A	N/A	... + 72
	XCV800	N/A	N/A	... + 80

Table 2: Virtex Pinout Tables (Chip-Scale and QFP Packages) (Continued)

Pin Name	Device	CS144	TQ144	PQ/HQ240
<b>V<sub>REF</sub> Bank 6</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	H2, K1	116, 123	36, 50
	XCV100/150	... + J3	... + 118	... + 47
	XCV200/300	N/A	N/A	... + 54
	XCV400	N/A	N/A	... + 33
	XCV600	N/A	N/A	... + 48
	XCV800	N/A	N/A	... + 40
<b>V<sub>REF</sub> Bank 7</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	D4, E1	133, 140	9, 23
	XCV100/150	... + D2	... + 138	... + 12
	XCV200/300	N/A	N/A	... + 5
	XCV400	N/A	N/A	... + 26
	XCV600	N/A	N/A	... + 11
	XCV800	N/A	N/A	... + 19
<b>GND</b>	All	A1, B9, B11, C7, D5, E4, E11, F1, G10, J1, J12, L3, L5, L7, L9, N12	9, 18, 26, 35, 46, 54, 64, 75, 83, 91, 100, 111, 120, 129, 136, 144,	1, 8, 14, 22, 29, 37, 45, 51, 59, 69, 75, 83, 91, 98, 106, 112, 119, 129, 135, 143, 151, 158, 166, 172, 182, 190, 196, 204, 211, 219, 227, 233



*Table 3: Virtex Pinout Tables (BGA)*

Pin Name	Device	BG256	BG352	BG432	BG560
GCK0	All	Y11	AE13	AL16	AL17
GCK1	All	Y10	AF14	AK16	AJ17
GCK2	All	A10	B14	A16	D17
GCK3	All	B10	D14	D17	A17
M0	All	Y1	AD24	AH28	AJ29
M1	All	U3	AB23	AH29	AK30
M2	All	W2	AC23	AJ28	AN32
CCLK	All	B19	C3	D4	C4
PROGRAM	All	Y20	AC4	AH3	AM1
DONE	All	W19	AD3	AH4	AJ5
INIT	All	U18	AD2	AJ2	AH5
BUSY/DOUT	All	D18	E4	D3	D4
D0/DIN	All	C19	D3	C2	E4
D1	All	E20	G1	K4	K3
D2	All	G19	J3	K2	L4
D3	All	J19	M3	P4	P3
D4	All	M19	R3	V4	W4
D5	All	P19	U4	AB1	AB5
D6	All	T20	V3	AB3	AC4
D7	All	V19	AC3	AG4	AJ4
WRITE	All	A19	D5	B4	D6
CS	All	B18	C4	D5	A2
TDI	All	C17	B3	B3	D5
TDO	All	A20	D4	C4	E6
TMS	All	D3	D23	D29	B33
TCK	All	A1	C24	D28	E29
DXN	All	W3	AD23	AH27	AK29
DXP	All	V4	AE24	AK29	AJ28

Table 3: Virtex Pinout Tables (BGA) (Continued)

Pin Name	Device	BG256	BG352	BG432	BG560
<b>V<sub>CCINT</sub></b> <b>Notes:</b> <ul style="list-style-type: none"> <li>Superset includes all pins, including the ones in <b>bold</b> type. Subset excludes pins in <b>bold</b> type.</li> <li>In BG352, for XCV300 all the V<sub>CCINT</sub> pins in the superset must be connected. For XCV150/200, V<sub>CCINT</sub> pins in the subset must be connected, and pins in <b>bold</b> type can be left unconnected (these unconnected pins cannot be used as user I/O.)</li> <li>In BG432, for XCV400/600/800 all V<sub>CCINT</sub> pins in the superset must be connected. For XCV300, V<sub>CCINT</sub> pins in the subset must be connected, and pins in <b>bold</b> type can be left unconnected (these unconnected pins cannot be used as user I/O.)</li> <li>In BG560, for XCV800/1000 all V<sub>CCINT</sub> pins in the superset must be connected. For XCV400/600, V<sub>CCINT</sub> pins in the subset must be connected, and pins in <b>bold</b> type can be left unconnected (these unconnected pins cannot be used as user I/O.)</li> </ul>	XCV50/100	C10, D6, D15, F4, F17, L3, L18, R4, R17, U6, U15, V10	N/A	N/A	N/A
	XCV150/200/300	Same as above	A20, C14, D10, J24, K4, P2, P25, V24, W2, AC10, AE14, AE19, <b>B16, D12, L1, L25, R23, T1, AF11, AF16</b>	A10, A17, B23, C14, C19, K3, K29, N2, N29, T1, T29, W2, W31, AB2, AB30, AJ10, AJ16, AK13, AK19, AK22, <b>B26, C7, F1, F30, AE29, AF1, AH8, AH24</b>	N/A
	XCV400/600/800/1000	N/A	N/A	Same as above	A21, B14, B18, B28, C24, E9, E12, F2, H30, J1, K32, N1, N33, U5, U30, Y2, Y31, AD2, AD32, AG3, AG31, AK8, AK11, AK17, AK20, AL14, AL27, AN25, <b>B12, C22, M3, N29, AB2, AB32, AJ13, AL22</b>
V <sub>CCO</sub> , Bank 0	All	D7, D8	A17, B25, D19	A21, C29, D21	A22, A26, A30, B19, B32
V <sub>CCO</sub> , Bank 1	All	D13, D14	A10, D7, D13	A1, A11, D11	A10, A16, B13, C3, E5
V <sub>CCO</sub> , Bank 2	All	G17, H17	B2, H4, K1	C3, L1, L4	B2, D1, H1, M1, R2
V <sub>CCO</sub> , Bank 3	All	N17, P17	P4, U1, Y4	AA1, AA4, AJ3	V1, AA2, AD1, AK1, AL2
V <sub>CCO</sub> , Bank 4	All	U13, U14	AC8, AE2, AF10	AH11, AL1, AL11	AM2, AM15, AN4, AN8, AN12
V <sub>CCO</sub> , Bank 5	All	U7, U8	AC14, AC20, AF17	AH21, AJ29, AL21	AL31, AM21, AN18, AN24, AN30
V <sub>CCO</sub> , Bank 6	All	N4, P4	U26, W23, AE25	AA28, AA31, AL31	W32, AB33, AF33, AK33, AM32

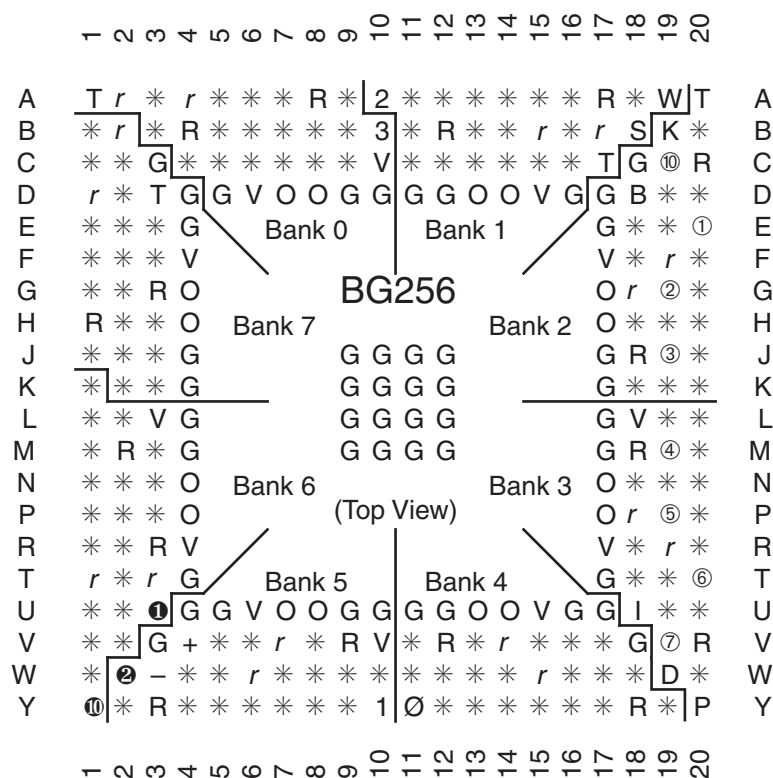
Table 3: Virtex Pinout Tables (BGA) (Continued)

Pin Name	Device	BG256	BG352	BG432	BG560
V <sub>CCO</sub> , Bank 7	All	G4, H4	G23, K26, N23	A31, L28, L31	C32, D33, K33, N32, T33
V <sub>REF</sub> Bank 0 (VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all VREF pins are general I/O.	XCV50	A8, B4	N/A	N/A	N/A
	XCV100/150	... + A4	A16, C19, C21	N/A	N/A
	XCV200/300	... + A2	... + D21	B19, D22, D24, D26	N/A
	XCV400	N/A	N/A	... + C18	A19, D20, D26, E23, E27
	XCV600	N/A	N/A	... + C24	... + E24
	XCV800	N/A	N/A	... + B21	... + E21
	XCV1000	N/A	N/A	N/A	... + D29
V <sub>REF</sub> Bank 1 (VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all VREF pins are general I/O.	XCV50	A17, B12	N/A	N/A	N/A
	XCV100/150	... + B15	B6, C9, C12	N/A	N/A
	XCV200/300	... + B17	... + D6	A13, B7, C6, C10	N/A
	XCV400	N/A	N/A	... + B15	A6, D7, D11, D16, E15
	XCV600	N/A	N/A	... + D10	... + D10
	XCV800	N/A	N/A	... + B12	... + D13
	XCV1000	N/A	N/A	N/A	... + E7
V <sub>REF</sub> Bank 2 (VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all VREF pins are general I/O.	XCV50	C20, J18	N/A	N/A	N/A
	XCV100/150	... + F19	E2, H2, M4	N/A	N/A
	XCV200/300	... + G18	... + D2	E2, G3, J2, N1	N/A
	XCV400	N/A	N/A	... + R3	G5, H4, L5, P4, R1
	XCV600	N/A	N/A	... + H1	... + K5
	XCV800	N/A	N/A	... + M3	... + N5
	XCV1000	N/A	N/A	N/A	... + B3

Table 4: Virtex Pinout Tables (Fine-Pitch BGA) (Continued)

Pin Name	Device	FG256	FG456	FG676	FG680
<b>V<sub>REF</sub> Bank 4</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	P9, T12	N/A	N/A	N/A
	XCV100/150	... + T11	AA13, AB16, AB19	N/A	N/A
	XCV200/300	... + R13	... + AB20	N/A	N/A
	XCV400	N/A	N/A	AC15, AD18, AD21, AD22, AF15	N/A
	XCV600	N/A	N/A	... + AF20	AT19, AU7, AU17, AV8, AV10, AW11
	XCV800	N/A	N/A	... + AF17	... + AV14
	XCV1000	N/A	N/A	N/A	... + AU6
<b>V<sub>REF</sub> Bank 5</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	T4, P8	N/A	N/A	N/A
	XCV100/150	... + R5	W8, Y10, AA5	N/A	N/A
	XCV200/300	... + T2	... + Y6	N/A	N/A
	XCV400	N/A	N/A	AA10, AB8, AB12, AC7, AF12	N/A
	XCV600	N/A	N/A	... + AF8	AT27, AU29, AU31, AV35, AW21, AW23
	XCV800	N/A	N/A	... + AE10	... + AT25
	XCV1000	N/A	N/A	N/A	... + AV36
<b>V<sub>REF</sub> Bank 6</b> (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V <sub>REF</sub> pins are general I/O.	XCV50	J3, N1	N/A	N/A	N/A
	XCV100/150	... + M1	N2, R4, T3	N/A	N/A
	XCV200/300	... + N2	... + Y1	N/A	N/A
	XCV400	N/A	N/A	AB3, R1, R4, U6, V5	N/A
	XCV600	N/A	N/A	... + Y1	AB35, AD37, AH39, AK39, AM39, AN36
	XCV800	N/A	N/A	... + U2	... + AE39
	XCV1000	N/A	N/A	N/A	... + AT39

## BG256 Pin Function Diagram



DS003\_18\_100300

Figure 4: BG256 Pin Function Diagram