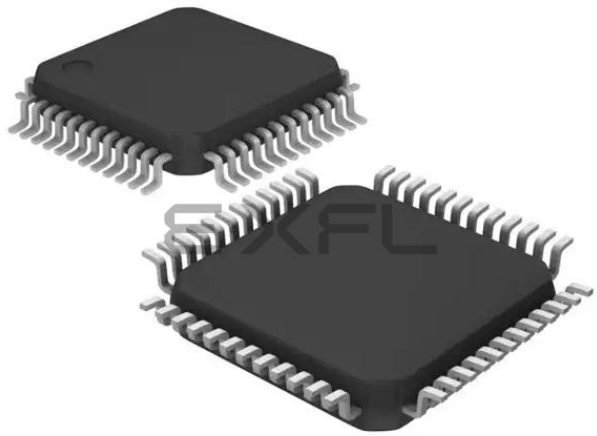

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	Flexcomm, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc51u68jbd48e

5. Block diagram

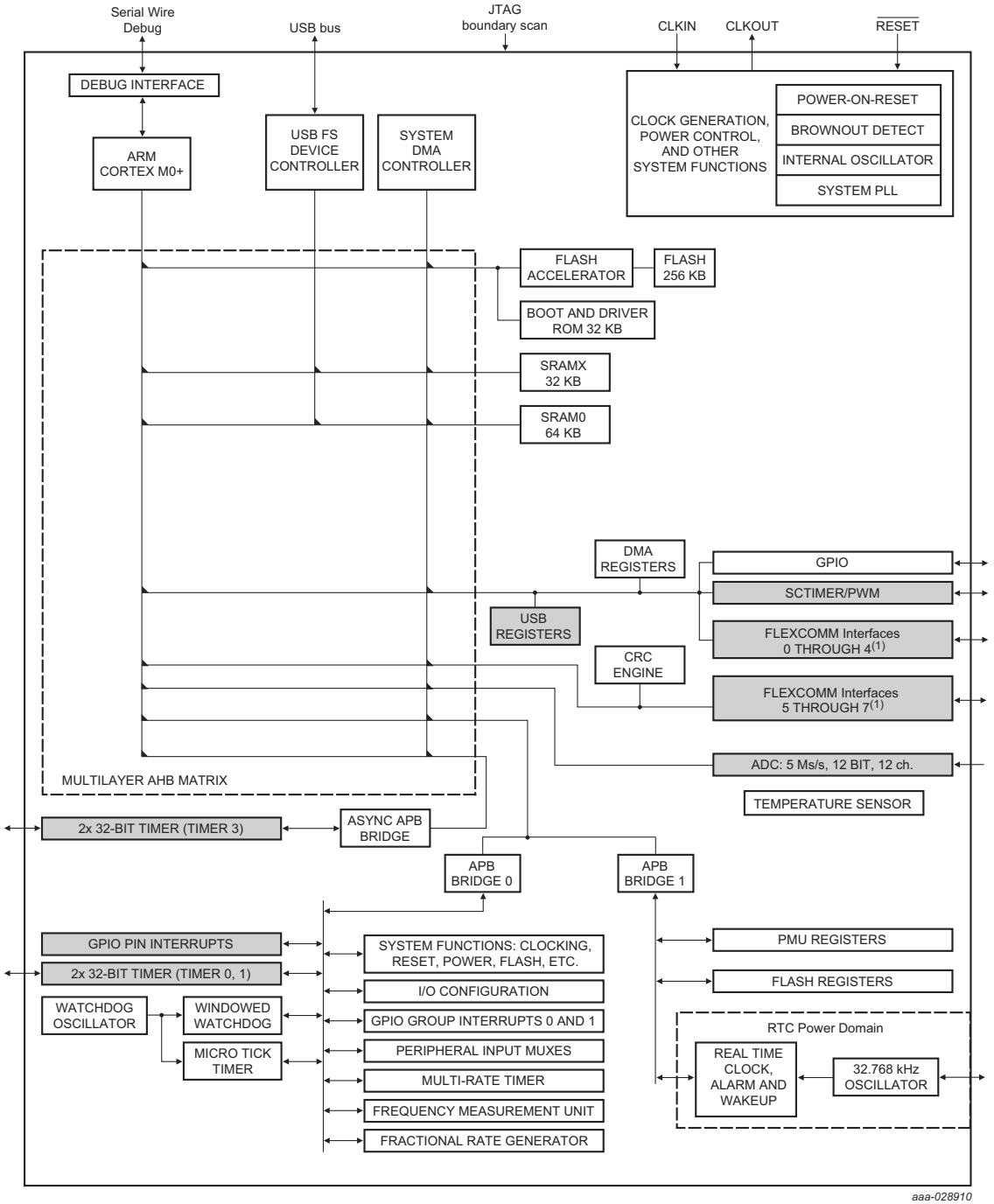


Fig 2. LPC51U68 Block diagram

6. Pinning information

6.1 Pinning

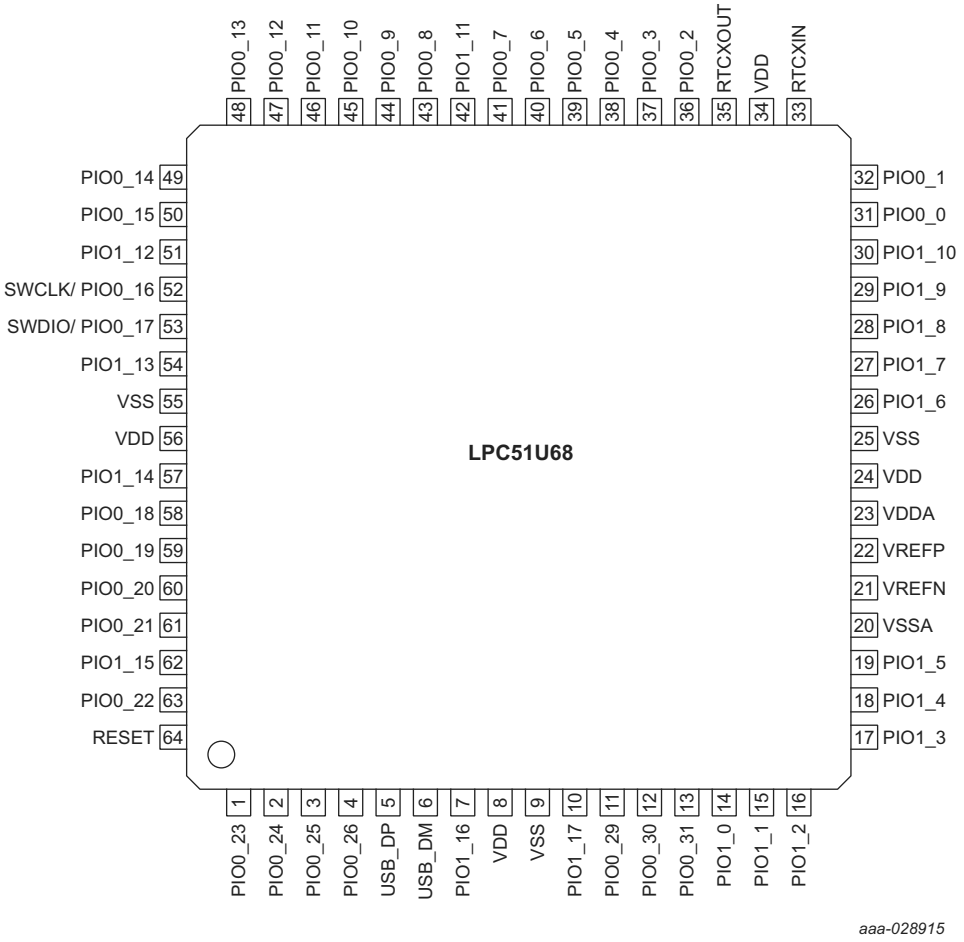


Fig 3. LQFP64 Pin configuration

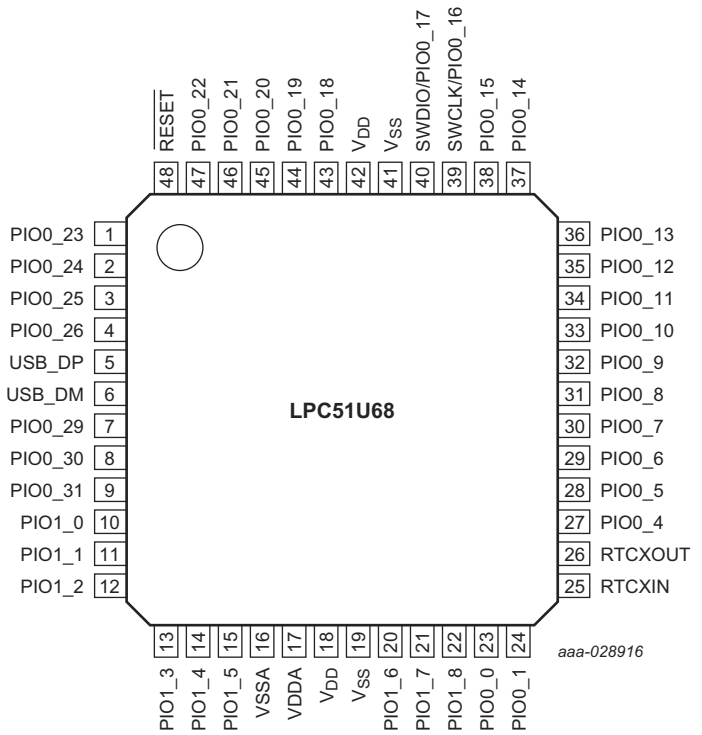


Fig 4. LQFP48 Pin configuration

Table 4. Pin description *…continued*

Symbol	64-pin	48-pin		Reset state [1]	Type	Description
PIO1_10	30	-	[2]	PU	I/O	**PIO1_10 —** General-purpose digital input/output pin.
						R — Reserved.
					I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm Interface 6: USART TXD, I2C SCL, SPI MISO, I2S WS.
					O	**SCT0_OUT4 —** SCT0 output 4. PWM output 4.
					I/O	**FC1_SCK —** Flexcomm Interface 1: USART or SPI clock.
						R — Reserved.
						R — Reserved.
					I	**USB_FRAME —** USB start-of-frame signal derived from host signaling.
PIO1_11	42	-	[2]	PU	I/O	**PIO1_11 —** General-purpose digital input/output pin.
						R — Reserved.
					I/O	**FC6_RTS_SCL_SSEL1 —** Flexcomm Interface 6: USART RTS, I2C SCL, SPI SSEL1.
					I	**CTimer1_CAP0 —** 32-bit CTimer1 capture input 0.
					I/O	**FC4_SCK —** Flexcomm Interface 4: USART or SPI clock.
						R — Reserved.
						R — Reserved.
					I	**USB_VBUS —** Monitors the presence of USB bus power. This signal must be HIGH for USB reset to occur.
PIO1_12	51	-	[2]	PU	I/O	**PIO1_12 —** General-purpose digital input/output pin.
						R — Reserved.
					I/O	**FC5_RXD_SDA_MOSI —** Flexcomm Interface 5: USART RXD, I2C SDA, SPI MOSI.
					O	**CTimer1_MAT0 —** 32-bit CTimer1 match output 0.
					I/O	**FC7_SCK —** Flexcomm Interface 7: USART, SPI, or I2S clock.
					I	**UTICK_CAP2 —** Micro-tick timer capture input 2.
PIO1_13	54	-	[2]	PU	I/O	**PIO1_13 —** General-purpose digital input/output pin.
						R — Reserved.
					I/O	**FC5_TXD_SCL_MISO —** Flexcomm Interface 5: USART TXD, I2C SCL, SPI MISO.
					O	**CTimer1_MAT1 —** 32-bit CTimer1 match output 1.
					I/O	**FC7_RXD_SDA_MOSI_DATA —** Flexcomm Interface 7: USART RXD, I2C SDA, SPI MOSI, I2S DATA.
PIO1_14	57	-	[2]	PU	I/O	**PIO1_14 —** General-purpose digital input/output pin.
						R — Reserved.
					I/O	**FC2_RXD_SDA_MOSI —** Flexcomm Interface 2: USART RXD, I2C SDA, SPI MOSI.
					O	**SCT0_OUT7 —** SCT0 output 7. PWM output 7.
					I/O	**FC7_TXD_SCL_MISO_WS —** Flexcomm Interface 7: USART TXD, I2C SCL, SPI MISO, I2S WS.

Table 4. Pin description *…continued*

Symbol	64-pin	48-pin		Reset state [1]	Type	Description
PIO1_15	62	-	[2]	PU	I/O	**PIO1_15 —** General-purpose digital input/output pin.
						R — Reserved.
					O	**SCT0_OUT5 —** SCT0 output 5. PWM output 5.
					I	**CTimer1_CAP3 —** 32-bit CTimer1 capture input 3.
					I/O	**FC7_CTS_SDA_SSEL0 —** Flexcomm Interface 7: USART CTS, I2C SDA, SPI SSEL0.
PIO1_16	7	-	[2]	PU	I/O	**PIO1_16 —** General-purpose digital input/output pin.
						R — Reserved.
					O	**CTimer0_MAT0 —** 32-bit CTimer0 match output 0.
					I	**CTimer0_CAP0 —** 32-bit CTimer0 capture input 0.
					I/O	**FC7_RTS_SCL_SSEL1 —** Flexcomm Interface 7: USART RTS, I2C SCL, SPI SSEL1.
PIO1_17	10	-	[2]	PU	I/O	**PIO1_17 —** General-purpose digital input/output pin.
						R — Reserved.
						R — Reserved.
						R — Reserved.
					I/O	**MCLK —** MCLK input or output for I2S and/or digital microphone.
					I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
USB_DP	5	5	[6]	F	I/O	USB0 bidirectional D+ line.
USB_DM	6	6	[6]	F	I/O	USB0 bidirectional D- line.
RESETN	64	48	[5]	PU	I	External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. Wakes up the part from deep power-down mode.
RTCXIN	33	25		-	-	RTC oscillator input.
RTCXOUT	35	26		-	-	RTC oscillator output.
VREFP	22	-		-	-	ADC positive reference voltage. On LQFP48, VREFP is internally tied to the VDDA pin.
VREFN	21	-		-	-	ADC negative reference voltage. On LQFP48, VREFN is internally tied to the VDDA pin.
V_{DDA}	23	17		-	-	Analog supply voltage.
V_{DD}	8, 24, 34, 56	18, 42		-	-	Single 1.62 V to 3.6 V power supply powers internal digital functions and I/Os.
V_{SS}	9, 25, 55	19, 41		-	-	Ground.
V_{SSA}	20	16		-	-	Analog ground.

- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator with auto-baud function.
- A fractional rate divider is shared among all USARTs.
- Interrupts available for FIFO receive level reached, FIFO transmit level reached, Transmit Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Loopback mode for testing of data and flow control.
- In synchronous slave mode, wakes up the part from deep-sleep mode.
- Special operating mode allows operation at up to 9600 baud using the 32.768 kHz RTC oscillator as the UART clock. This mode can be used while the device is in deep-sleep mode and can wake-up the device when a character is received.
- USART transmit and receive functions work with the system DMA controller.
- Activity on the USART synchronous slave mode allows wake-up from deep-sleep mode on any enabled interrupt

7.14.4 SPI serial I/O controller

7.14.4.1 Features

- Master and slave operation.
- Maximum data rate of 71 Mbit/s in master mode and 15 Mbit/s in slave mode for SPI functions.
- Data frames of 1 to 16 bits supported directly. Larger frames supported by software or DMA set-up.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data. This can be useful while setting up an SPI memory.
- Control information can optionally be written along with data. This allows very versatile operation, including “any length” frames.
- Four Slave Select input/outputs with selectable polarity and flexible usage.
- Activity on the SPI in slave mode allows wake-up from deep-sleep mode on any enabled interrupt.

  Remark: Texas Instruments SSI and National Microwire modes are not supported.

7.14.5 I^2C-bus interface

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example, an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.14.6 Features

- Independent Master, Slave, and Monitor functions.
- Bus speeds supported:

- The Watchdog clock (WDCLK) source is a selectable frequency in the range of 6 kHz to 1.5 MHz. The accuracy of this clock is limited to +/- 40% over temperature, voltage, and silicon processing variations.
- The Watchdog timer can be configured to run in deep-sleep mode.
- Debug mode.

7.15.4 RTC timer

The RTC block has two timers: main RTC timer, and high-resolution/wake-up timer. The main RTC timer is a 32-bit timer that uses a 1 Hz clock and is intended to run continuously as a real-time clock. When the timer value reaches a match value, an interrupt is raised. The alarm interrupt can also wake up the part from any low power mode, if enabled.

The high-resolution or wake-up timer is a 16-bit timer that uses a 1 kHz clock and operates as a one-shot down timer. When the timer is loaded, it starts counting down to 0 at which point an interrupt is raised. The interrupt can be used to wake-up the part from any low power modes. This timer is intended to be used for timed wake-up from deep-sleep or deep power-down modes. The high-resolution wake-up timer can be disabled to conserve power if not used.

The RTC timer uses the 32.768 kHz clock input to create a 1 Hz or 1 kHz clock.

7.15.4.1 Features

- The RTC oscillator has the following clock outputs:
  - 32.768 kHz clock, selectable for system clock and CLKOUT pin.
  - 1 Hz clock for RTC timing.
  - 1 kHz clock for high-resolution RTC timing.
- 32-bit, 1 Hz RTC counter and associated match register for alarm generation.
- Separate 16-bit high-resolution/wake-up timer clocked at 1 kHz for 1 ms resolution with a more that one minute maximum time-out period.
- RTC alarm and high-resolution/wake-up timer time-out each generate independent interrupt requests. Either time-out can wake up the part from any of the low power modes, including deep power-down.

7.15.5 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

7.15.5.1 Features

- 24-bit interrupt timer.
- Four channels independently counting down from individually set values.
- Repeat interrupt, one-shot interrupt, and one-shot bus stall modes.

7.15.6 Micro-tick timer (UTICK)

The ultra-low power Micro-tick Timer, running from the Watchdog oscillator, can be used to wake up the device from low power modes.

7.15.6.1 Features

- Ultra simple timer.
- Write once to start.
- Interrupt or software polling.
- Four capture registers that can be triggered by external pin transitions.

7.16 12-bit Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12-bit and fast conversion rates of up to 5.0 Msamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the SCTimer/PWM, external pins, and the ARM TXEV interrupt.

The ADC supports a variable clocking scheme with clocking synchronous to the system clock or independent, asynchronous clocking for high-speed conversions

The ADC includes a hardware threshold compare function with zero-crossing detection. The threshold crossing interrupt is connected internally to the SCTimer/PWM inputs for tight timing control between the ADC and the SCTimer/PWM.

7.16.1 Features

- 12-bit successive approximation analog to digital converter.
- Input multiplexing up to 12 pins.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and “zero crossing” detection.
- Measurement range V_{REFN} to V_{REFP} (not to exceed V_{DDA} voltage level).
- 12-bit conversion rate of 5.0 MHz. Options for reduced resolution at higher conversion rates.
- Burst conversion mode for single or multiple inputs.
- Synchronous or asynchronous operation. Asynchronous operation maximizes flexibility in choosing the ADC clock frequency, Synchronous mode minimizes trigger latency and can eliminate uncertainty and jitter in response to a trigger.
- A temperature sensor is connected as an alternative input for ADC channel 0.

7.17 Temperature sensor

The temperature sensor transducer uses an intrinsic pn-junction diode reference and outputs a Complement To Absolute Temperature (V_{CTAT}) voltage. The output voltage varies inversely with device temperature with an absolute accuracy of better than ±3 °C over the full temperature range (-40 °C to +105 °C). The temperature sensor is only approximately linear with a slight curvature. The output voltage is measured over different ranges of temperatures and fit with linear-least-square lines.

Table 19. Typical AHB/APB peripheral power consumption [3][4][5]

T_{amb} = 25 °C, V_{DD} = 3.3 V;

Peripheral		I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz
CTimer0		0.52	0.50	0.50
CTimer1		0.39	0.46	0.47
Fractional Rate Generator		0.46	0.44	0.44
Async APB peripheral		**CPU: 12 MHz, Async APB bus: 12 MHz**	**CPU: 48 MHz, sync APB bus: 12 MHz[2]**	**CPU: 96MHz, Async APB bus: 12 MHz[2]**
CTimer3		0.36	0.36	0.36

[1] Turn off the peripheral when the configuration is done.

[2] For optimal system power consumption, use fixed low frequency Async APB bus when the CPU is at a higher frequency.

[3] The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using ASYNCAPBCLKCTRL, AHBCLKCTRL0/1, and PDRUNCFG0 registers. All other blocks are disabled and no code accessing the peripheral is executed.

[4] The supply currents are shown for system clock frequencies of 12 MHz, 48 MHz, and 96 MHz.

[5] Typical ratings are not guaranteed. Characterized through bench measurements using typical samples.

10.4 Pin characteristics

Table 20. Static characteristics: pin characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.62 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$\overline{\text{RESET}}$ pin							
V_{IH}	HIGH-level input voltage			0.8 × V_{DD}	-	5.0	V
V_{IL}	LOW-level input voltage			−0.5	-	0.3 × V_{DD}	V
V_{hys}	hysteresis voltage		[1][14]	0.05 × V_{DD}	-	-	V
Standard I/O pins							
Input characteristics							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled.		-	3.0	180	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; V_{DD} = 3.6 V; for RESETN pin.			3.0	180	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	3.0	180	nA
V_I	input voltage	pin configured to provide a digital function;	[3]				
		V_{DD} > 1.8 V		0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_{IH}	HIGH-level input voltage	1.62 V ≤ V_{DD} < 2.7 V		1.5	-	5.0	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		2.0	-	5.0	V
V_{IL}	LOW-level input voltage	1.62 V ≤ V_{DD} < 2.7 V		−0.5	-	+0.4	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		−0.5	-	+0.8	V
V_{hys}	hysteresis voltage		[14]	0.1 × V_{DD}	-	-	V

Table 20. Static characteristics: pin characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.62 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Output characteristics							
V_O	output voltage	output active		0	-	V_{DD}	V
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/pull-down resistors disabled		-	3	180	nA
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA; 1.62 V ≤ V_{DD} < 2.7 V		V_{DD} − 0.4	-	-	V
		I_{OH} = −6 mA; 2.7 V ≤ V_{DD} ≤ 3.6 V		V_{DD} − 0.4			
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; 1.62 V ≤ V_{DD} < 2.7 V		-	-	0.4	V
		I_{OL} = 6 mA; 2.7 V ≤ V_{DD} ≤3.6 V		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 1.62 V ≤ V_{DD} < 2.7 V		4.0	-	-	mA
		V_{OH} = V_{DD} − 0.4 V; 2.7 V ≤ V_{DD} ≤ 3.6 V		6.0	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; 1.62 V ≤ V_{DD} < 2.7 V		4.0	-	-	mA
		V_{OL} = 0.4 V; 2.7 V ≤ V_{DD} ≤ 3.6 V		6.0	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	1.62 V ≤ V_{DD} < 2.7 V	[2][4]	-	-	35	mA
	drive HIGH; connected to ground;	2.7 V ≤ V_{DD} ≤ 3.6 V		-	-	87	mA
I_{OLS}	LOW-level short-circuit output current	1.62 V ≤ V_{DD} < 2.7 V	[2][4]	-	-	30	mA
	drive LOW; connected to V_{DD}	2.7 V ≤ V_{DD} ≤ 3.6 V		-	-	77	mA
Weak input pull-up/pull-down characteristics							
I_{pd}	pull-down current	V_I = V_{DD}		25		80	μA
		V_I = 5 V	[2]	80		100	μA
I_{pu}	pull-up current	V_I = 0 V		−25		−80	μA
		V_{DD} < V_I < 5 V	[2][7]	6		30	μA
Open-drain I^2C pins							
V_{IH}	HIGH-level input voltage	1.62 V ≤ V_{DD} < 2.7 V		0.7 × V_{DD}	-	-	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		0.7 × V_{DD}	-	-	V
V_{IL}	LOW-level input voltage	1.62 V ≤ V_{DD} < 2.7 V		0	-	0.3 × V_{DD}	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		0	-	0.3 × V_{DD}	V
V_{hys}	hysteresis voltage			0.1 × V_{DD}	-	-	V
I_{LI}	input leakage current	V_I = V_{DD}	[5]	-	2.5	3.5	μA
		V_I = 5 V		-	5.5	10	μA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; pin configured for standard mode or fast mode		4.0	-	-	mA
		V_{OL} = 0.4V; pin configured for Fast-mode Plus		20	-	-	mA

Table 20. Static characteristics: pin characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.62 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
USB_DM and USB_DP pins							
V_I	input voltage			0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
Z_{out}	output impedance		[11]	33.0	-	44	Ω
V_{OH}	HIGH-level output voltage		[12]	2.8	-	-	V
V_{OL}	LOW-level output voltage		[13]	-	-	0.3	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.3$ V	[9][10]	38	-	74	mA
		$V_{OH} = V_{DD} - 0.3$ V	[10][11]	6.0		9.0	mA
I_{OL}	LOW-level output current	V_{OL} = 0.3 V	[9][10]	38	-	74	mA
		V_{OL} = 0.3 V	[10][11]	6.0		9.0	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; pad connected to ground	[10]	-	-	100	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; pad connected to ground	[10]	-	-	100	mA
Pin capacitance							
C_{io}	input/output capacitance	I^2C-bus pins	[8]	-	-	6.0	pF
		pins with digital functions only	[6]	-	-	2.0	pF
		Pins with digital and analog functions	[6]	-	-	7.0	pF

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltage.

[2] Based on characterization. Not tested in production.

[3] With respect to ground.

[4] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[5] To V_{SS}.

[6] The values specified are simulated and absolute values, including package/bondwire capacitance.

[7] The weak pull-up resistor is connected to the V_{DD} rail and pulls up the I/O pin to the V_{DD} level.

[8] The value specified is a simulated value, excluding package/bondwire capacitance.

[9] Without 33 Ω ± 2 % series external resistor.

[10] The parameter values specified are simulated and absolute values.

[11] With 33 Ω ± 2 % series external resistor.

[12] With 15 KΩ ± 5 % resistor to V_{SS}.

[13] With 1.5 KΩ ± 5% resistor to 3.6 V external pull-up.

[14] Guaranteed by design, not tested in production.

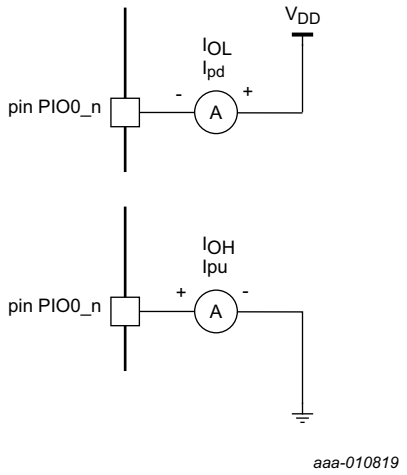
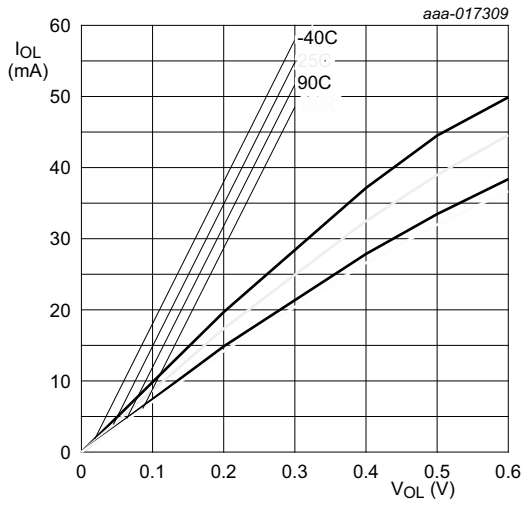
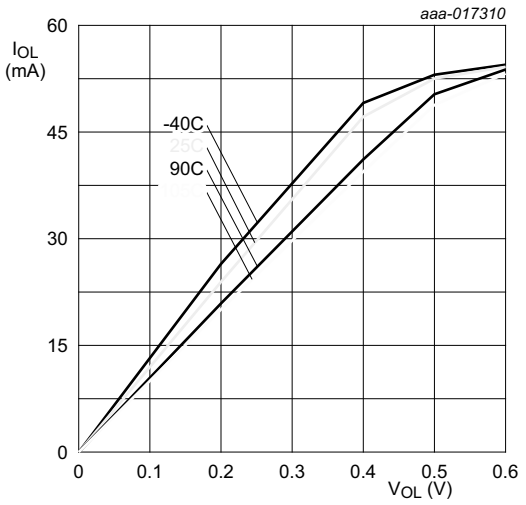


Fig 12. Pin input/output current measurement

10.4.1 Electrical pin characteristics



Conditions: V_{DD} = 1.8 V; on pins PIO0_23 to PIO0_26.



Conditions: V_{DD} = 3.3 V; on pins PIO0_23 to PIO0_26.

Fig 13. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

[2] Simulated using 10 cm of 50 Ω PCB trace with 5 pF receiver input. Rise and fall times measured between 80 % and 20 % of the full output signal level.

[3] The slew rate is configured in the IOCON block the SLEW bit. See the *LPC51U68 UM11071* user manual.

[4] C_L = 20 pF. Rise and fall times measured between 90 % and 10 % of the full input signal level.

11.3 Wake-up process

Table 23. Dynamic characteristic: Typical wake-up times from low power modes
V_{DD} = 3.3 V;T_{amb} = 25 °C; using FRO as the system clock.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from Sleep mode	[2][3]	-	2.0	-	µs
		from Deep-sleep mode	[2][3][5]	-	19	-	µs
		from deep power-down mode; RTC disabled; using $\overline{\text{RESET}}$ pin.	[4][5]	-	1.2	-	ms

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler.

[3] FRO enabled, all peripherals off. PLL disabled.

[4] RTC disabled. Wake up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when the $\overline{\text{RESET}}$ pin is triggered to wake the device up and when a GPIO output pin is set in the reset handler.

[5] FRO disabled.

11.4 System PLL

Table 24. PLL lock times and current
T_{amb} = −40 °C to +105 °C. V_{DD} = 1.62 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PLL configuration: input frequency 12 MHz; output frequency 75 MHz							
$t_{lock(PLL)}$	PLL lock time	PLL set-up procedure followed	[2]	-	-	400	µs
$I_{DD(PLL)}$	PLL current	when locked	[1][3]	-	-	550	µA
PLL configuration: input frequency 12 MHz; output frequency 100 MHz							
$t_{lock(PLL)}$	PLL lock time	PLL set-up procedure followed	[2]	-	-	400	µs
$I_{DD(PLL)}$	PLL current	when locked	[1][3]	-	-	750	µA
PLL configuration: input frequency 32.768 kHz; output frequency 75 MHz							
$t_{lock(PLL)}$	PLL lock time	-	[1]	-	-	6250	µs
$I_{DD(PLL)}$	PLL current	when locked	[1][3]	-	-	450	µA
PLL configuration: input frequency 32.768 kHz; output frequency 100 MHz							
$t_{lock(PLL)}$	PLL lock time	-	[1]	-	-	6250	µs
$I_{DD(PLL)}$	PLL current	when locked	[1][3]	-	-	560	µA

[1] Data based on characterization results, not tested in production.

[2] PLL set-up requires high-speed start-up and transition to normal mode. Lock times are only valid when high-speed start-up settings are applied followed by normal mode settings. The procedure for setting up the PLL is described in the LPC51U68 user manual.

[3] PLL current measured using lowest CCO frequency to obtain the desired output frequency.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

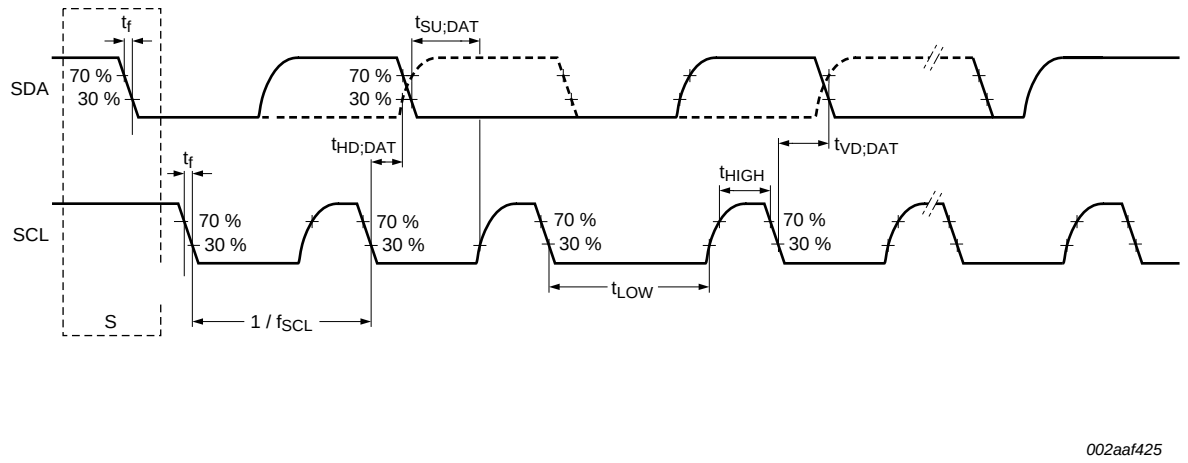


Fig 18. I²C-bus pins clock timing

11.9 I²S-bus interface

Table 30. Dynamic characteristics: I²S-bus interface pins [1][4]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.62 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1.0 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Typ[3]	Max	Unit
Common to master and slave							
t_{WH}	pulse width HIGH	on pins I2Sx_TX_SCK and I2Sx_RX_SCK[5]					
		CCLK = 1 MHz to 12 MHz		(T_{cyc}/2) -1	-	(T_{cyc}/2) +1	ns
		CCLK = 48 MHz to 60 MHz		(T_{cyc}/2) -1	-	(T_{cyc}/2) +1	ns
		CCLK = 96 MHz		(T_{cyc}/2) -1	-	(T_{cyc}/2) +1	ns
t_{WL}	pulse width LOW	on pins I2Sx_TX_SCK and I2Sx_RX_SCK[5]					
		CCLK = 1 MHz to 12 MHz		(T_{cyc}/2) -1	-	(T_{cyc}/2) +1	ns
		CCLK = 48 MHz to 60 MHz		(T_{cyc}/2) -1	-	(T_{cyc}/2) +1	ns
		CCLK = 96 MHz		(T_{cyc}/2) -1	-	(T_{cyc}/2) +1	ns

[2] Clock Divider register (DIV) = 0x0.

[3] Typical ratings are not guaranteed.

[4] The Flexcomm Interface function clock frequency should not be above 48 MHz. See the data rates section in the I²S chapter (UM10912) to calculate clock and sample rates.

[5] Based on simulation. Not tested in production.

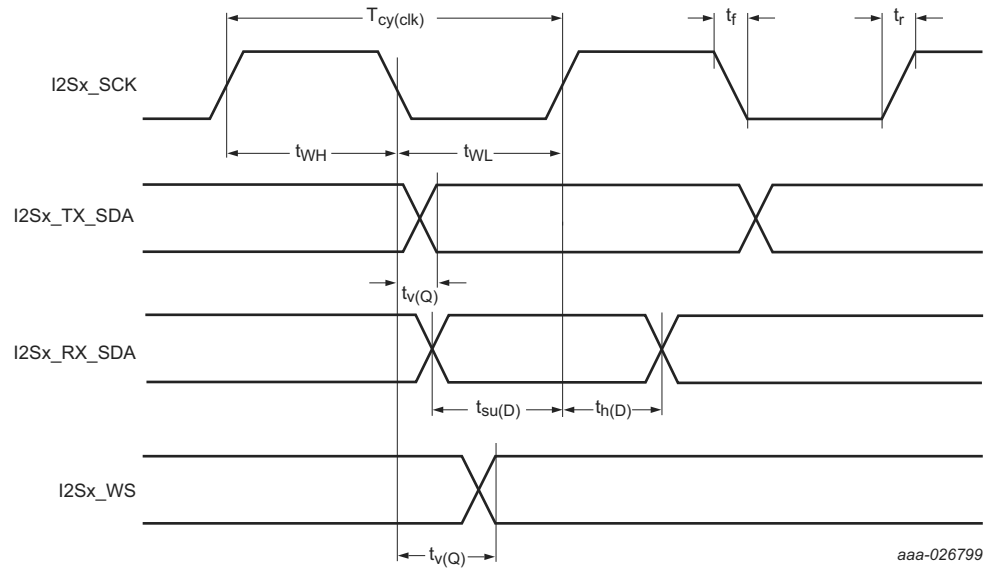


Fig 19. I²S-bus timing (master)

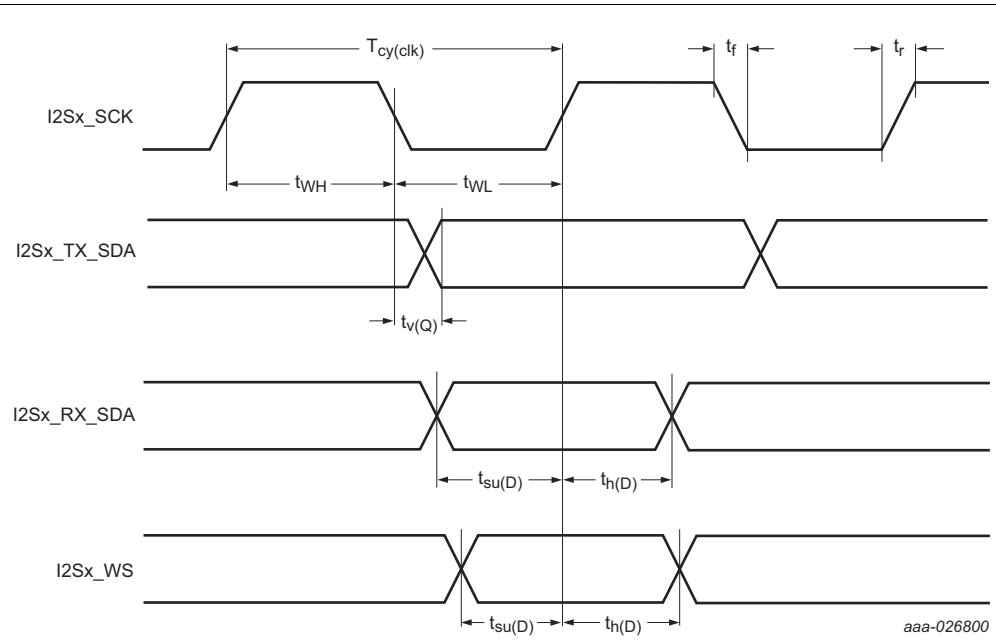


Fig 20. I²S-bus timing (slave)

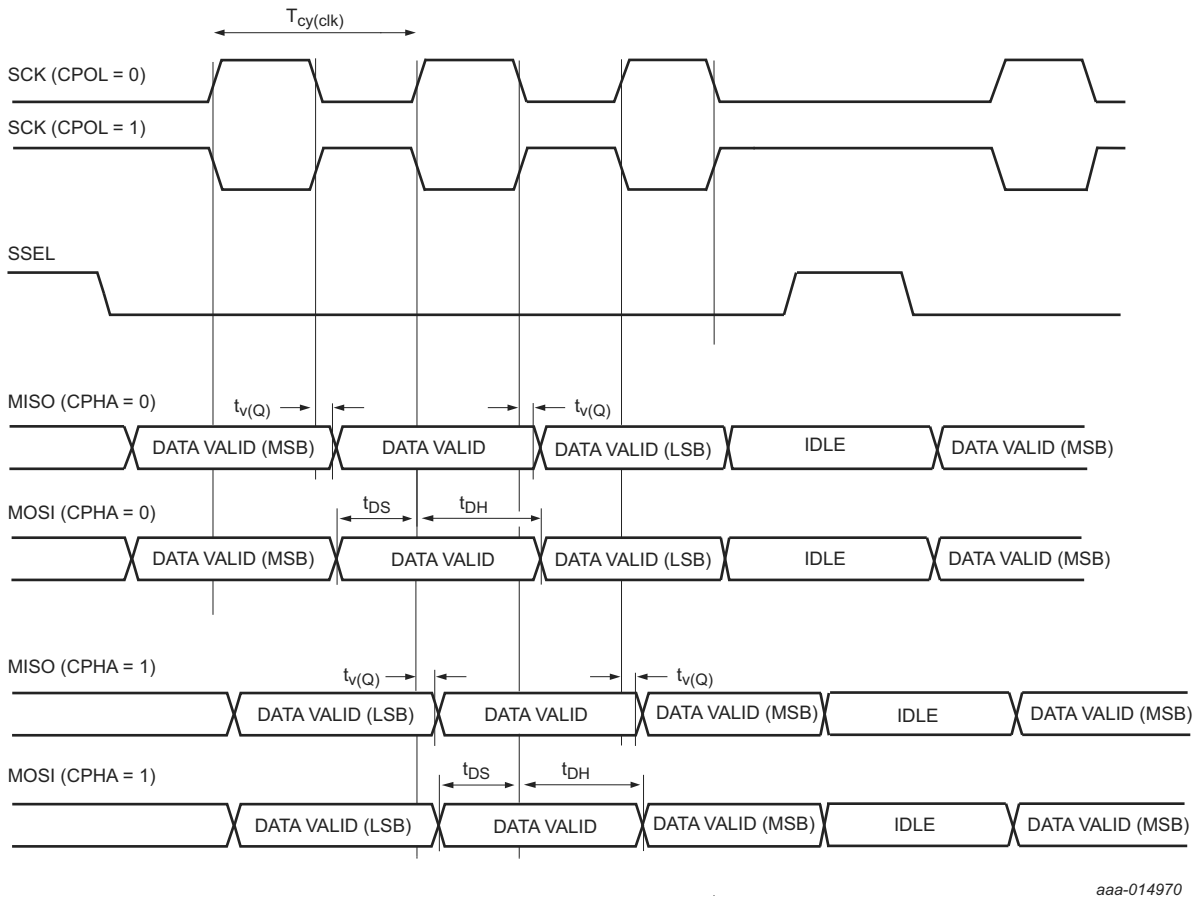


Fig 22. SPI slave timing

11.11 USART interface

The actual USART bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master synchronous mode is 20 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 16 Mbit/s

Table 32. USART dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.62 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW set to standard mode for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
USART master (in synchronous mode) 1.62 V ≤ V_{DD} ≤ 2.0 V						
$t_{su(D)}$	data input set-up time	CCLK = 1 MHz to 12 MHz	45	-	-	ns
		CCLK = 48 MHz to 60 MHz	39	-	-	ns
		CCLK = 96 MHz	38	-	-	ns
$t_{h(D)}$	data input hold time	CCLK = 1 MHz to 12 MHz	0	-	-	ns
		CCLK = 48 MHz to 60 MHz	0	-	-	ns
		CCLK = 96 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz	2	-	9	ns
		CCLK = 48 MHz to 60 MHz	1	-	5	ns
		CCLK = 96 MHz	1	-	4	ns
USART slave (in synchronous mode) 1.62 V ≤ V_{DD} ≤ 2.0 V						
$t_{su(D)}$	data input set-up time	CCLK = 1 MHz to 12 MHz	1	-	-	ns
		CCLK = 48 MHz to 60 MHz	1	-	-	ns
		CCLK = 96 MHz	1	-	-	ns
$t_{h(D)}$	data input hold time	CCLK = 1 MHz to 12 MHz	2	-	-	ns
		CCLK = 48 MHz to 60 MHz	3	-	-	ns
		CCLK = 96 MHz	3	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz	30	-	55	ns
		CCLK = 48 MHz to 60 MHz	23	-	46	ns
		CCLK = 96 MHz	22	-	46	ns
USART master (in synchronous mode) 2.7 V ≤ V_{DD} ≤ 3.6 V						
$t_{su(D)}$	data input set-up time	CCLK = 1 MHz to 12 MHz	35	-	-	ns
		CCLK = 48 MHz to 60 MHz	27	-	-	ns
		CCLK = 96 MHz	25	-	-	ns
$t_{h(D)}$	data input hold time	CCLK = 1 MHz to 12 MHz	0	-	-	ns
		CCLK = 48 MHz to 60 MHz	0	-	-	ns
		CCLK = 96 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz	2	-	9	ns
		CCLK = 48 MHz to 60 MHz	2	-	5	ns
		CCLK = 96 MHz	1	-	4	ns

11.13 USB interface characteristics

Table 34. Dynamic characteristics: USB pins (Full-Speed)

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to V_{DD}, unless otherwise specified; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %		4.0	-	20	ns
t_f	fall time	10 % to 90 %		4.0	-	20	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f		90	-	111.11	%
V_{CRS}	output signal crossover voltage			1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 26		160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 26		−2	-	+5	ns
t_{JR1}	receiver jitter to next transition			−18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %		−9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 26	[1]	40	-		ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 26	[1]	82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

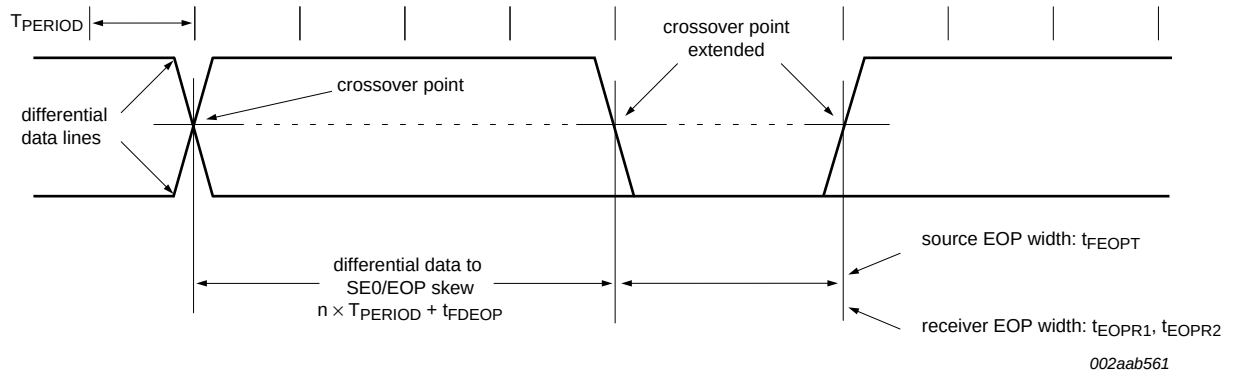


Fig 24. Differential data-to-EOP transition skew and EOP width

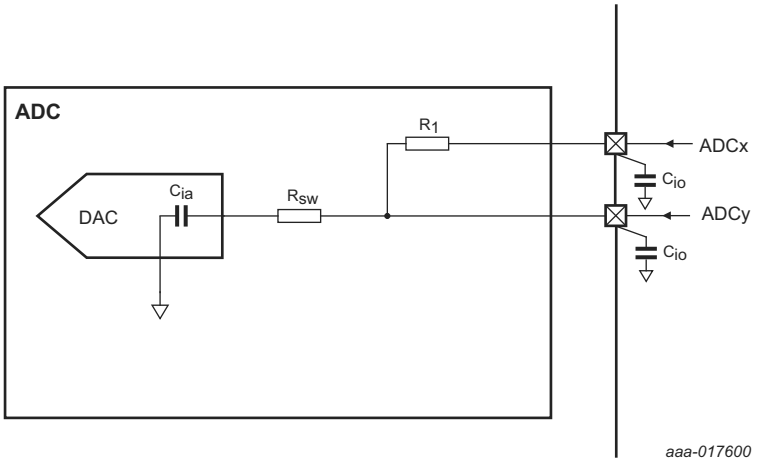


Fig 26. ADC input impedance

12.3 Temperature sensor

Table 38. Temperature sensor static and dynamic characteristics
$V_{DD} = V_{DDA} = 1.62$ V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = −40 °C to +105 °C	[1]	-	-	3	°C
E_L	linearity error	T_{amb} = −40 °C to +105 °C		-	-	3	°C
$t_{s(pu)}$	power-up settling time	to 99% of temperature sensor output value	[2]	-	10	15	µs

[1] Absolute temperature accuracy.

[2] Based on simulation.

$C_{Parasitic}$ – Parasitic or stray capacitance of external circuit.

Although $C_{Parasitic}$ can be ignored in general, the actual board layout and placement of external components influences the optimal values of external load capacitors. Therefore, it is recommended to fine tune the values of external load capacitors on actual hardware board to get the accurate clock frequency. For fine tuning, output the RTC Clock to one of the GPIOs and optimize the values of external load capacitors for minimum frequency deviation.

13.5.1 RTC Printed Circuit Board (PCB) design guidelines

- Connect the crystal and external load capacitors on the PCB as close as possible to the oscillator input and output pins of the chip.
- The length of traces in the oscillation circuit should be as short as possible and must not cross other signal lines.
- Ensure that the load capacitors CX1, CX2, and CX3, in case of third overtone crystal usage, have a common ground plane.
- Loops must be made as small as possible to minimize the noise coupled in through the PCB and to keep the parasitics as small as possible.
- Lay out the ground (GND) pattern under crystal unit.
- Do not lay out other signal lines under crystal unit for multi-layered PCB.

13.6 Suggested USB interface solutions

The USB device can be connected to the USB as self-powered device (see Figure 32) or bus-powered device (see Figure 33).

On the LPC51U68, the USB_VBUS pin is 5 V tolerant only when V_{DD} is applied and at operating voltage level. Therefore, if the USB_VBUS function is connected to the USB connector and the device is self-powered, the USB_VBUS pin must be protected for situations when V_{DD} = 0 V.

If V_{DD} is always at operating level while VBUS = 5 V, the USB_VBUS pin can be connected directly to the VBUS pin on the USB connector.

For systems where V_{DD} can be 0 V and VBUS is directly applied to the VBUS pin, precautions must be taken to reduce the voltage to below 3.6 V, which is the maximum allowable voltage on the USB_VBUS pin in this case.

One method is to use a voltage divider to connect the USB_VBUS pin to the VBUS on the USB connector. The voltage divider ratio should be such that the USB_VBUS pin is greater than 0.7 V_{DD} to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

For the following operating conditions

$VBUS_{max}$ = 5.25 V

V_{DD} = 3.6 V,

the voltage divider should provide a reduction of 3.6 V/5.25 V or ~0.686 V.