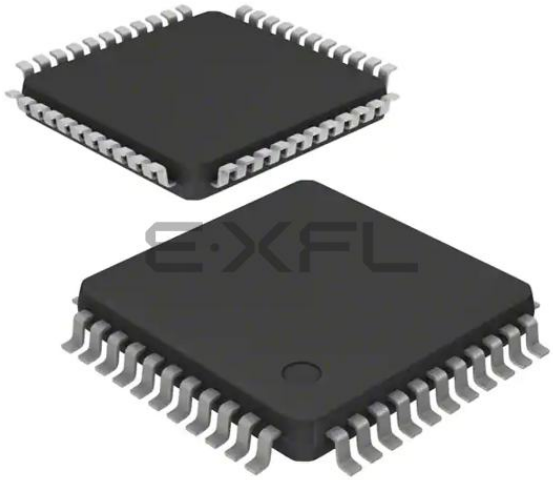

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	31
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	748 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e7216asg

Table of Contents

Pin Description

Figure 3 shows the pin assignments for the standard mode of the 40-pin dual in-line package (DIP). Figure 4 on page 6 shows the pin assignments for the electronically programmable read-only memory (EPROM) mode of the 40-pin DIP.

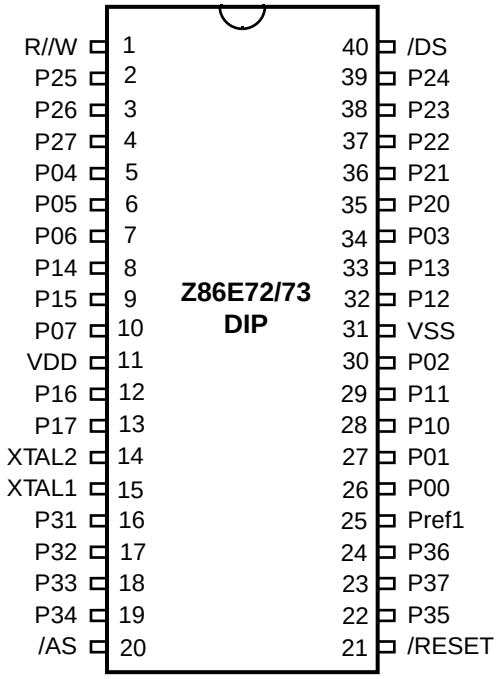


Figure 3. 40-Pin DIP Pin Assignments (Standard Mode)

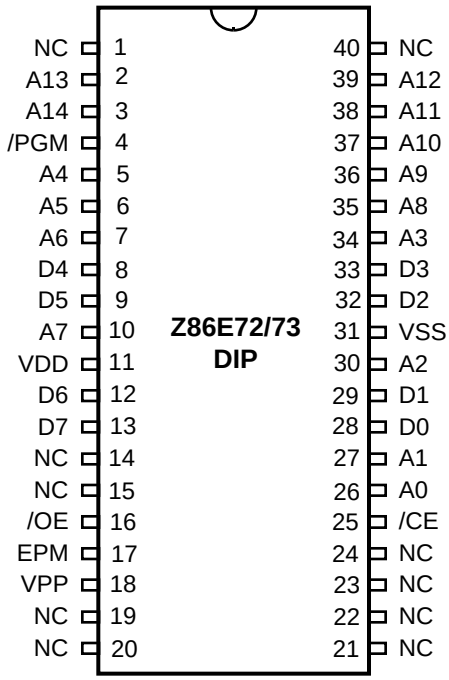


Figure 4. 40-Pin DIP Pin Assignments (EPROM Mode)

Figure 5 on page 7 shows the pin assignments for the standard mode of the 44-pin plastic leaded chip carrier (PLCC). Figure 6 on page 7 displays the pin assignments for the EPROM mode of the 44-pin PLCC.

Table 4. Z86E72/73 40-Pin DIP Identification—EPROM Mode (Continued)

40-Pin #	Symbol	Function	Direction
34	A3	Address 3	Input
35–39	A8–A12	Address 8, 9, 10, 11, 12	Input
40	N/C	Not Connected	

Table 5. Z86E72/73 44-Pin LQFP/PLCC Pin Identification—EPROM Mode

44-Pin LQFP	44-Pin PLCC	Symbol	Function	Direction
1–2	18–19	A5–A6	Address 5, 6	Input
3–4	20–21	D4–D5	Data 4, 5	Input/Output
5	22	A7	Address 7	Input
6–7	23–24	V_{DD}	Power Supply	
8–9	25–26	D6–D7	Data 6, 7	Input/Output
10	27	XTAL2	Crystal Oscillator Clock	
11	28	XTAL1	Crystal Oscillator Clock	
12	29	/OE	Output Enable	Input
13	30	EPM	EPROM Prog. Mode	Input
14	31	V_{PP}	Prog. Voltage	Input
15–16	32–33	N/C	Not Connected	
17	34	V_{SS}	Ground	
18–21	35–38	N/C	Not Connected	
22	39	/CE	Chip Select	Input
23–24	40–41	A0–A1	Address 0, 1	Input
25–26	42–43	D0–D1	Data 0, 1	Input/Output
27	44	A2	Address 2	Input
28–29	1–2	V_{SS}	Ground	
30–31	3–4	D2–D3	Data 2, 3	Input/Output
32	5	A3	Address 3	Input
33–37	6–10	A8–A12	Address 8, 9, 10, 11, 12	Input
38–40	11–13	N/C	Not Connected	

Table 8. DC Characteristics (Continued)

Sym.	Parameter	V_{CC}	T_A = 0 °C to +70 °C Min	Max	Typical @ 25°C	Units	Conditions
V_{RAM}	Static RAM Data Retention Voltage	Vram			0.5	V	Worst case 0.8 V guaranteed by design only Note 6

Notes:	ICC1	Typ	Max	Unit	Frequency
	Crystal/Resonator	3.0 mA	5	mA	8.0 MHz
	External Clock Drive	0.3 mA	5	mA	8.0 MHz

1. All outputs unloaded, inputs at rail
2. CL1 = CL2 = 100 pF
3. Same as note [4] except inputs at V_{CC}
4. The V_{LV} increases as the temperature decreases.
5. Oscillator stopped
6. Oscillator does not stop when V_{CC} falls below V_{LV} threshold.
7. 32 kHz clock driver input
8. For analog comparator, inputs when analog comparators are enabled
9. WDT, Comparators, Low Voltage Detection, and ADC (if applicable) are disabled. The IC might draw more current if any of the above peripherals is enabled.

* All outputs excluding P00, P01, P36, and P37

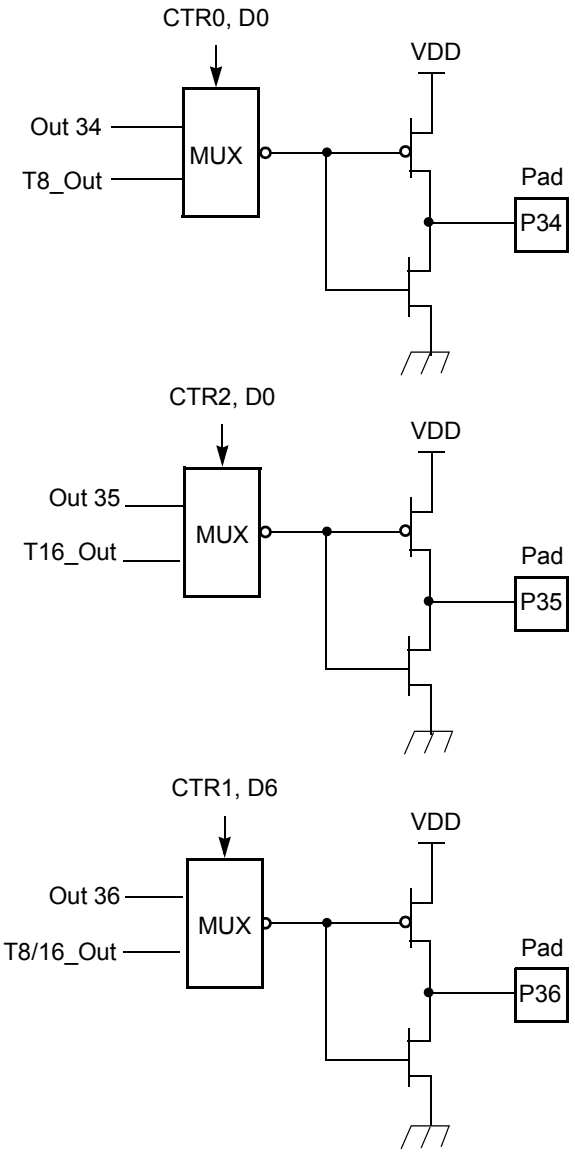


Figure 19. Port 3 Configuration

Functional Description

The Z86E72/73 microcontrollers incorporate special functions to enhance the Z8's functionality in consumer and battery-operated applications.

Reset

The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source
- Low Voltage Detection
- External Reset

Program Memory

The Z86E72/73 microcontrollers address up to 16K/32 KB of internal program memory, with the remainder being external memory (Figure 20). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain five 16-bit vectors that correspond to the five available interrupts. Addresses of 16K/32K consist of on-chip OTP. At addresses 16K or 32K and greater, the Z86E72/73 microcontrollers execute external program memory fetches (see “External Memory” on page 38).

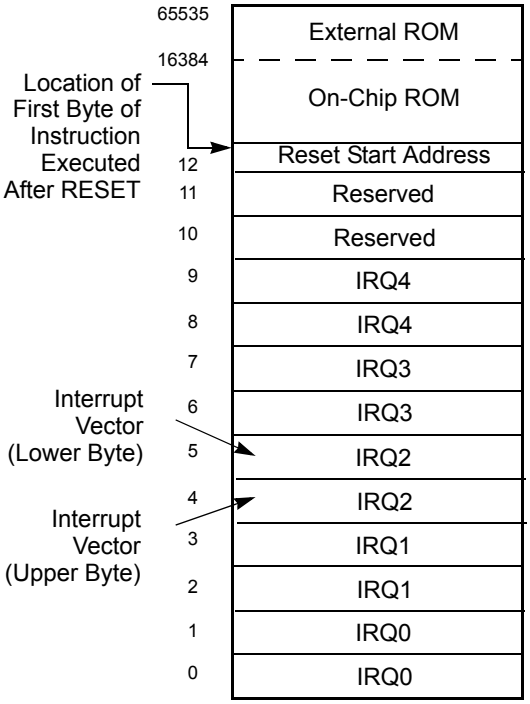


Figure 20. Program Memory Map

RAM

The Z86E72 has a 768-byte RAM; 256 bytes make up the register file. The remaining 512 bytes make up the Extended Data RAM. The Z86E73 has just the 256 bytes of the register file.

Extended Data RAM

The Extended Data RAM of the Z86E72 occupies the address range FE00H–FFFFH (512 bytes). This range of addresses FD00H–FFFFH cannot be used to directly read from or write to external memory. Accessing the Extended Data RAM is accomplished by using LDE or LDEI instructions. Port 1 and Port 0 are free to be set as I/O or ADDR/DATA modes; expect high-impedance when accessing Extended Data RAM. In addition, if the external memory uses the same address range of the Extended Data RAM, it can be used as the External Stack only.

Exercise caution when using extended data RAM (not Z8 RAM) on the Z86E72 OTP microcontroller. Extended RAM spaces FF0C–FF0F, FF10, FE0C–FE0F, and FE10 are reserved. Do not use these extended RAM locations.

Note: The Extended Data RAM cannot be used as STACK or instruction/code memory. Accessing the Extended Data RAM has the following condition: P01M register bits D4–D3 cannot be set to 11.

External Memory

The Z86E72/73 microcontrollers address up to 32 KB (minus FD00H–FFFFH) of external memory beginning at address 8000H (32K+1). External data memory is included with, or separated from, the external program memory space. /DM, an optional I/O function that is programmed to appear on P34, is used to distinguish between data and program memory space. The state of the /DM signal is controlled by the type of instruction being executed. An LDC op code references PROGRAM (/DM inactive) memory, and an LDE instruction references data (/DM active Low) memory. See Figure 21.

Table 13. Expanded Register Group D (Continued)

(D) 09h	HI16
(D) 08h	LO16
(D) 07h	TC16H
(D) 06h	TC16L
(D) 05h	TC8H
(D) 04h	TC8L
(D) 03h	Reserved
(D) 02h	CTR2
(D) 01h	CTR1
(D) 00h	CTR0

HI8(D)0Bh Register

This register (Table 14) holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 1.

Table 14. HI8(D)0Bh Register

Field	Bit Position	Value	Description
T8_Capture_HI	76543210	R/W	Captured Data No Effect

L08(D)0Ah Register

This register (Table 15) holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 0.

Table 15. LO8(D)0Ah Register

Field	Bit Position	Value	Description
T8_Capture_L0	76543210	R/W	Captured Data No Effect

Counter_INT_Mask

Set this bit to allow interrupt when T8 has a time out.

P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

CTR1(D)01h Register

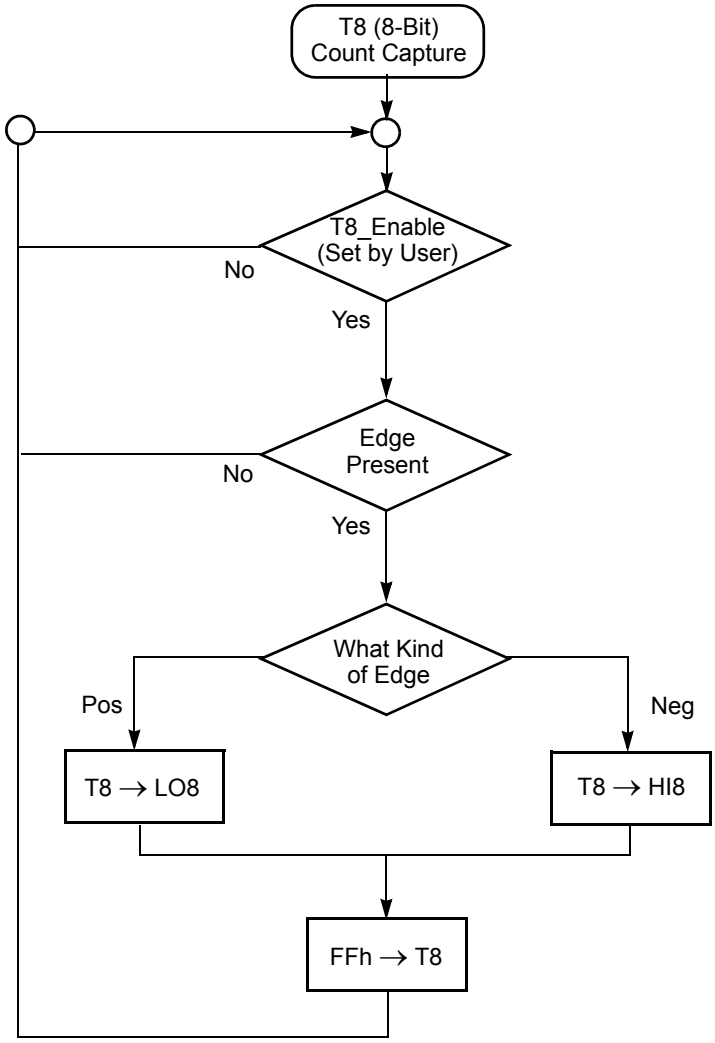
This register (Table 23) controls the functions in common with the T8 and T16.

Table 23. CTR1(D)01h Register

Field	Bit Position		Value	Description
Mode	7-------	R/W	0*	Transmit Mode
			1	Demodulation Mode
P36_Out/Demodulator_Input	-6------	R/W		Transmit Mode
			0*	Port Output
			1	T8/16 Output
				Demodulation Mode
			0	P31
			1	P20
T8/T16_Logic/Edge _Detect	--54----	R/W		Transmit Mode
			0 0	AND
			0 1	OR
			1 0	NOR
			1 1	NAND
				Demodulation Mode
			0 0	Falling Edge
			0 1	Rising Edge
			1 0	Both Edges
			1 1	Reserved
Transmit_Submode/Glitch_Filter	----32--	R/W		Transmit Mode
			0 0	Normal Operation
			0 1	Ping-Pong Mode
			1 0	T16_OUT = 0
			1 1	T16_OUT = 1
				Demodulation Mode
			0 0	No Filter
			0 1	4 SCLK Cycle
			1 0	8 SCLK Cycle
			1 1	16 SCLK Cycle

T8 Demodulation Mode

You need to program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1 D5, D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1 D5, D4) is detected during counting, the current value of T8 is one's complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if negative edge, HI8. One of the edge-detect status bits (CTR1 D1, D0) is set, and an interrupt can be generated if enabled (CTR0 D2). Meanwhile, T8 is loaded with FFh and starts counting again. When T8 reaches 0, the time-out status bit (CTR0 D5) is set, an interrupt can be generated if enabled (CTR0 D1), and T8 continues counting from FFh (see Figure 30 and Figure 31).



HALT

HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, and IRQ4 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP

This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 μA (typical) or less. STOP Mode is terminated only by a reset, such as WDT time-out, POR, SMR, or external reset. This causes the processor to restart the application program at address 000CH. To enter STOP (or HALT) mode, you need to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, you must execute a NOP (op code = FFH) immediately before the appropriate sleep instruction. For example:

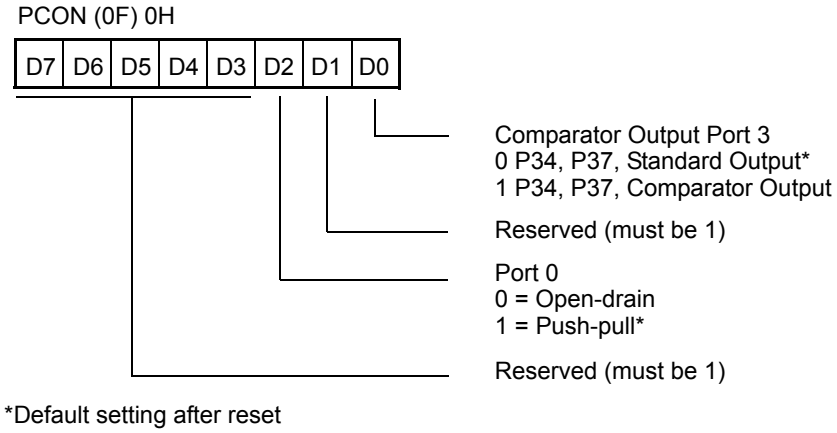
```
FF          NOP         ; clear the pipeline
6F          STOP        ; enter STOP Mode
```

or

```
FF          NOP         ; clear the pipeline
7F          HALT        ; enter HALT Mode
```

Port Configuration Register (PCON)

The PCON register (Figure 39) configures the comparator output on Port 3. It is located in the expanded register file at Bank F, location 00.



*Default setting after reset

Figure 39. Port Configuration Register (PCON)—Write Only

Stop-Mode Recovery Delay Select (D5)

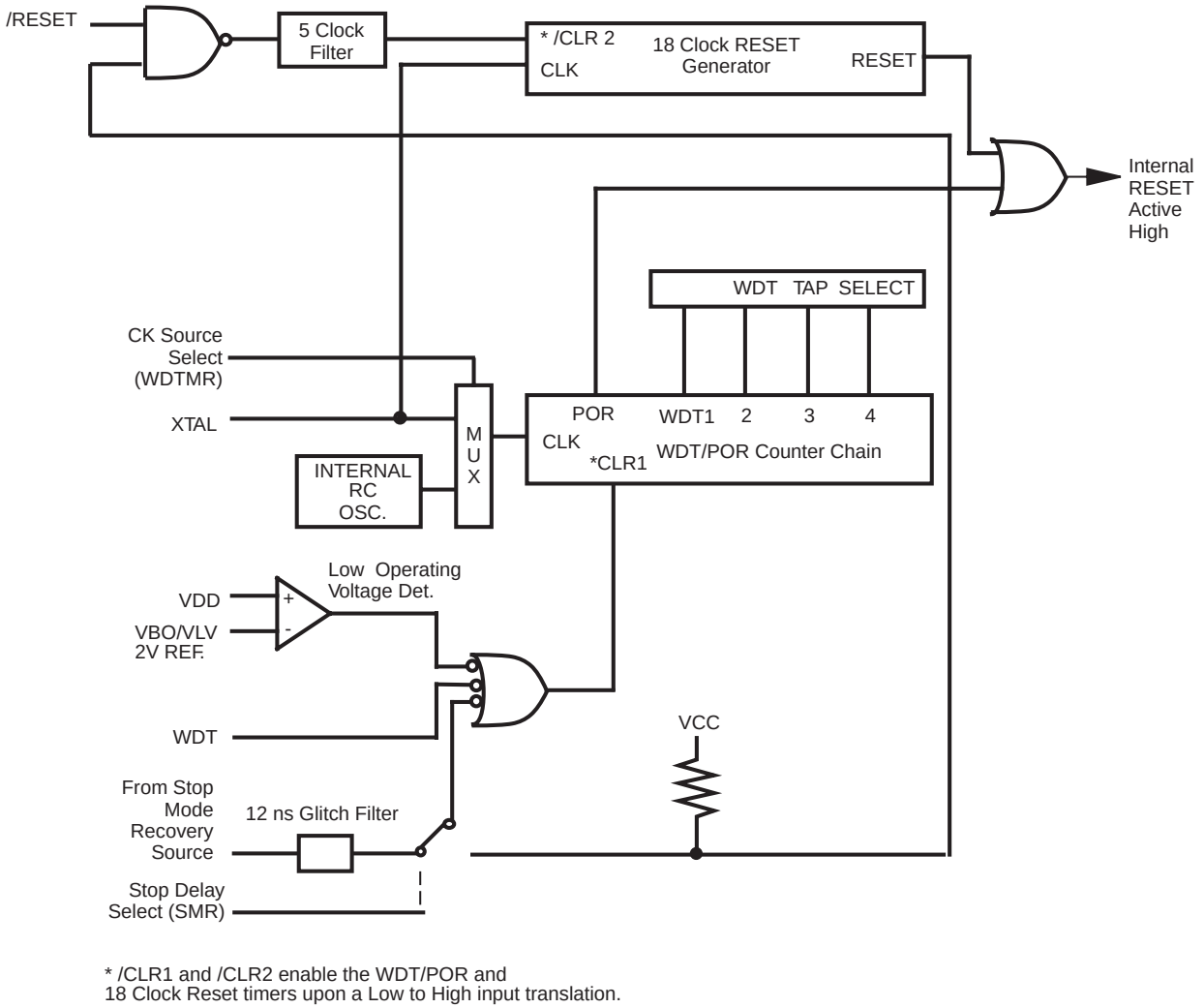
This bit, if low, disables the 5 ms /RESET delay after Stop-Mode Recovery. The default configuration of this bit is one. If the “fast” wake up is selected, the Stop-Mode Recovery source needs to be kept active for at least 5TpC.

Stop-Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the Z86E7X from STOP Mode. A 0 indicates Low level recovery. The default is 0 on POR.

Cold or Warm Start (D7)

This bit is set by the device upon entering STOP Mode. It is a read-only Flag bit. A 1 in D7 (warm) indicates that the device awakes from a SMR source or a WDT while in STOP Mode. A 0 in this bit (cold) indicates that the device is reset by a POR or WDT while not in STOP Mode.



* /CLR1 and /CLR2 enable the WDT/POR and
18 Clock Reset timers upon a Low to High input translation.

Figure 44. Resets and WDT

Low-Voltage Protection

An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below V_{LV} (Low Voltage). The minimum operating voltage varies with the temperature and operating frequency, while V_{LV} varies with temperature only.

Note: The LVD flag will be valid after enabling the detection for 20 μS (design estimation, not tested in production). LVD does not work at STOP mode. It must be disabled during STOP mode in order to reduce current.

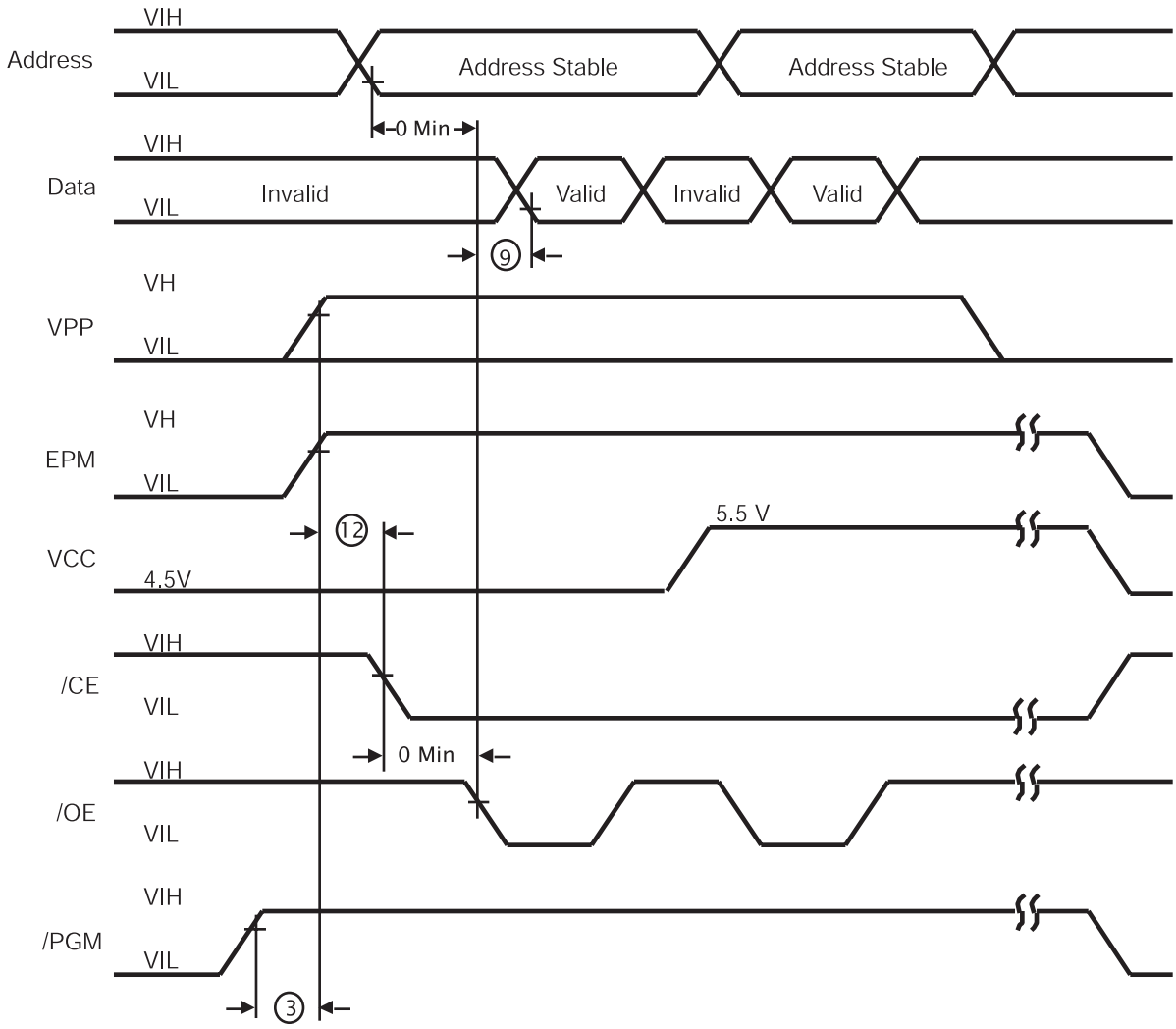


Figure 45. EPROM Read

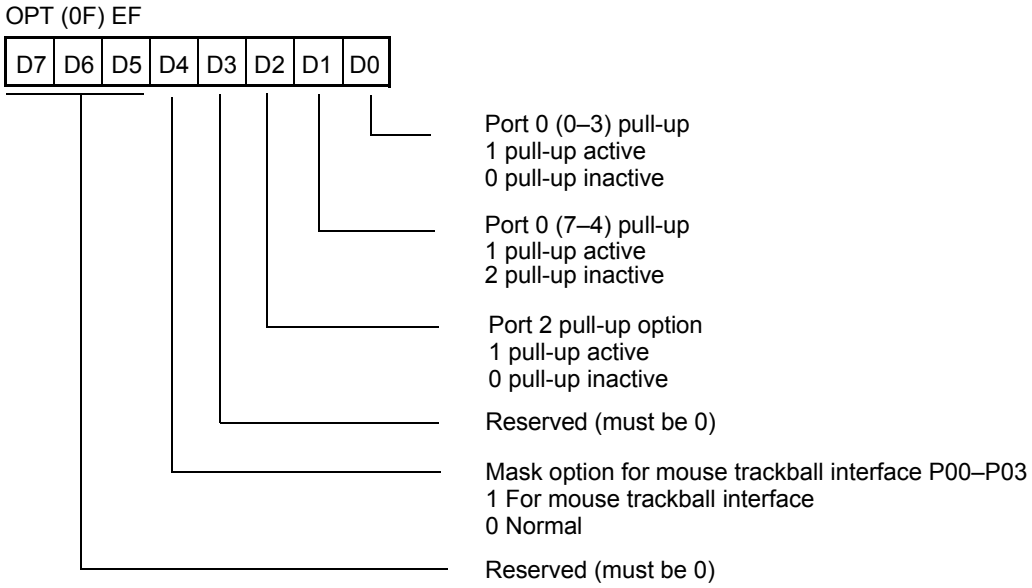
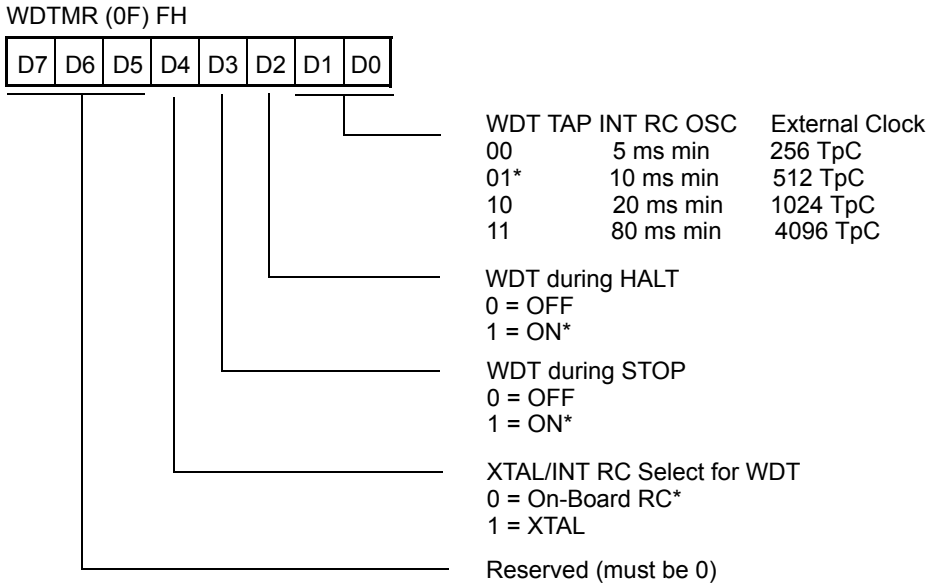


Figure 54. Option Bit Register



* Default setting after reset

Figure 55. Watch-Dog Timer Mode Register—(F) 0FH: Write Only

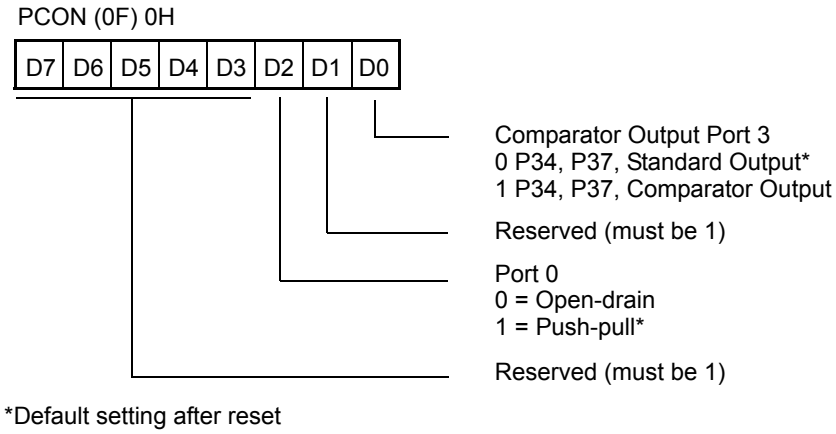


Figure 56. Port Configuration Register (PCON)—(0F) 0H: Write Only

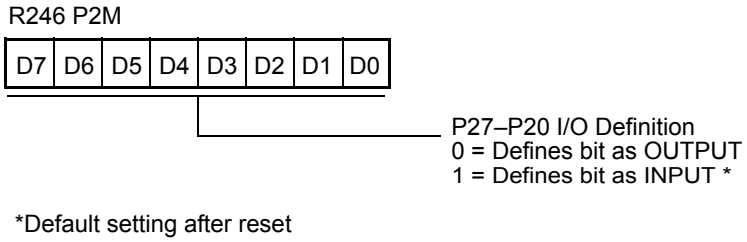


Figure 57. Port 2 Mode Register—F6H: Write Only

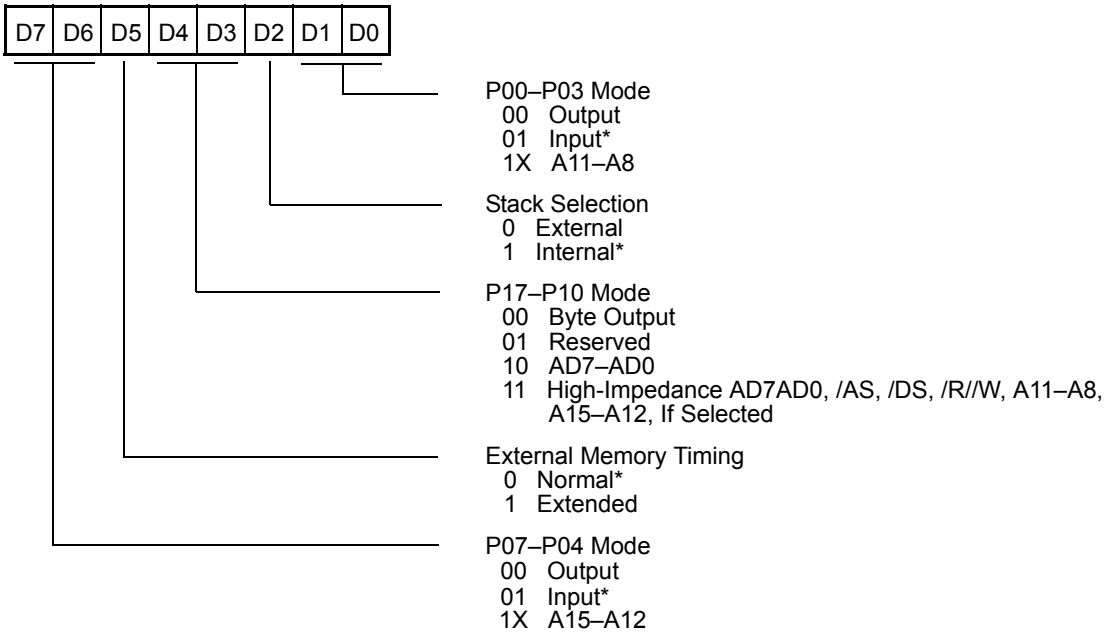


Figure 59. Port 0 and 1 Mode Register—F8H: Write Only

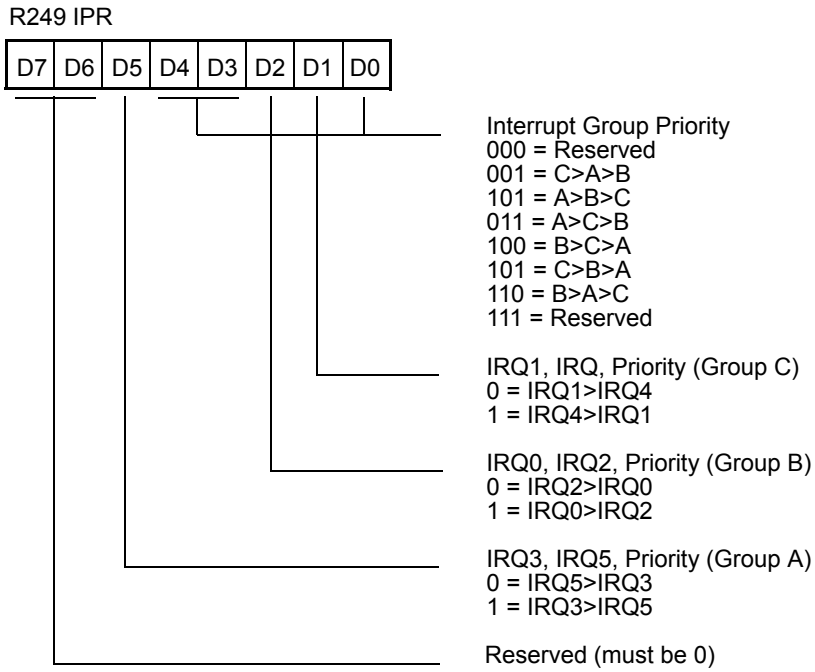


Figure 66. Stack Pointer Low—(0) FFH: Read/Write