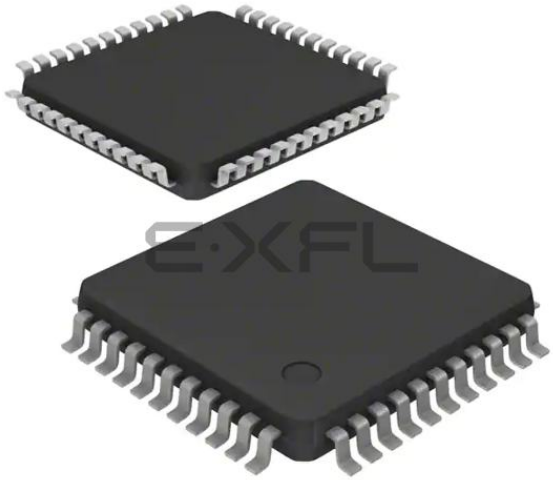

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	31
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	748 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e7216fsc

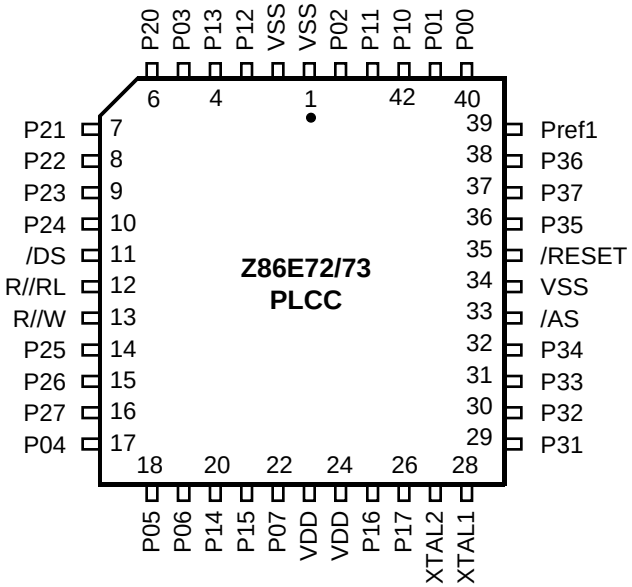


Figure 5. 44-Pin PLCC Pin Assignments (Standard Mode)

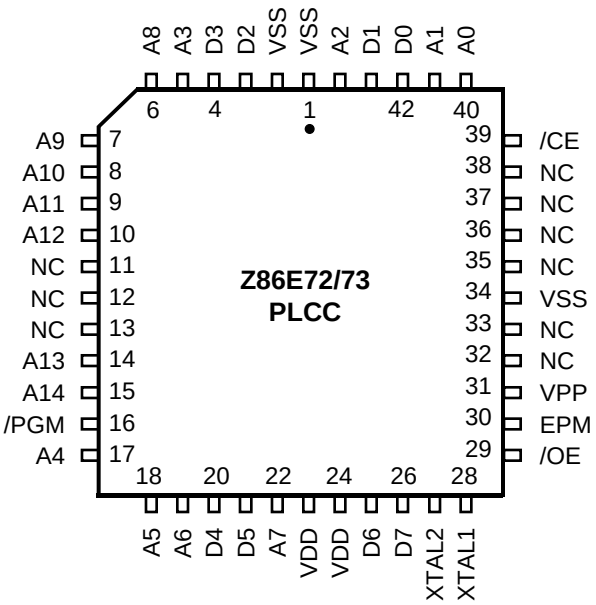


Figure 6. 44-Pin PLCC Pin Assignments (EPROM Mode)

Table 4. Z86E72/73 40-Pin DIP Identification—EPROM Mode (Continued)

40-Pin #	Symbol	Function	Direction
34	A3	Address 3	Input
35–39	A8–A12	Address 8, 9, 10, 11, 12	Input
40	N/C	Not Connected	

Table 5. Z86E72/73 44-Pin LQFP/PLCC Pin Identification—EPROM Mode

44-Pin LQFP	44-Pin PLCC	Symbol	Function	Direction
1–2	18–19	A5–A6	Address 5, 6	Input
3–4	20–21	D4–D5	Data 4, 5	Input/Output
5	22	A7	Address 7	Input
6–7	23–24	V_{DD}	Power Supply	
8–9	25–26	D6–D7	Data 6, 7	Input/Output
10	27	XTAL2	Crystal Oscillator Clock	
11	28	XTAL1	Crystal Oscillator Clock	
12	29	/OE	Output Enable	Input
13	30	EPM	EPROM Prog. Mode	Input
14	31	V_{PP}	Prog. Voltage	Input
15–16	32–33	N/C	Not Connected	
17	34	V_{SS}	Ground	
18–21	35–38	N/C	Not Connected	
22	39	/CE	Chip Select	Input
23–24	40–41	A0–A1	Address 0, 1	Input
25–26	42–43	D0–D1	Data 0, 1	Input/Output
27	44	A2	Address 2	Input
28–29	1–2	V_{SS}	Ground	
30–31	3–4	D2–D3	Data 2, 3	Input/Output
32	5	A3	Address 3	Input
33–37	6–10	A8–A12	Address 8, 9, 10, 11, 12	Input
38–40	11–13	N/C	Not Connected	

Table 10. Additional Timing (Continued)

				T_A = 0°C to +70°C			
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
6	TpTi	Timer Input Period	3.0 V 5.5 V	8TpC 8TpC			1
7	TrTin,TfTi	Timer Input Rise and Fall Timers	3.0 V 5.5 V	100 70		ns ns	1 1
8A	TwIL	Interrupt Request Low Time	3.0 V 5.5 V	100 70		ns ns	1, 2 1, 2
8B	TwIL	Int. Request Low Time	4.5 V 5.5 V	3TpC 5TpC			1, 3 1, 3
9	TwIH	Interrupt Request Input High Time	4.5 V 5.5 V	5TpC 5TpC			1, 2 1, 2
10	Twsm	Stop-Mode Recovery Width Spec	3.0 V 5.5 V 3.0 V 5.5 V	12 12 5TpC 5TpC		ns ns	7 7 6 6
11	Tost	Oscillator Start-up Time	3.0 V 5.5 V		5TpC 5TpC		4
12	Twdt	Watch-Dog Timer Delay Time (5 ms)	3.0 V 5.5 V	12 5	75 20	ms ms	
		(10 ms)	3.0 V 5.5 V	25 10	150 40	ms ms	
		(20 ms)	3.0 V 5.5 V	50 20	300 80	ms ms	
		(80 ms)	3.0 V 5.5 V	225 80	1200 320	ms ms	

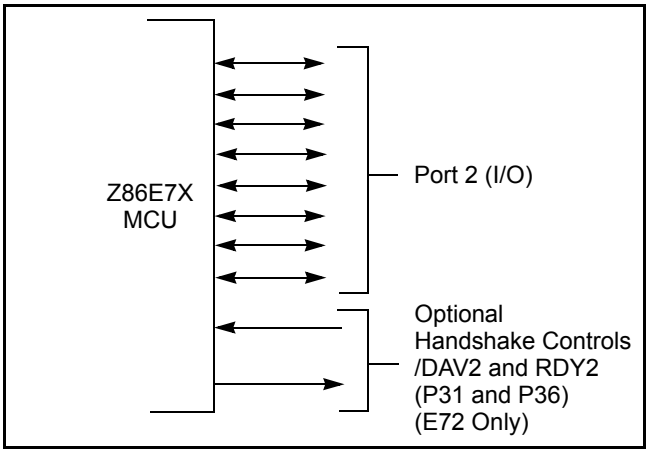
Notes:
1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. Interrupt request through Port 3 (P30).
4. SMR – D5 = 0
5. Reg. WDTMR
6. Reg. SMR – D5 = 0
7. Reg. SMR – D5 = 1

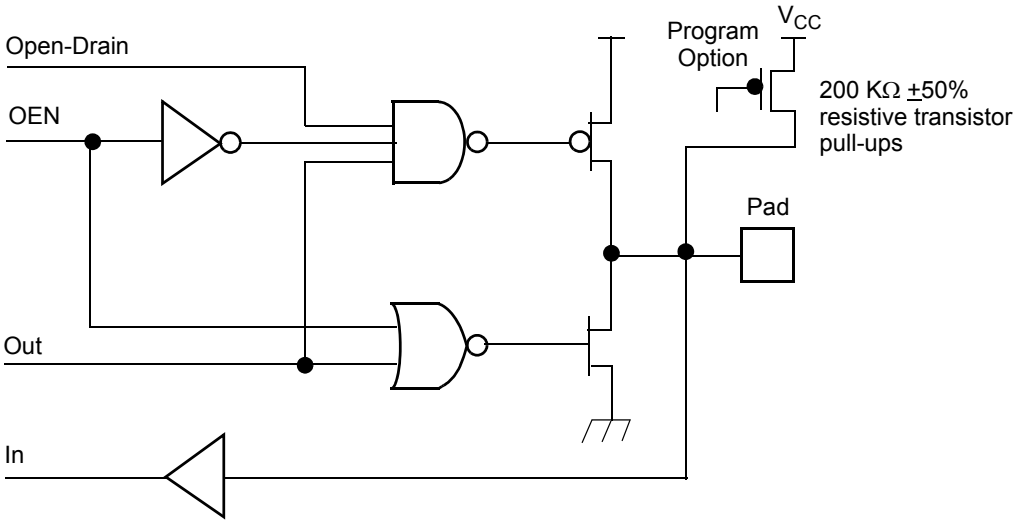
Figure 12 shows the input handshake timing, and Figure 13 shows the output handshake timing. Table 11 describes the handshake timing.

Figure 15. Port 1 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 16). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A software option is available to connect eight 200 KΩ (±50%) pull-up resistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. Port 2 can be placed under handshake control. In this configuration, Port 3 lines, P31 and P36 are used as the handshake controls lines /DAV2 and RDY2. The handshake signal assignment for Port 3, lines P31 and P36 is dictated by the direction (input or output) assigned to Bit 7, Port 2.





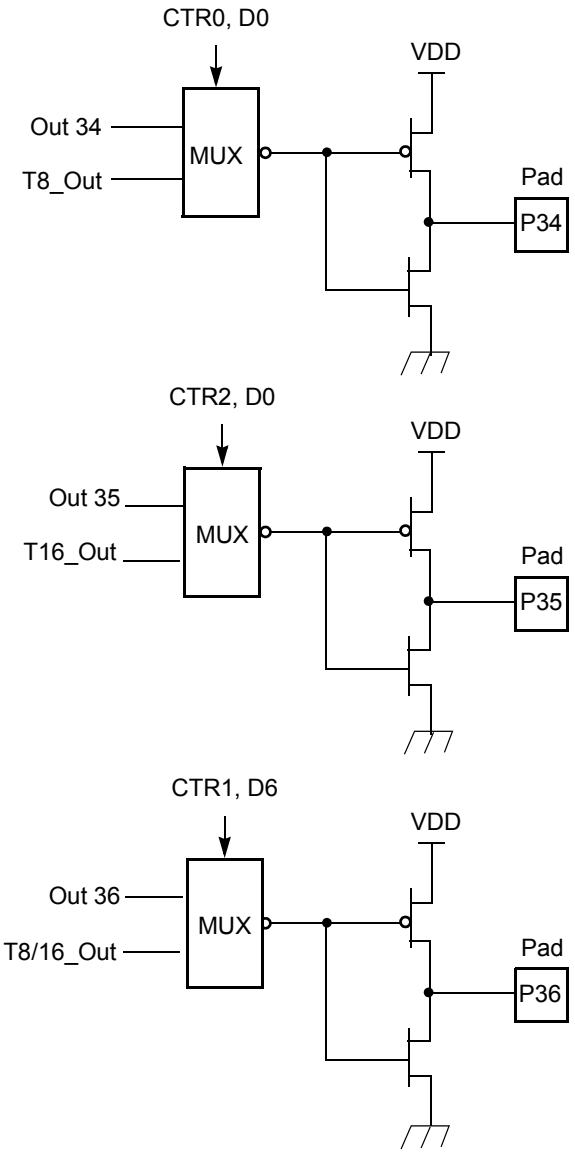


Figure 19. Port 3 Configuration

Table 13. Expanded Register Group D (Continued)

(D) 09h	HI16
(D) 08h	LO16
(D) 07h	TC16H
(D) 06h	TC16L
(D) 05h	TC8H
(D) 04h	TC8L
(D) 03h	Reserved
(D) 02h	CTR2
(D) 01h	CTR1
(D) 00h	CTR0

HI8(D)0Bh Register

This register (Table 14) holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 1.

Table 14. HI8(D)0Bh Register

Field	Bit Position	Value	Description
T8_Capture_HI	76543210	R/W	Captured Data No Effect

L08(D)0Ah Register

This register (Table 15) holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 0.

Table 15. LO8(D)0Ah Register

Field	Bit Position	Value	Description
T8_Capture_L0	76543210	R/W	Captured Data No Effect

T8 Demodulation Mode

You need to program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1 D5, D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1 D5, D4) is detected during counting, the current value of T8 is one's complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if negative edge, HI8. One of the edge-detect status bits (CTR1 D1, D0) is set, and an interrupt can be generated if enabled (CTR0 D2). Meanwhile, T8 is loaded with FFh and starts counting again. When T8 reaches 0, the time-out status bit (CTR0 D5) is set, an interrupt can be generated if enabled (CTR0 D1), and T8 continues counting from FFh (see Figure 30 and Figure 31).

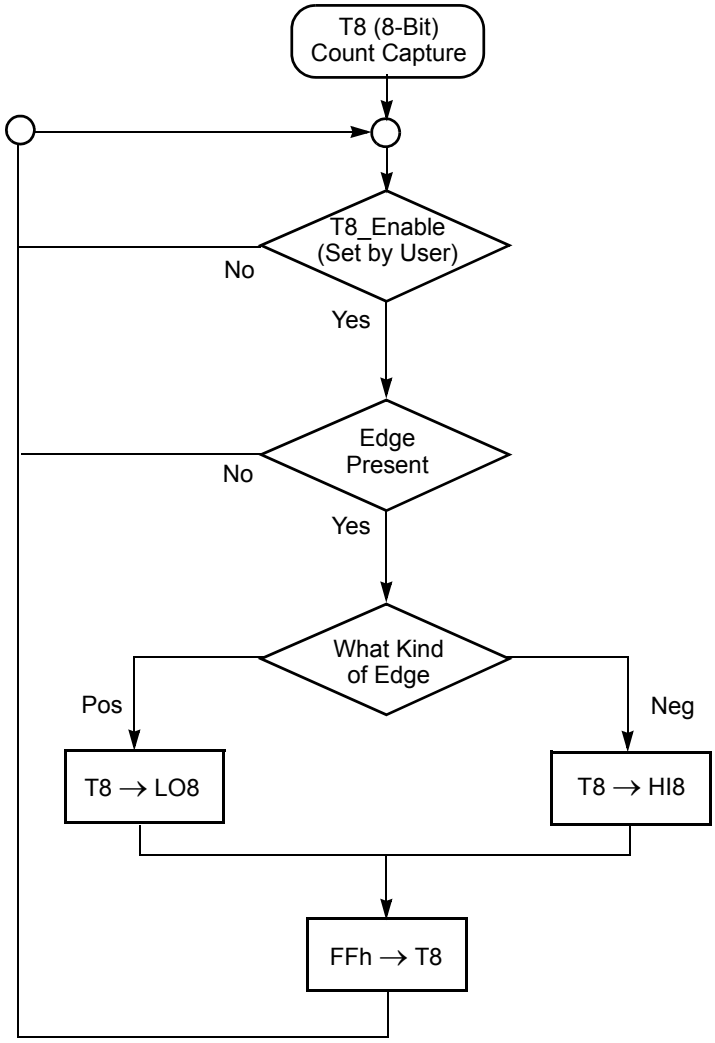


Figure 30. Demodulation Mode Count Capture Flowchart

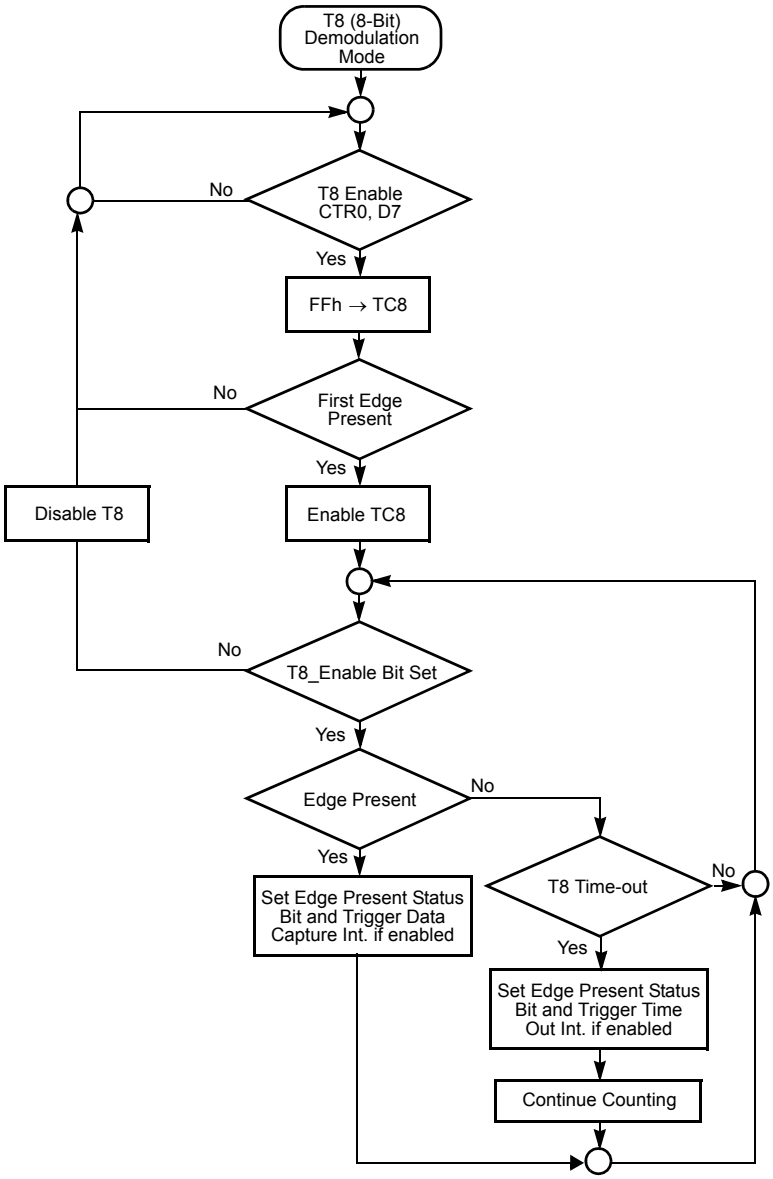


Figure 31. Demodulation Mode Flowchart

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground. The RC oscillator configuration is an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (see Figure 38).

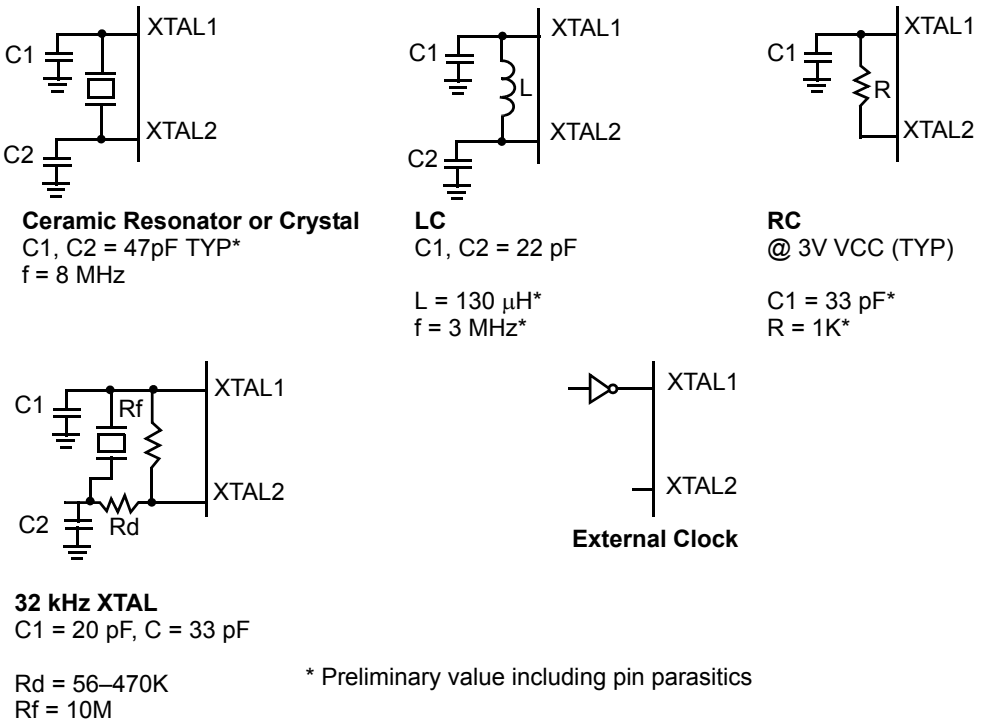


Figure 38. Oscillator Configuration

Power-On Reset (POR)

A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows VCC and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status.
- Stop-Mode Recovery (if D5 of SMR = 1).
- WDT Time-Out.

The POR time is a nominal 5 ms. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC, and LC oscillators).

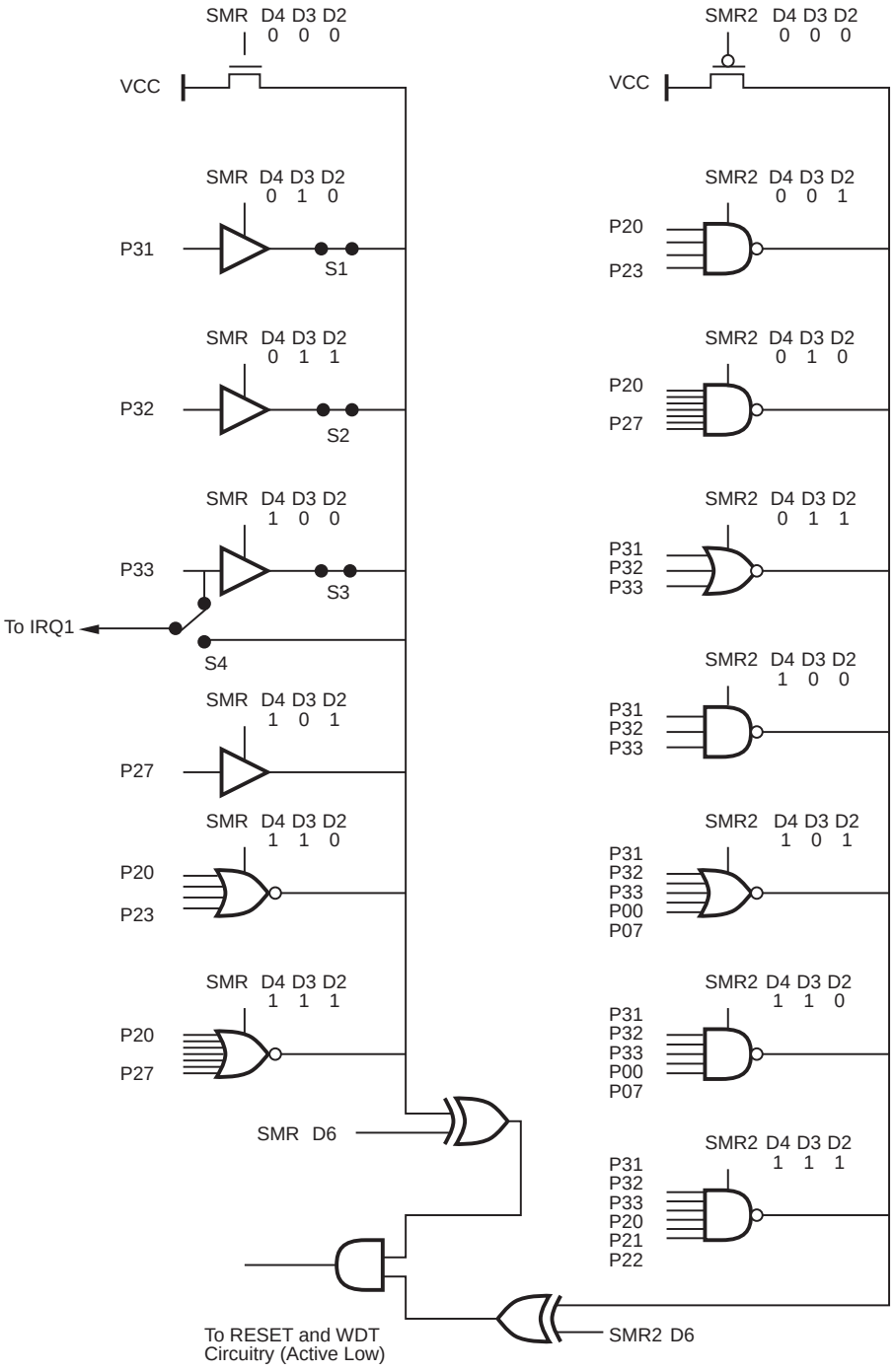


Figure 40. Stop-Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a Divide-by-16 prescaler of SCLK/TCLK (Figure 41). The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT Mode (where TCLK sources interrupt logic). After Stop-Mode Recovery, this bit is set to a 0.

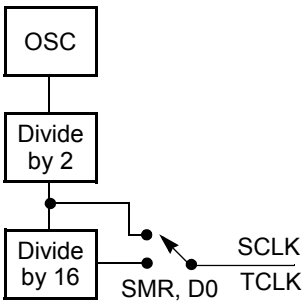


Figure 41. SCLK Circuit

Stop-Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the STOP recovery (Figure 40 on page 68 and Table 28).

Table 28. Stop-Mode Recovery Source

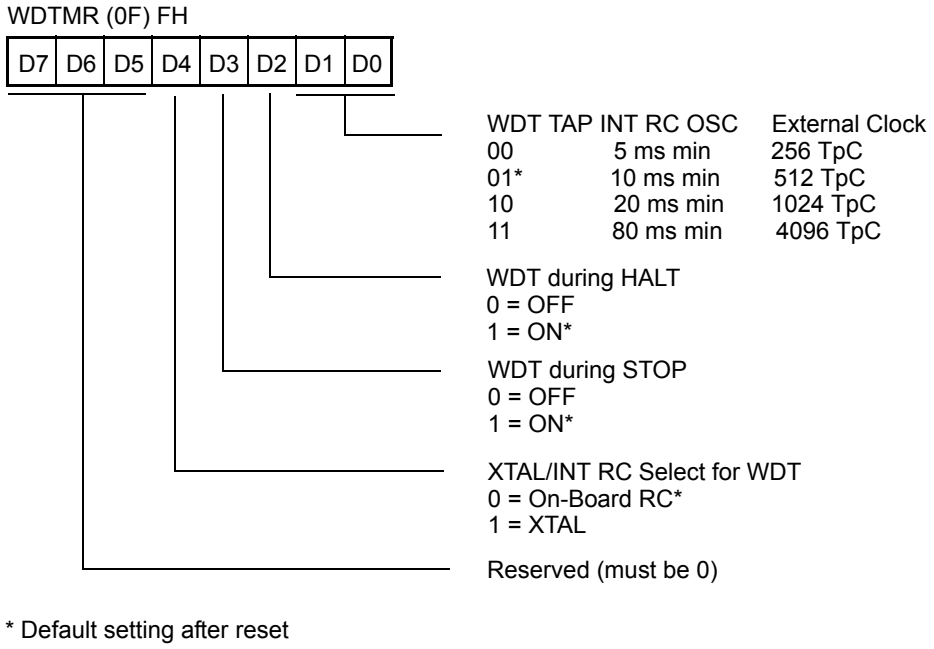
SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Note: Any Port 2 bit defined as an output drives the corresponding input to the default state to allow the remaining inputs to control the AND/OR function. Refer to “Stop-Mode Recovery Register 2 (SMR2)” on page 71 for other recovery sources.

Watch-Dog Timer Mode Register (WDTMR)

The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source is selected with bit 4 of the WDT register. Bit 0 and 1 control a tap circuit that determines the time-out period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during STOP. Bits 5 through 7 are reserved. See Figure 43.



* Default setting after reset

Figure 43. Watch-Dog Timer Mode Register—Write Only

This register is accessible only during the first 60 processor cycles (SCLK) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 40 on page 68). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register Group at address location 0FH. It is organized as shown in Figure 43.

WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as shown in Table 29.

Table 29. WDT Time Select

D1	D0	Time-Out of Internal RC OSC	Time-Out of XTAL Clock
0	0	5 ms min	256 TpC
0	1	10 ms min	512 TpC
1	0	20 ms min	1024 TpC
1	1	80 ms min	4096 TpC

Notes:
TpC = XTAL clock cycle
The default on reset is 10 ms.

WDTMR During HALT (D2)

This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1.

WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Since the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during STOP. The default is 1.

Clock Source for WDT (D4)

This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed, and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator. See Figure 44.

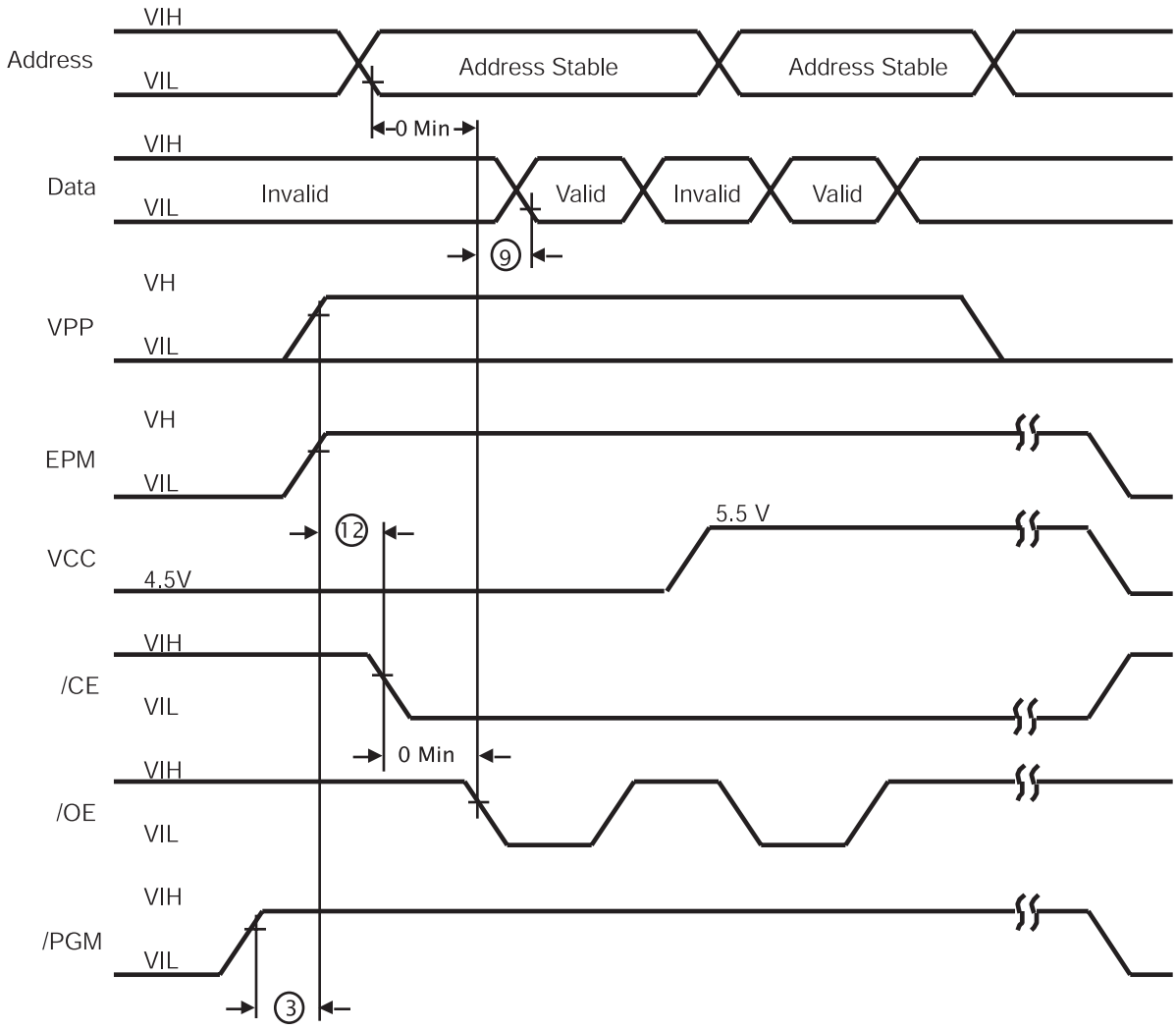


Figure 45. EPROM Read

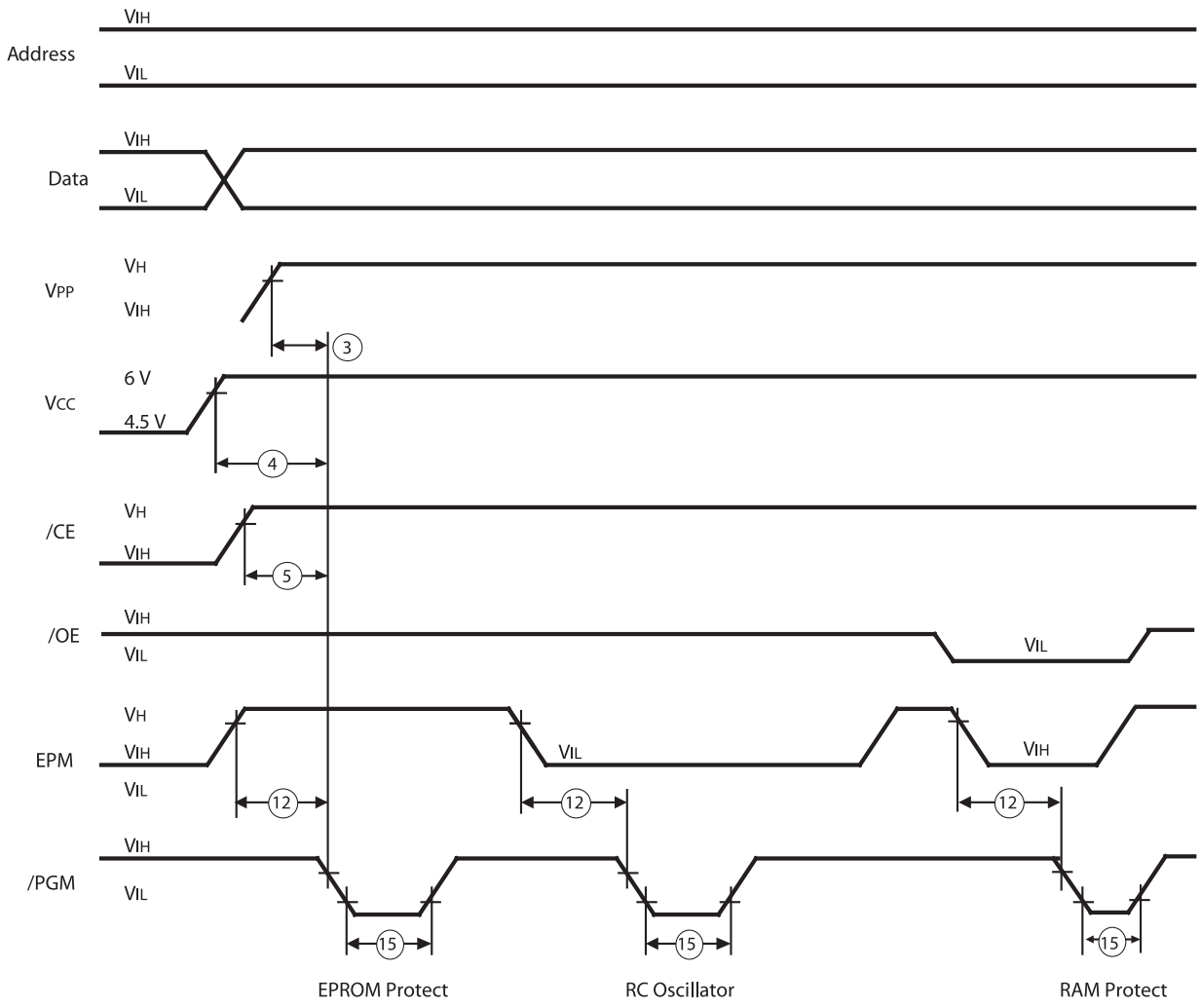


Figure 47. Programming EPROM, RAM Protect, and 16K Size Selection

Figure 48 shows the programming flowchart.

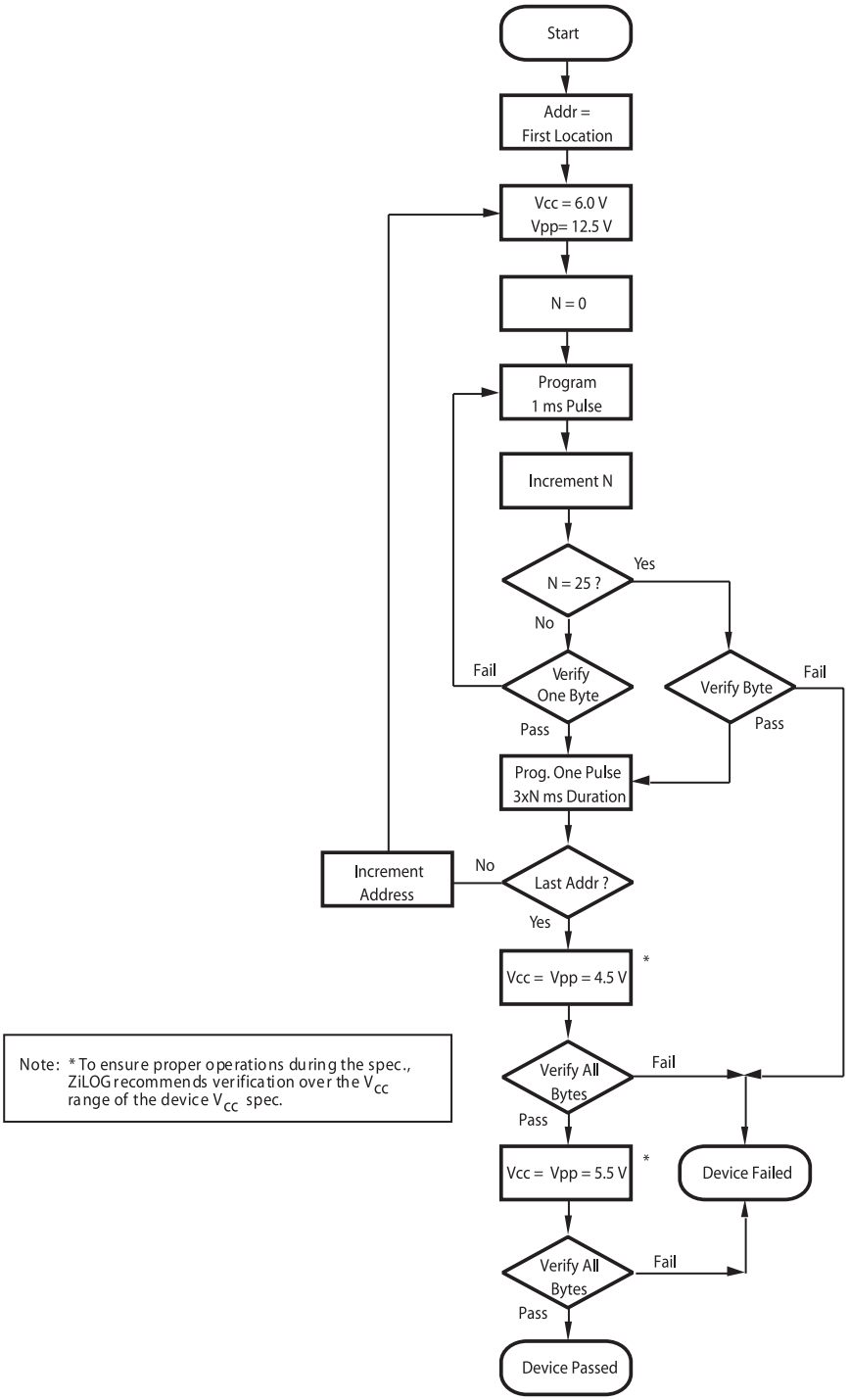


Figure 48. Programming Flowchart

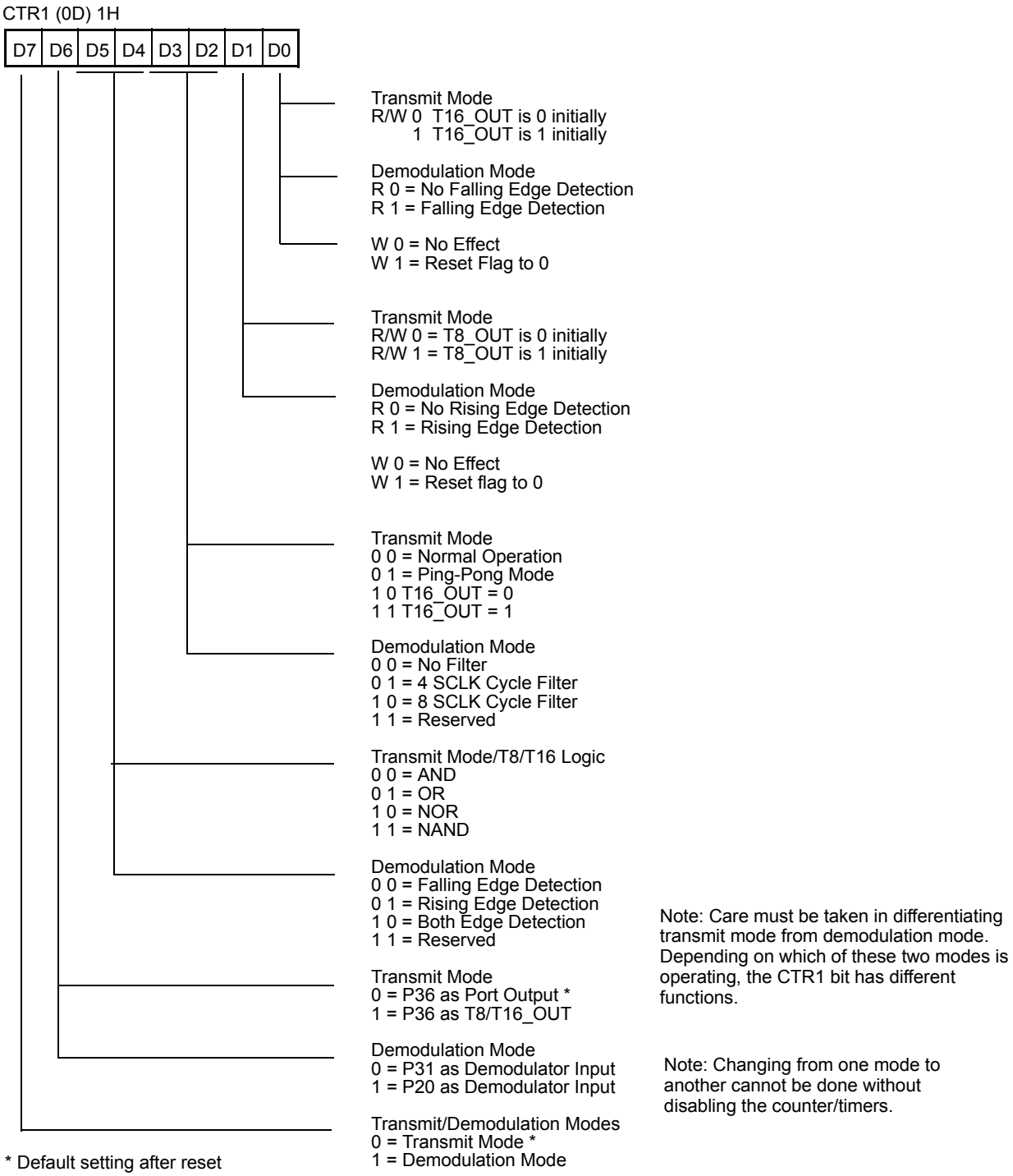


Figure 50. T8 and T16 Common Control Functions—(0D) 1H: Read/Write

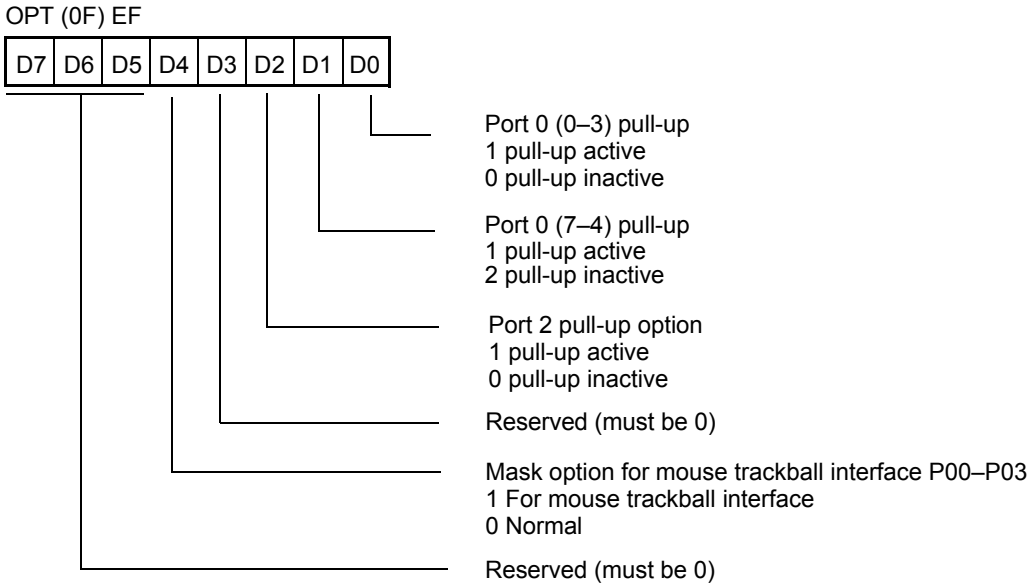
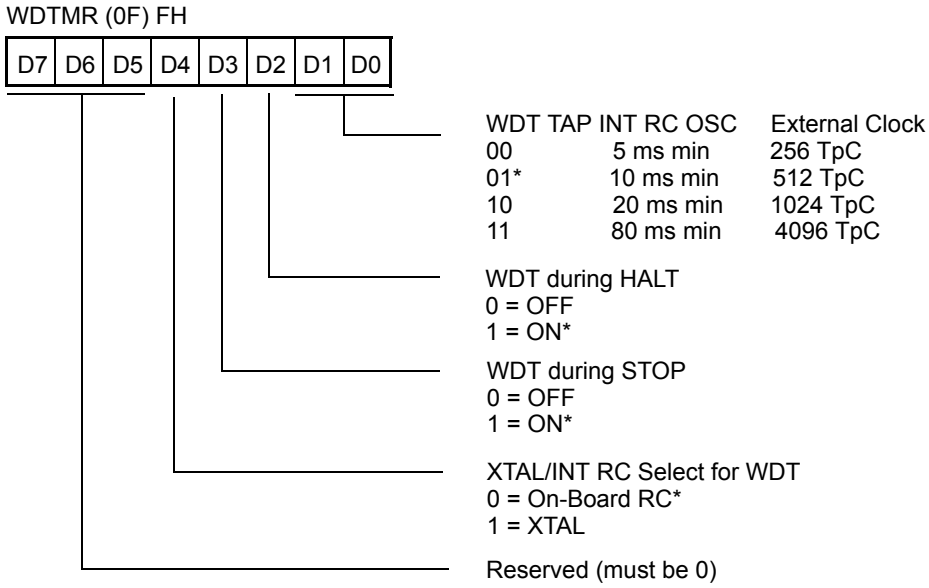


Figure 54. Option Bit Register



* Default setting after reset

Figure 55. Watch-Dog Timer Mode Register—(F) 0FH: Write Only

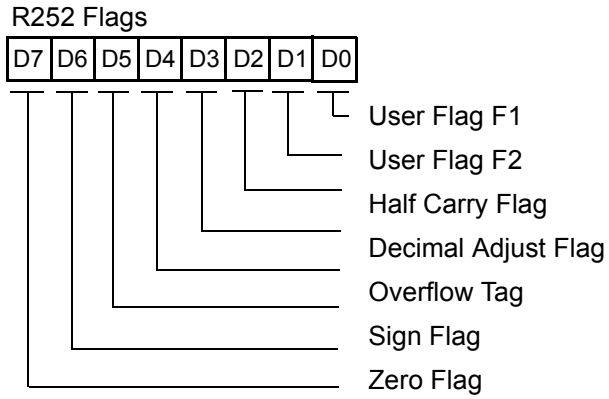


Figure 63. Flag Register—(0) FCH: Read/Write

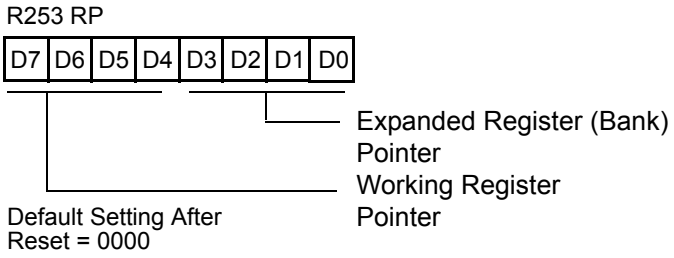


Figure 64. Register Pointer—(0) FDH: Read/Write

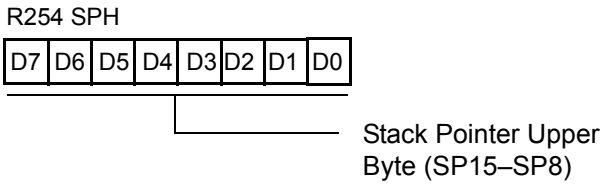
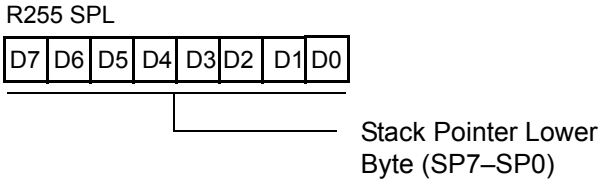


Figure 65. Stack Pointer High—(0) FEH: Read/Write



Ordering Information

Table 33 lists the ordering codes for the 16-MHz Z86E72/73.

Table 33. Ordering Codes

40-Pin DIP	44-Pin PLCC	44-Pin LQFP
Z86E7216PSC	Z86E7216VSC	Z86E7216ASC
Z86E7316PSC	Z86E7316VSC	Z86E7316ASC

Figure 70 shows an example of what the ordering codes represent.

Example:

Z 86E73 16 P S C is a Z86E73, 16 MHz, DIP, 0 °C to +70 °C, Plastic Standard

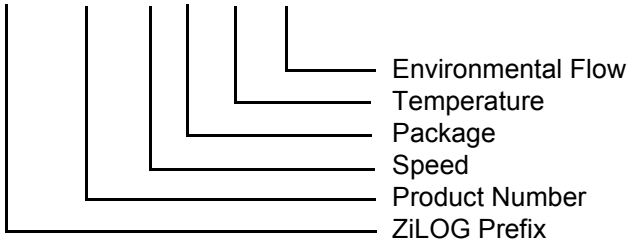


Figure 70. Ordering Codes Example

For fast results, contact your local ZiLOG sales office for assistance in ordering the part wanted.

Package

P = Plastic DIP
A = Low-profile Quad Flat Pack
V = Plastic Chip Carrier

Temperature

S = 0 °C to +70 °C

Speed

16 = 16 MHz

Environmental

C = Plastic Standard