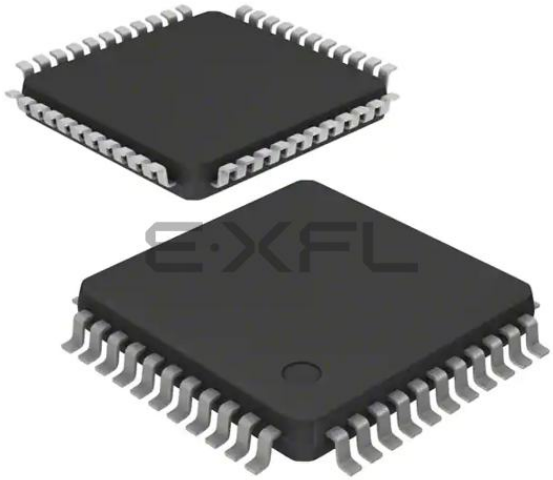

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	31
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	748 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e7216fsc00tr

Features

Table 1 lists some of the features of the Z86E72/73 microcontrollers.

Table 1. Z86E72/73 Features

Part	ROM (KB)	RAM* (Bytes)	I/O	Voltage Range
Z86E73	32	236	31	3.0 V to 5.5 V
Z86E72	16	748	31	3.0 V to 5.5 V

Note: *General-purpose

- Low power consumption—60 mW (typical)
- Two standby modes (typical)
  - STOP—2 μA
  - HALT—0.8 mA
- Special architecture to automate both generation and reception of complex pulses or signals:
  - One programmable 8-bit counter/timer with two capture registers
  - One programmable 16-bit counter/timer with one capture register
  - Programmable input glitch filter for pulse reception
- Five priority interrupts
  - Three external
  - Two assigned to counter/timers
- Two independent comparators with programmable interrupt polarity
- On-chip oscillator that accepts a crystal, ceramic resonator, LC, RC (mask option), or external clock drive
- Software-selectable 200±50% KΩ resistive transistor pull-ups on Port 0 and Port 2
  - Port 2 pull-ups are bit selectable
  - Pull-ups automatically disabled as outputs
- Software mouse/trackball interface on P00 through P03

General Description

The Z86E7X family are OTP-based members of the Z8® MCU single-chip family with 236 or 748 bytes of general-purpose RAM. The only differentiating factor between the E72/73 versions is the availability of RAM and ROM. This EPROM microcontroller family of OTP controllers also offers the use of external memory, which enables this Z8 microcontroller to be used where code flexibility is required. ZiLOG's CMOS microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and easy hardware/software system expansion along with cost-effective and low power consumption.

The Z86E7X architecture is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File to allow access to register-mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The Z8 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

Z8 applications demand powerful I/O capabilities. The Z86E7X family fulfills this with three package options in which the E72/73 versions provide 31 pins of dedicated input and output. These lines are grouped into four ports. Each port consists of eight lines (Port 3 has seven lines of I/O and one Pref comparator input) and is configurable under software control to provide timing, status signals, parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are five basic address spaces available to support a wide range of configurations: program memory, register file, Expanded Register File, Extended Data RAM, and external memory. The register file is composed of 256 bytes of RAM. It includes 4 I/O port registers, 16 control and status registers, and the rest are general-purpose registers. The Extended Data RAM adds 512 (E72) of usable general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86E7X family offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages (Figure 19 on page 34).

Note: All signals with a preceding front slash, “/”, are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

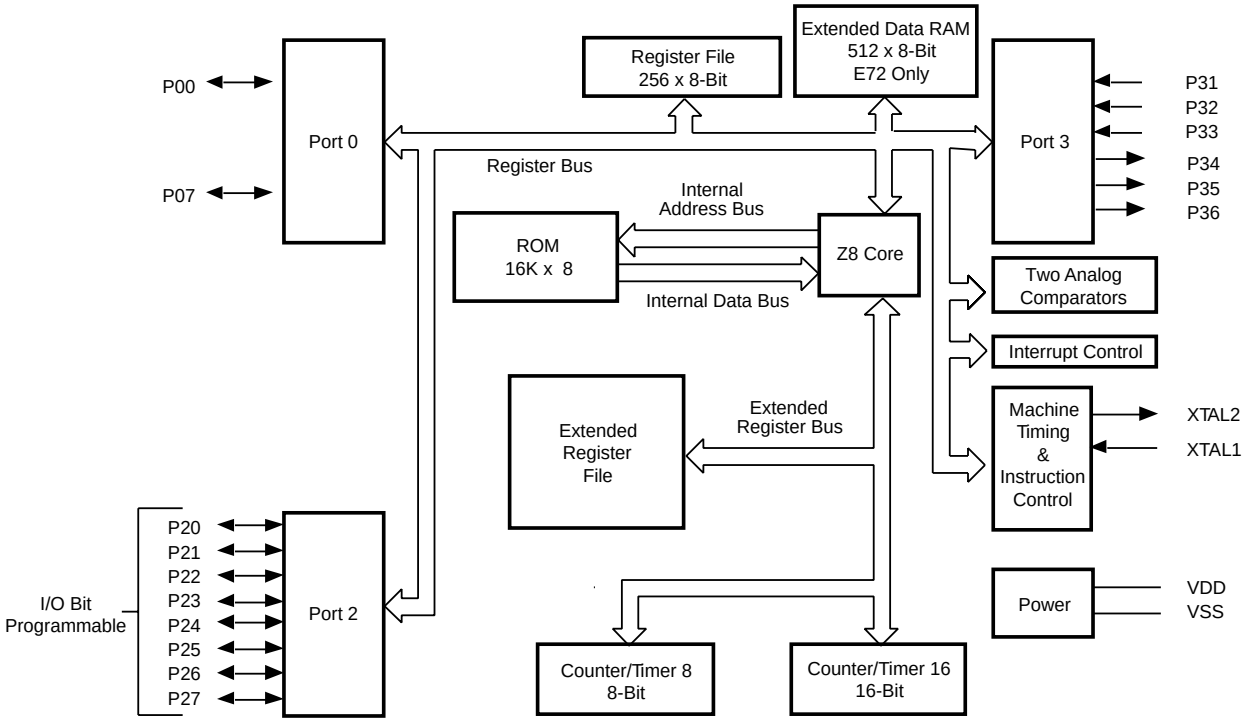

Figure 2. Z86E7X Functional Block Diagram

Table 3. Pin Identification (Standard Mode) (Continued)

40-Pin DIP #	44-Pin PLCC #	44-Pin LQFP #	Symbol	Direction	Description
14	27	10	XTAL2	Output	Crystal, Oscillator Clock
11	23, 24	6, 7	V_{DD}		Power Supply
31	1, 2, 34	17, 28, 29	V_{SS}		Ground
25	39	22	Pref1	Input	Comparator 1 Reference
NC	12	39	R//RL	Input	ROM//ROMless

Table 4. Z86E72/73 40-Pin DIP Identification—EPROM Mode

40-Pin #	Symbol	Function	Direction
1	N/C	Not Connected	
2–3	A13–14	Address 13, 14	Input
4	/PGM	Program Mode	Input
5–7	A4–A6	Address 4, 5, 6	Input
8–9	D4–D5	Data 4, 5	Input/Output
10	A7	Address 7	Input
11	V_{DD}	Power Supply	
12–13	D6–D7	Data 6, 7	Input/Output
14–15	N/C	Not Connected	
16	/OE	Output Enable	Input
17	EPM	EPROM Prog. Mode	Input
18	V_{PP}	Prog. Voltage	Input
19–24	N/C	Not Connected	
25	/CE	Chip Enable	Input
26–27	A0–A1	Address 0, 1	Input
28–29	D0–D1	Data 0, 1	Input/Output
30	A2	Address 2	Input
31	V_{SS}	Ground	
32–33	D2–D3	Data 2, 3	Input/Output

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 9).

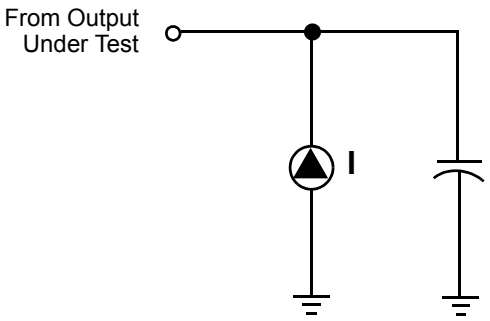

Figure 9. Test Load Diagram

Capacitance

Table 7 lists the capacitances for the Z86E72/73 microcontrollers.

Table 7. Capacitance

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

Note: T_A = 25 °C, V_{CC} = GND = 0 V, f = 1.0 MHz, unmeasured pins returned to GND.

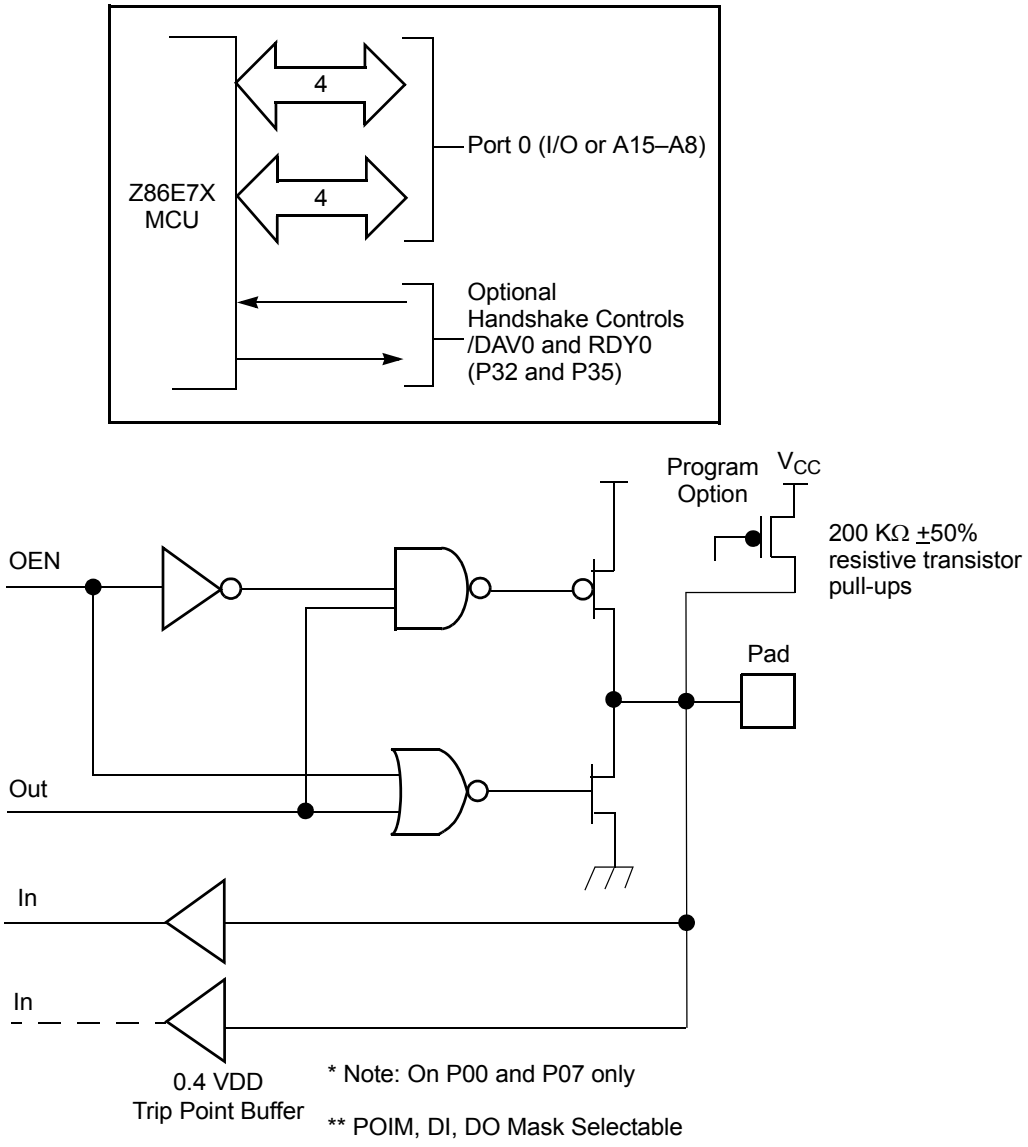

Figure 14. Port 0 Configuration

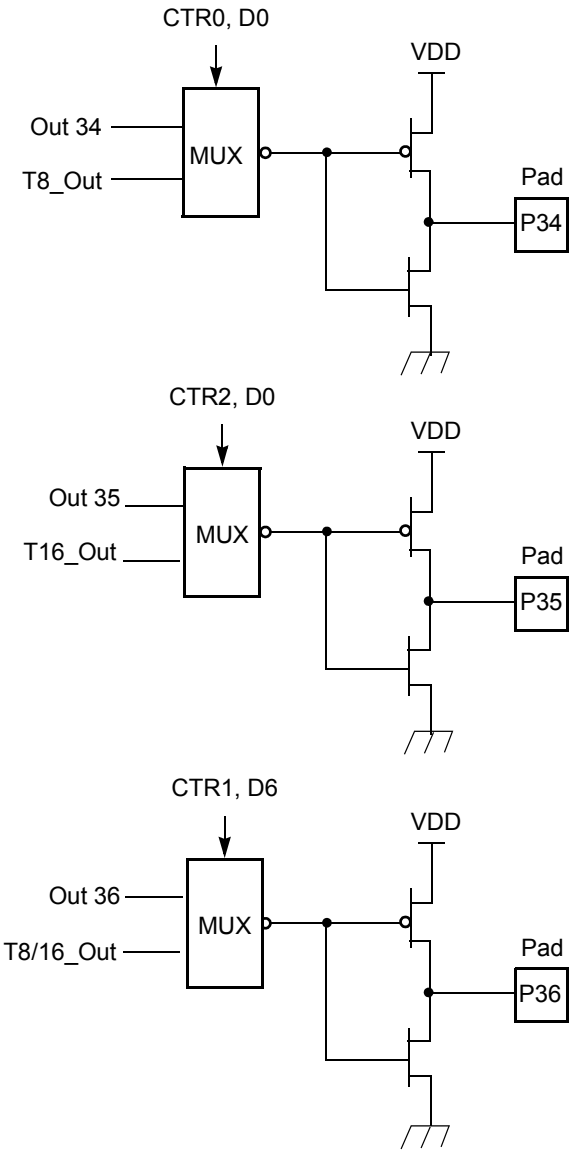

Figure 19. Port 3 Configuration

/RESET (Input, Active Low)

Reset initializes the MCU. Reset is accomplished either through Power-On, Watch-Dog Timer, Stop-Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the reset line need to be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally. There is no condition internal to the Z86E7X that does not allow an external reset to occur.

After the POR time, /RESET is a Schmitt-triggered input. To avoid asynchronous and noisy reset problems, the Z86E7X is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks or for the duration of the external reset, whichever is longer.

During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. Program execution begins at location 000CH, 5–10 TpC cycles after the RST is released. For Power-On Reset, the typical reset output time is 5 ms.

Note: The Z86E7X devices do not have internal pull resistors on Port 3 inputs.

HI16(D)09h Register

This register (Table 16) holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Table 16. HI16(D)09h Register

Field	Bit Position	Value	Description
T16_Capture_HI	76543210	R/W	Captured Data No Effect

L016(D)08h Register

This register (Table 17) holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Table 17. LO16(D)08h Register

Field	Bit Position	Value	Description
T16_Capture_LO	76543210	R/W	Captured Data No Effect

TC16H(D)07h Register

Table 18 describes the Counter/Timer2 MS-Byte Hold Register.

Table 18. TC16H(D)07h Register

Field	Bit Position	Value	Description
T16_Data_HI	76543210	R/W	Data

TC16L(D)06h Register

Table 19 describes the Counter/Timer2 LS-Byte Hold Register.

Table 19. TC16L(D)06h Register

Field	Bit Position	Value	Description
T16_Data_LO	76543210	R/W	Data

TC8H(D)05h Register

Table 20 describes the Counter/Timer8 High Hold Register.

Table 20. TC8H(D)05h Register

Field	Bit Position	Value	Description
T8_Level_HI	76543210	R/W	Data

TC8L(D)04h Register

Table 21 describes the Counter/Timer8 Low Hold Register.

Table 21. TC8L(D)04h Register

Field	Bit Position	Value	Description
T8_Level_LO	76543210	R/W	Data

CTR0(D)00h Register

Table 22 describes the Counter/Timer8 Control Register.

Table 22. CTR0(D)00h Register

Field	Bit Position		Value	Description
T8_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo	-6------	R/W	0	Modulo-N
			1	Single Pass
Time_Out	--5------	R	0	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
		W	1	Reset Flag to 0
T8 _Clock	---43---	R/W	0 0	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_MASK	-----2--	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.

Counter_INT_Mask

Set this bit to allow interrupt when T8 has a time out.

P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

CTR1(D)01h Register

This register (Table 23) controls the functions in common with the T8 and T16.

Table 23. CTR1(D)01h Register

Field	Bit Position		Value	Description
Mode	7-------	R/W	0*	Transmit Mode
			1	Demodulation Mode
P36_Out/Demodulator_Input	-6------	R/W		Transmit Mode
			0*	Port Output
			1	T8/16 Output
				Demodulation Mode
			0	P31
			1	P20
T8/T16_Logic/Edge _Detect	--54----	R/W		Transmit Mode
			0 0	AND
			0 1	OR
			1 0	NOR
			1 1	NAND
				Demodulation Mode
			0 0	Falling Edge
			0 1	Rising Edge
			1 0	Both Edges
			1 1	Reserved
Transmit_Submode/Glitch_Filter	----32--	R/W		Transmit Mode
			0 0	Normal Operation
			0 1	Ping-Pong Mode
			1 0	T16_OUT = 0
			1 1	T16_OUT = 1
				Demodulation Mode
			0 0	No Filter
			0 1	4 SCLK Cycle
			1 0	8 SCLK Cycle
			1 1	16 SCLK Cycle

Table 23. CTR1(D)01h Register (Continued)

Field	Bit Position		Value	Description
Initial_T8_Out/Rising_Edge	------1-			Transmit Mode
		R/W	0	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/Falling _Edge	-------0			Transmit Mode
		R/W	0	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

Note: * Indicates the value upon Power-On Reset.

Mode

If it is 0, the counter/timers are in the transmit mode; otherwise, they are in the demodulation mode.

P36_Out/Demodulator_Input

In transmit mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In demodulation mode, this bit defines whether the input signal to the counter/timers is from P20 or P31.

T8/T16_Logic/Edge _Detect

In transmit mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In demodulation mode, this field defines which edge needs to be detected by the edge detector.

Transmit_Submode/Glitch Filter

In transmit mode, this field defines whether T8 and T16 are in the “Ping-Pong” mode or in independent normal operation mode. Setting this field to “Normal

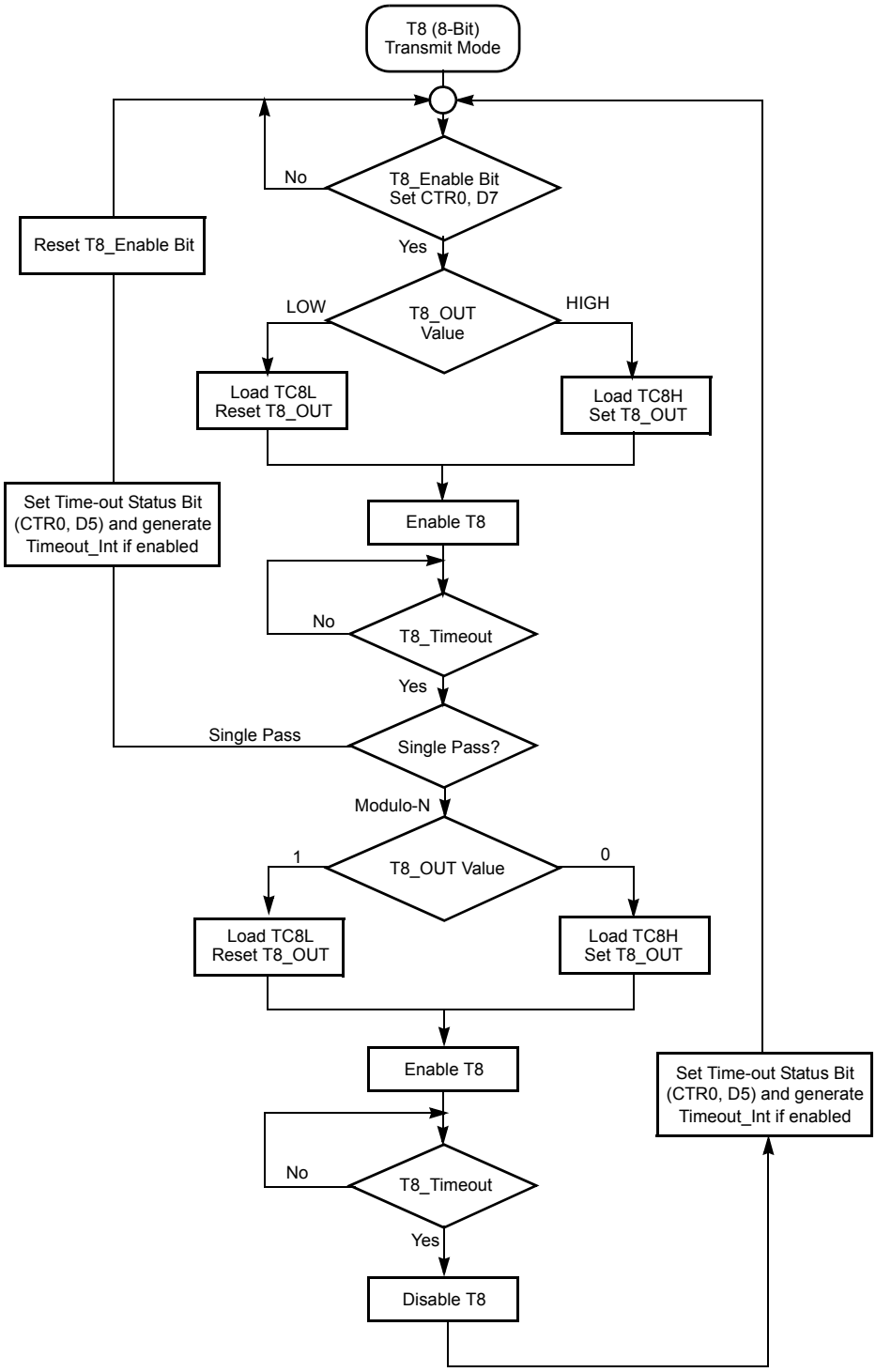

Figure 27. Transmit Mode Flowchart

If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A time out of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If D6 bit of CTR2 is toggled (by writing a 0 and then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both, depending on CTR1 D5, D4) but continues to ignore subsequent edges.

When T16 reaches 0, it continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt time-out can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in transmit mode. T8 and T16 need to be programmed in Single-Pass Mode (CTR0 D6, CTR2 D6), and Ping-Pong Mode needs to be programmed in CTR1 D3, D2. You can begin the operation by enabling either T8 or T16 (CTR0 D7 or CTR2 D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1 D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled and T16 is enabled. T16_OUT switches to its initial value (CTR1 D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, and the whole cycle repeats. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0 D1, CTR2 D1). To stop the Ping-Pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 35.

Note: Enabling Ping-Pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and then reset the status flags before instituting this operation.

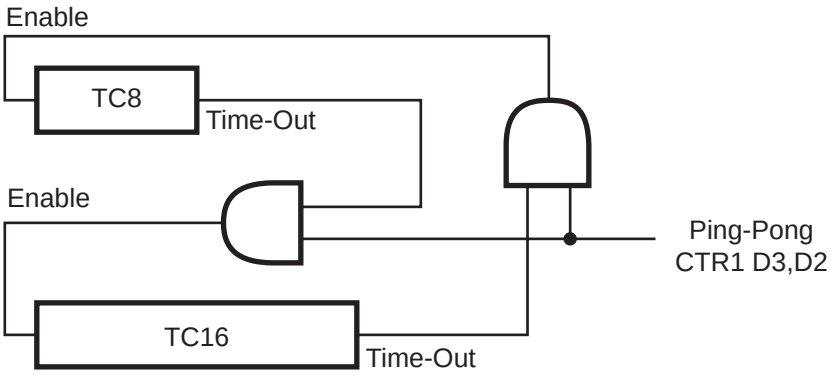

Figure 35. Ping-Pong Mode

Starting Ping-Pong Mode

First, make sure both counter/timers are not running. Then set T8 into Single-Pass Mode (CTR0 D6), set T16 into Single-Pass Mode (CTR2 D6), and set Ping-Pong Mode (CTR1 D2, D3). These instructions do not have to be in any particular order. Finally, start Ping-Pong Mode by enabling either T8 (CTR0 D7) or T16 (CTR2 D7).

During Ping-Pong Mode

The enable bits of T8 and T16 (CTR0 D7, CTR2 D7) are alternately set and cleared by hardware. The time-out bits (CTR0 D5, CTR2 D5) are set every time the counter/timers reach the terminal count.

Output Circuit

Figure 36 shows the output circuit.

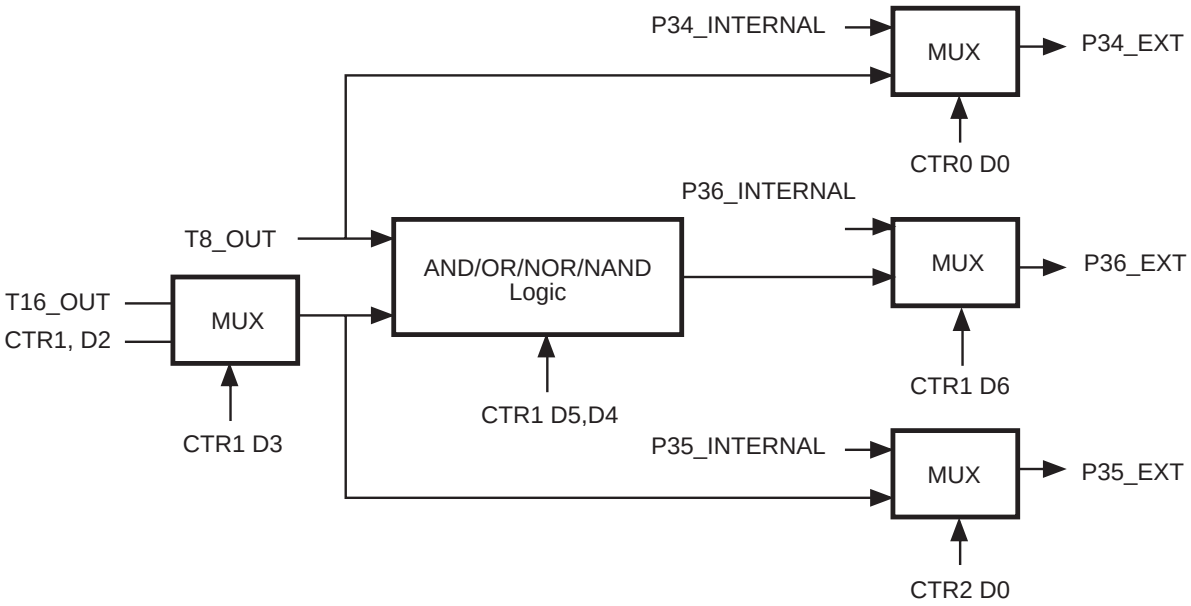

Figure 36. Output Circuit

Interrupts

The Z86E7X has five different interrupts. The interrupts are maskable and prioritized, as shown in Figure 37. The five sources are divided as follows: three sources are claimed by Port 3 lines P33–P31 and the remaining two by the counter/timers (see Table 26). The Interrupt Mask Register globally or individually enables or disables the five interrupt requests.

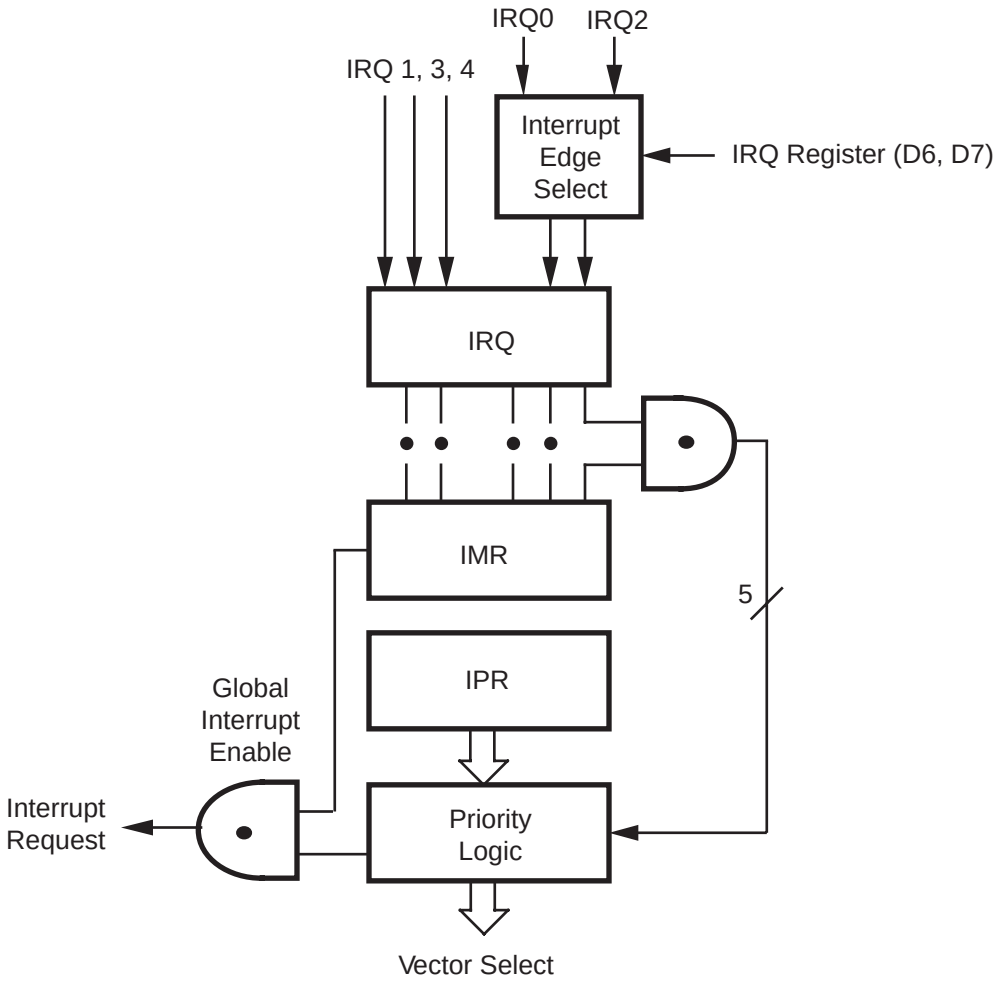

Figure 37. Interrupt Block Diagram

Table 26. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rising Falling Edge Triggered
IRQ1	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	/DAV2, IRQ2, T_{IN}	4,5	External (P31), Rising Falling Edge Triggered
IRQ3	T16	6, 7	Internal
IRQ4	T8	8, 9	Internal

WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as shown in Table 29.

Table 29. WDT Time Select

D1	D0	Time-Out of Internal RC OSC	Time-Out of XTAL Clock
0	0	5 ms min	256 TpC
0	1	10 ms min	512 TpC
1	0	20 ms min	1024 TpC
1	1	80 ms min	4096 TpC

Notes:
TpC = XTAL clock cycle
The default on reset is 10 ms.

WDTMR During HALT (D2)

This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1.

WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Since the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during STOP. The default is 1.

Clock Source for WDT (D4)

This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed, and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator. See Figure 44.

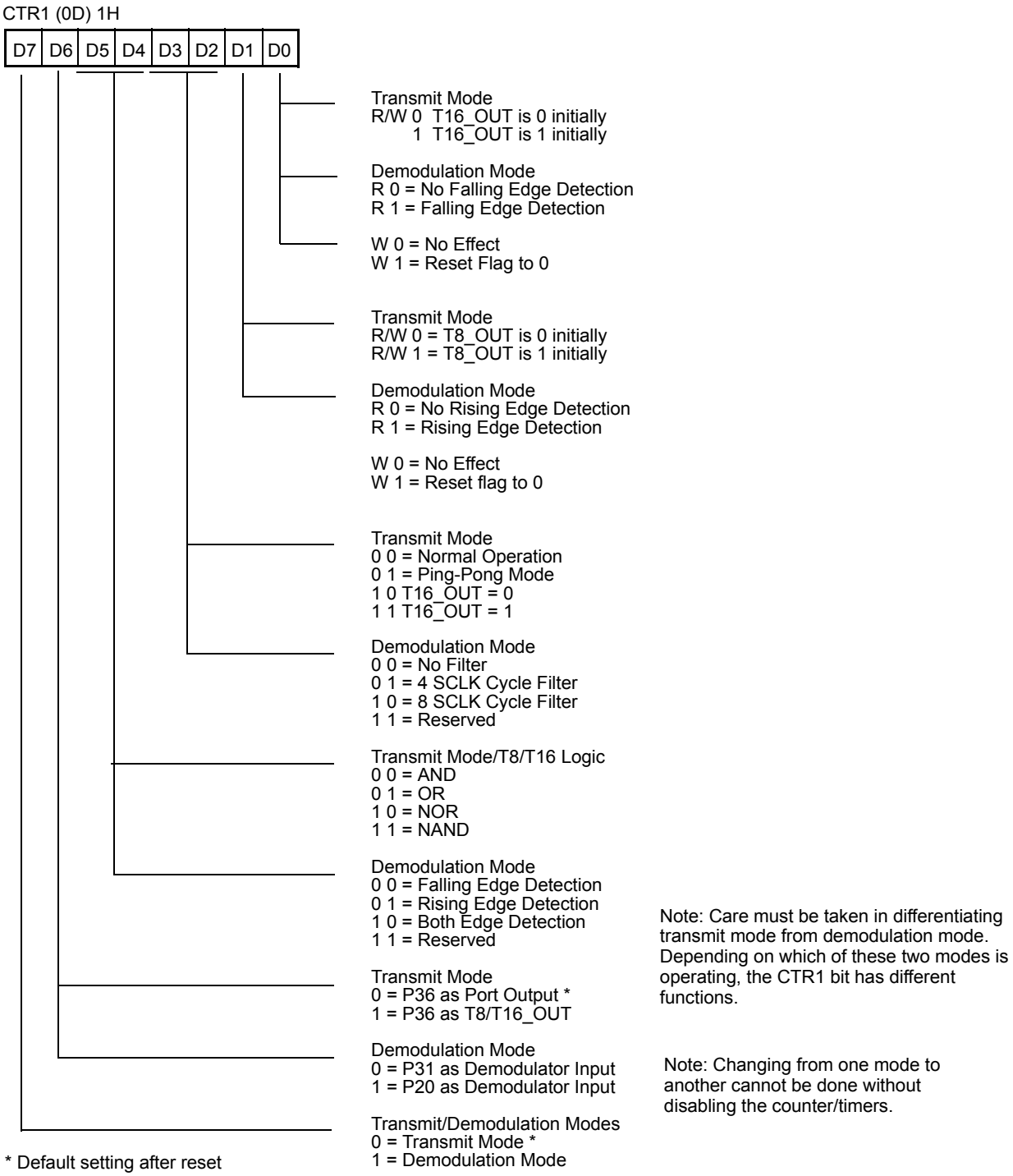

Figure 50. T8 and T16 Common Control Functions—(0D) 1H: Read/Write

Z8 Standard Control Register Diagrams

Figure 58 through Figure 66 show the Z8 standard control register diagrams.

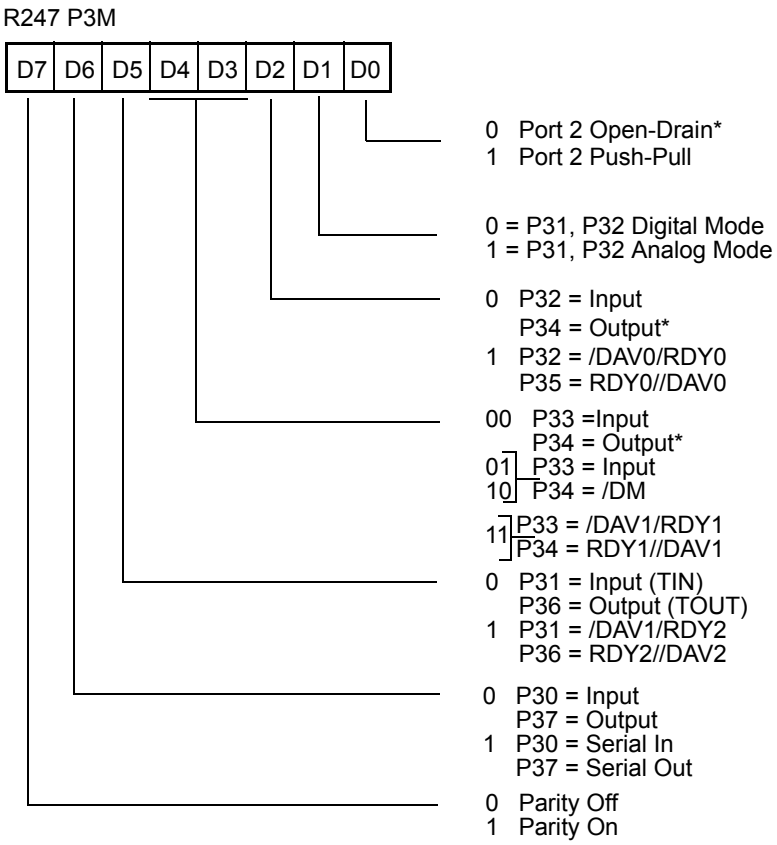

Figure 58. Port 3 Mode Register—F7H: Write Only

Figure 66. Stack Pointer Low—(0) FFH: Read/Write