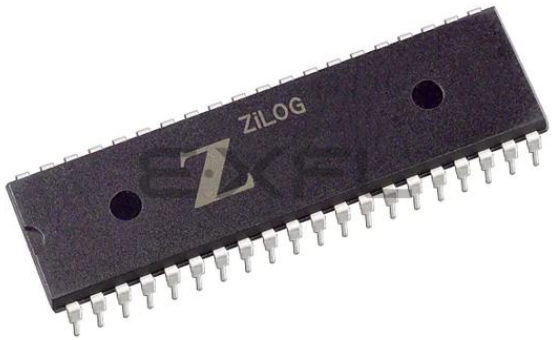

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	31
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	748 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e7216psc

General Description

The Z86E7X family are OTP-based members of the Z8® MCU single-chip family with 236 or 748 bytes of general-purpose RAM. The only differentiating factor between the E72/73 versions is the availability of RAM and ROM. This EPROM microcontroller family of OTP controllers also offers the use of external memory, which enables this Z8 microcontroller to be used where code flexibility is required. ZiLOG's CMOS microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and easy hardware/software system expansion along with cost-effective and low power consumption.

The Z86E7X architecture is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File to allow access to register-mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The Z8 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

Z8 applications demand powerful I/O capabilities. The Z86E7X family fulfills this with three package options in which the E72/73 versions provide 31 pins of dedicated input and output. These lines are grouped into four ports. Each port consists of eight lines (Port 3 has seven lines of I/O and one Pref comparator input) and is configurable under software control to provide timing, status signals, parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are five basic address spaces available to support a wide range of configurations: program memory, register file, Expanded Register File, Extended Data RAM, and external memory. The register file is composed of 256 bytes of RAM. It includes 4 I/O port registers, 16 control and status registers, and the rest are general-purpose registers. The Extended Data RAM adds 512 (E72) of usable general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86E7X family offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages (Figure 19 on page 34).

Note: All signals with a preceding front slash, “/”, are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

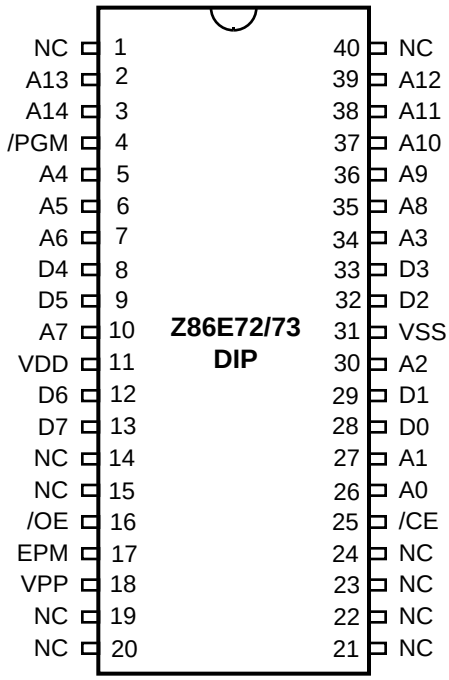


Figure 4. 40-Pin DIP Pin Assignments (EPROM Mode)

Figure 5 on page 7 shows the pin assignments for the standard mode of the 44-pin plastic leaded chip carrier (PLCC). Figure 6 on page 7 displays the pin assignments for the EPROM mode of the 44-pin PLCC.

Table 4. Z86E72/73 40-Pin DIP Identification—EPROM Mode (Continued)

40-Pin #	Symbol	Function	Direction
34	A3	Address 3	Input
35–39	A8–A12	Address 8, 9, 10, 11, 12	Input
40	N/C	Not Connected	

Table 5. Z86E72/73 44-Pin LQFP/PLCC Pin Identification—EPROM Mode

44-Pin LQFP	44-Pin PLCC	Symbol	Function	Direction
1–2	18–19	A5–A6	Address 5, 6	Input
3–4	20–21	D4–D5	Data 4, 5	Input/Output
5	22	A7	Address 7	Input
6–7	23–24	V_{DD}	Power Supply	
8–9	25–26	D6–D7	Data 6, 7	Input/Output
10	27	XTAL2	Crystal Oscillator Clock	
11	28	XTAL1	Crystal Oscillator Clock	
12	29	/OE	Output Enable	Input
13	30	EPM	EPROM Prog. Mode	Input
14	31	V_{PP}	Prog. Voltage	Input
15–16	32–33	N/C	Not Connected	
17	34	V_{SS}	Ground	
18–21	35–38	N/C	Not Connected	
22	39	/CE	Chip Select	Input
23–24	40–41	A0–A1	Address 0, 1	Input
25–26	42–43	D0–D1	Data 0, 1	Input/Output
27	44	A2	Address 2	Input
28–29	1–2	V_{SS}	Ground	
30–31	3–4	D2–D3	Data 2, 3	Input/Output
32	5	A3	Address 3	Input
33–37	6–10	A8–A12	Address 8, 9, 10, 11, 12	Input
38–40	11–13	N/C	Not Connected	

Table 9. External I/O or Memory Read and Write Timing

				T_A = 0 °C to +70 °C 16 MHz			
No.	**Symbol**	**Parameter**	**V_{CC}**	**Min.**	**Max.**	**Units**	**Notes**
1	TdA(AS)	Address Valid to /AS Rising Delay	3.0 V 5.5 V	55 55		ns ns	2
2	TdAS(A)	/AS Rising to Address Float Delay	3.0 V 5.5 V	70 70		ns ns	2
3	TdAS(DR)	/AS Rising to Read Data Required Valid	3.0 V 5.5 V		400 400	ns ns	1, 2 1, 2
4	TwAS	/AS Low Width	3.0 V 5.5 V	80 80		ns ns	2 2
5	Td	Address Float to /DS Falling	3.0 V 5.5 V	0 0		ns ns	
6	TwDSR	/DS (Read) Low Width	3.0 V 5.5 V	300 300		ns ns	1, 2
7	TwDSW	/DS (Write) Low Width	3.0 V 5.5 V	165 165		ns ns	1, 2
8	TdDSR(DR)	/DS Falling to Read Data Required Valid	3.0 V 5.5 V		260 260	ns ns	1, 2
9	ThDR(DS)	Read Data to /DS Rising Hold Time	3.0 V 5.5 V	0 0		ns ns	
10	TdDS(A)	/DS Rising to Address Active Delay	3.0 V 5.5 V	85 95		ns ns	2
11	TdDS(AS)	/DS Rising to /AS Falling Delay	3.0 V 5.5 V	60 70		ns ns	2
12	TdR/W(AS)	R//W Valid to /AS Rising Delay	3.0 V 5.5 V	70 70		ns ns	2
13	TdDS(R/W)	/DS Rising to R//W Not Valid	3.0 V 5.5 V	70 70		ns ns	2
14	TdDW(DSW)	Write Data Valid to /DS Falling (Write) Delay	3.0 V 5.5 V	80 80		ns ns	2
15	TdDS(DW)	/DS Rising to Write Data Not Valid Delay	3.0 V 5.5 V	70 80		ns ns	2
16	TdA(DR)	Address Valid to Read Data Required Valid	3.0 V 5.5 V		475 475	ns ns	1, 2

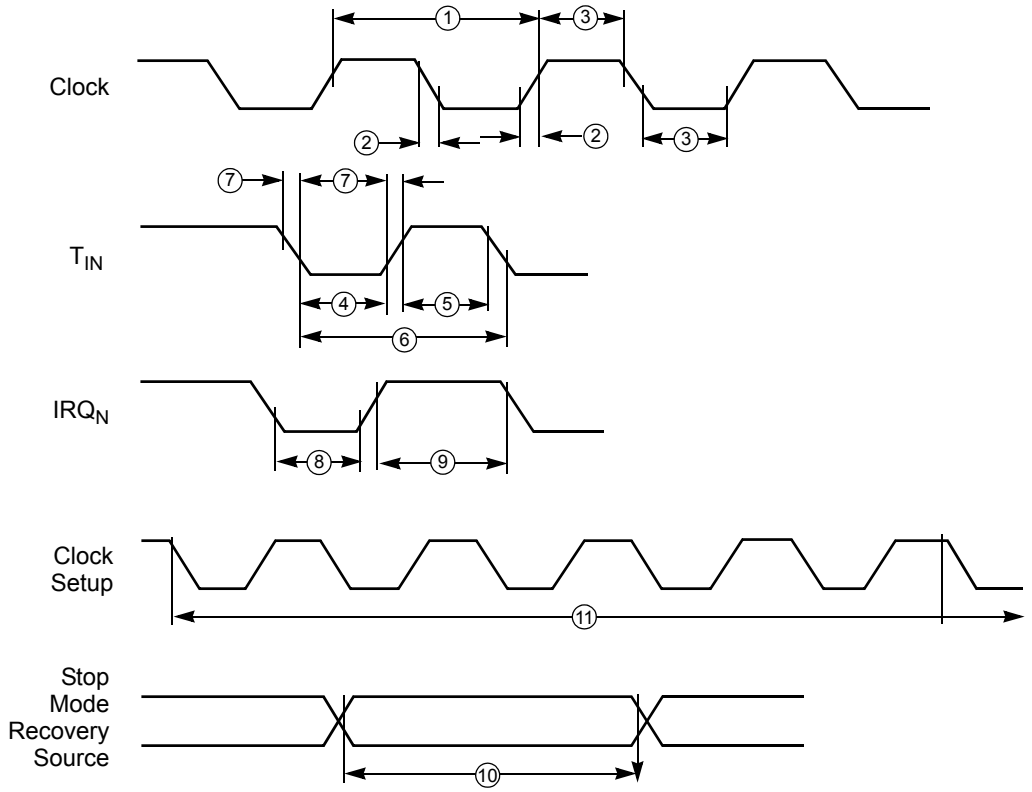


Figure 11. Additional Timing

Table 10. Additional Timing

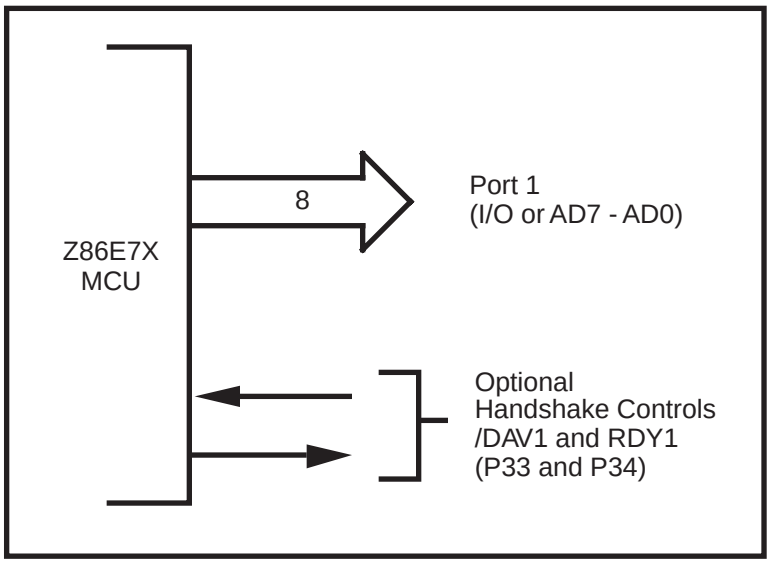
			T_A = 0°C to +70°C				
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	3.0 V 5.5 V	121 121	DC DC	ns ns	1 1
2	TrC,TfC	Clock Input Rise and Fall Times	3.0 V 5.5 V		25 25	ns ns	1 1
3	TwC	Input Clock Width	3.0 V 5.5 V	37 37		ns ns	1
4	TwTinL	Timer Input Low Width	3.0 V 5.5 V	100 70		ns ns	1
5	TwTinH	Timer Input High Width	3.0 V 5.5 V	3TpC 3TpC			1

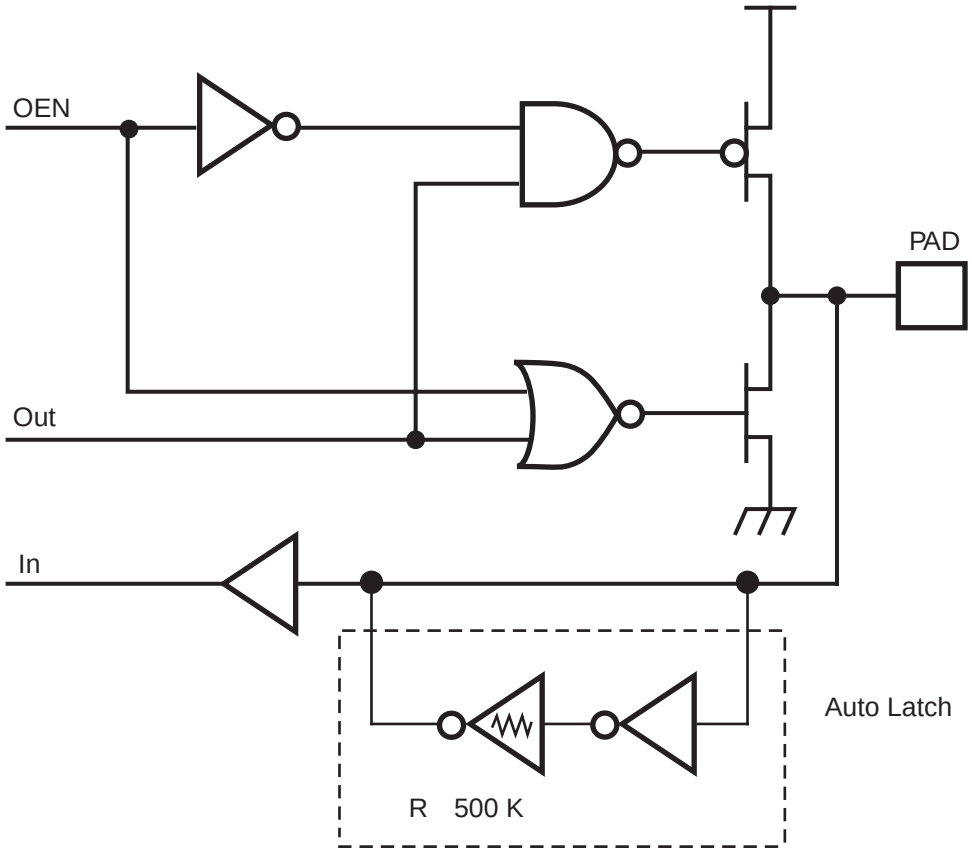
Table 10. Additional Timing (Continued)

				T_A = 0°C to +70°C			
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
6	TpTi	Timer Input Period	3.0 V 5.5 V	8TpC 8TpC			1
7	TrTin,TfTi	Timer Input Rise and Fall Timers	3.0 V 5.5 V	100 70		ns ns	1 1
8A	TwIL	Interrupt Request Low Time	3.0 V 5.5 V	100 70		ns ns	1, 2 1, 2
8B	TwIL	Int. Request Low Time	4.5 V 5.5 V	3TpC 5TpC			1, 3 1, 3
9	TwIH	Interrupt Request Input High Time	4.5 V 5.5 V	5TpC 5TpC			1, 2 1, 2
10	Twsm	Stop-Mode Recovery Width Spec	3.0 V 5.5 V 3.0 V 5.5 V	12 12 5TpC 5TpC		ns ns	7 7 6 6
11	Tost	Oscillator Start-up Time	3.0 V 5.5 V		5TpC 5TpC		4
12	Twdt	Watch-Dog Timer Delay Time (5 ms)	3.0 V 5.5 V	12 5	75 20	ms ms	
		(10 ms)	3.0 V 5.5 V	25 10	150 40	ms ms	
		(20 ms)	3.0 V 5.5 V	50 20	300 80	ms ms	
		(80 ms)	3.0 V 5.5 V	225 80	1200 320	ms ms	

Notes:
1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. Interrupt request through Port 3 (P30).
4. SMR – D5 = 0
5. Reg. WDTMR
6. Reg. SMR – D5 = 0
7. Reg. SMR – D5 = 1

Figure 12 shows the input handshake timing, and Figure 13 shows the output handshake timing. Table 11 describes the handshake timing.


Z86E7X
MCU
8
Port 1
(I/O or AD7 - AD0)
Optional
Handshake Controls
/DAV1 and RDY1
(P33 and P34)


OEN
PAD
Out
In
Auto Latch
R 500 K

The upper nibble of the register pointer (Figure 23 on page 42) selects which working register group of 16 bytes in the register file, out of the possible 256, is accessed. The lower nibble selects the expanded register file bank and, in the case of the Z86E7X family, banks 0, F, and D are implemented. A 0h in the lower nibble allows the normal register file (bank 0) to be addressed, but any other value from 1h to Fh exchanges the lower 16 registers to an expanded register bank.

For example, Z86E73 (see Figure 22):

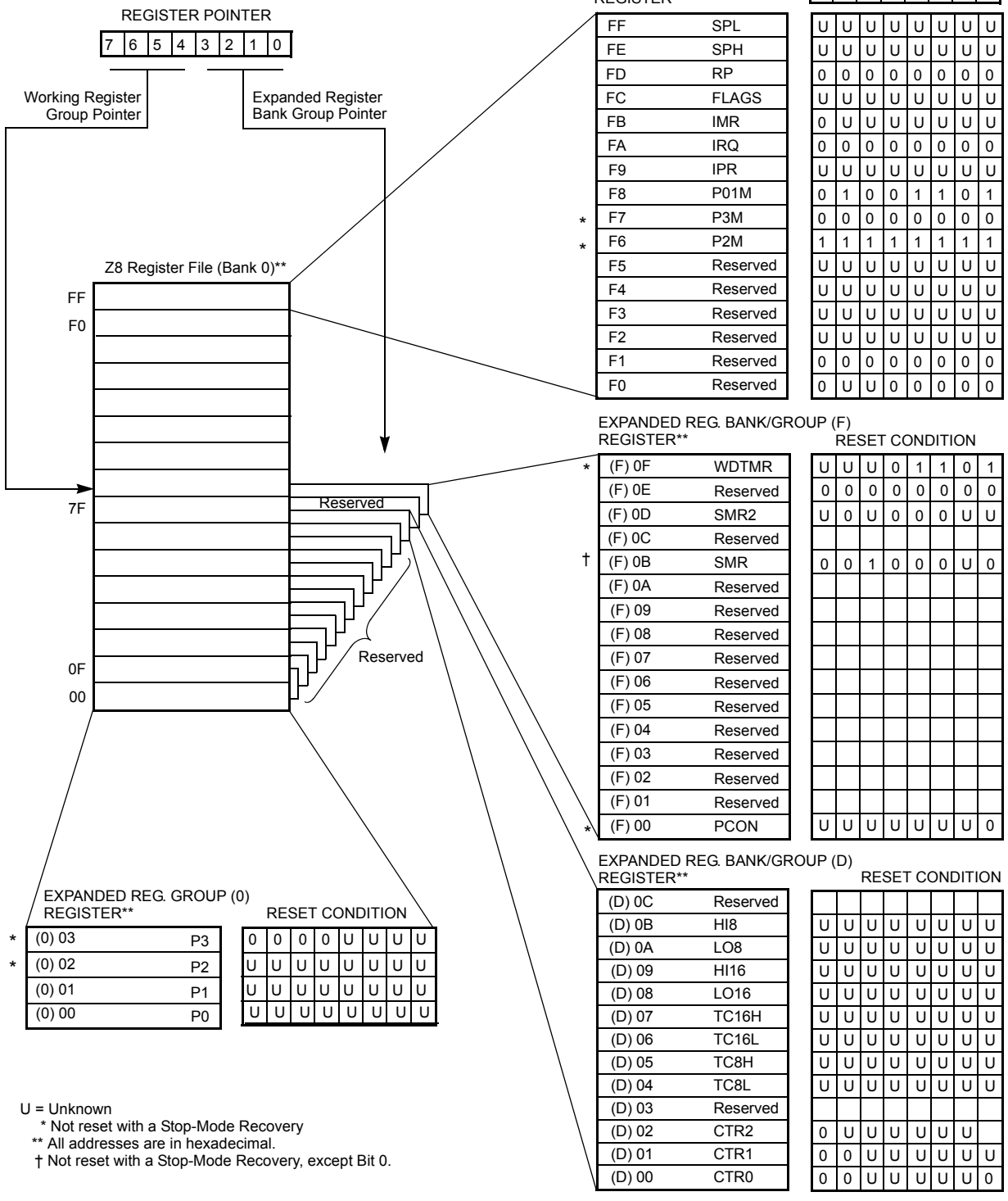
```
R253 RP = 00H
     R0 = Port0
     R1 = Port1
     R2 = Port2
     R3 = Port3
```

But if:

```
R253 RP = 0DH
     R0 = CTRL0
     R1 = CTRL1
     R2 = CTRL2
     R3 = Reserved
```

The counter/timers are mapped into ERF group D. Access is easily done using the following example:

```
LD          RP,#0Dh     ; Select ERF D for access and register
                        ; Bank 0 as the working register group.
LD          R0,#xx      ; access CTRL0
LD          1,#xx       ; access CTRL1
LD          RP,#7Dh     ; Select expanded register group (ERF)
                        ; group D for access and register
                        ; Bank 7 as the working register bank.
LD          R1,2        ; CTRL2→register 71H
```



U = Unknown
* Not reset with a Stop-Mode Recovery
** All addresses are in hexadecimal.
† Not reset with a Stop-Mode Recovery, except Bit 0.

HI16(D)09h Register

This register (Table 16) holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Table 16. HI16(D)09h Register

Field	Bit Position	Value	Description
T16_Capture_HI	76543210	R/W	Captured Data No Effect

L016(D)08h Register

This register (Table 17) holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Table 17. LO16(D)08h Register

Field	Bit Position	Value	Description
T16_Capture_LO	76543210	R/W	Captured Data No Effect

TC16H(D)07h Register

Table 18 describes the Counter/Timer2 MS-Byte Hold Register.

Table 18. TC16H(D)07h Register

Field	Bit Position	Value	Description
T16_Data_HI	76543210	R/W	Data

TC16L(D)06h Register

Table 19 describes the Counter/Timer2 LS-Byte Hold Register.

Table 19. TC16L(D)06h Register

Field	Bit Position	Value	Description
T16_Data_LO	76543210	R/W	Data

Counter_INT_Mask

Set this bit to allow interrupt when T8 has a time out.

P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

CTR1(D)01h Register

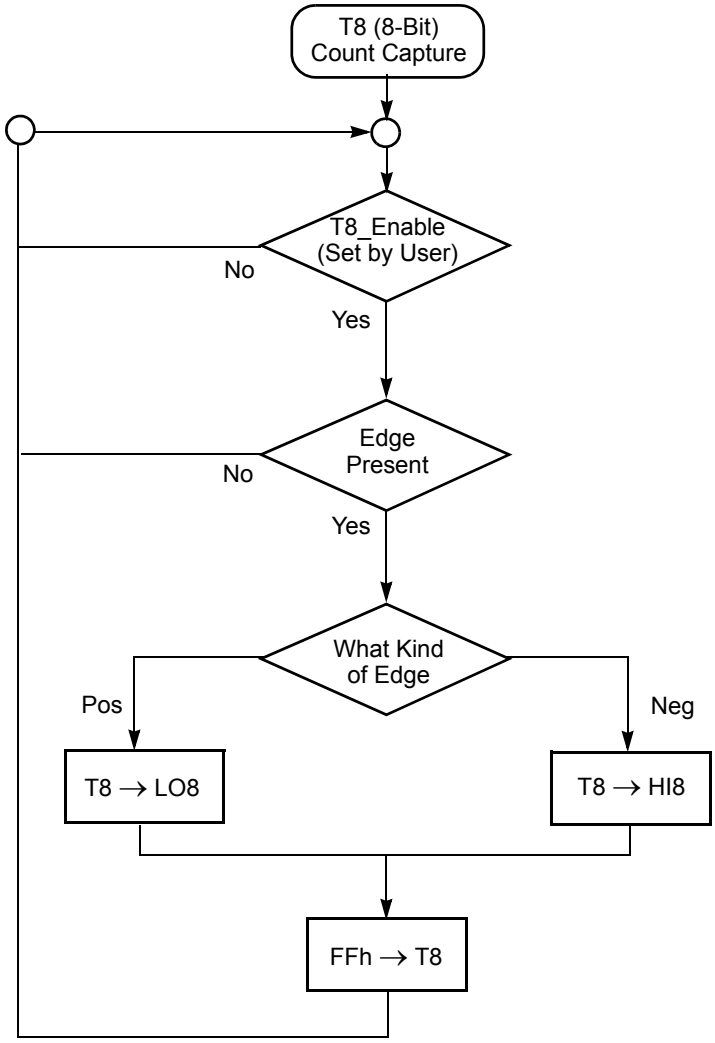
This register (Table 23) controls the functions in common with the T8 and T16.

Table 23. CTR1(D)01h Register

Field	Bit Position		Value	Description
Mode	7-------	R/W	0*	Transmit Mode
			1	Demodulation Mode
P36_Out/Demodulator_Input	-6------	R/W		Transmit Mode
			0*	Port Output
			1	T8/16 Output
				Demodulation Mode
			0	P31
			1	P20
T8/T16_Logic/Edge _Detect	--54----	R/W		Transmit Mode
			0 0	AND
			0 1	OR
			1 0	NOR
			1 1	NAND
				Demodulation Mode
			0 0	Falling Edge
			0 1	Rising Edge
			1 0	Both Edges
			1 1	Reserved
Transmit_Submode/Glitch_Filter	----32--	R/W		Transmit Mode
			0 0	Normal Operation
			0 1	Ping-Pong Mode
			1 0	T16_OUT = 0
			1 1	T16_OUT = 1
				Demodulation Mode
			0 0	No Filter
			0 1	4 SCLK Cycle
			1 0	8 SCLK Cycle
			1 1	16 SCLK Cycle

T8 Demodulation Mode

You need to program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1 D5, D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1 D5, D4) is detected during counting, the current value of T8 is one's complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if negative edge, HI8. One of the edge-detect status bits (CTR1 D1, D0) is set, and an interrupt can be generated if enabled (CTR0 D2). Meanwhile, T8 is loaded with FFh and starts counting again. When T8 reaches 0, the time-out status bit (CTR0 D5) is set, an interrupt can be generated if enabled (CTR0 D1), and T8 continues counting from FFh (see Figure 30 and Figure 31).



Starting Ping-Pong Mode

First, make sure both counter/timers are not running. Then set T8 into Single-Pass Mode (CTR0 D6), set T16 into Single-Pass Mode (CTR2 D6), and set Ping-Pong Mode (CTR1 D2, D3). These instructions do not have to be in any particular order. Finally, start Ping-Pong Mode by enabling either T8 (CTR0 D7) or T16 (CTR2 D7).

During Ping-Pong Mode

The enable bits of T8 and T16 (CTR0 D7, CTR2 D7) are alternately set and cleared by hardware. The time-out bits (CTR0 D5, CTR2 D5) are set every time the counter/timers reach the terminal count.

Output Circuit

Figure 36 shows the output circuit.

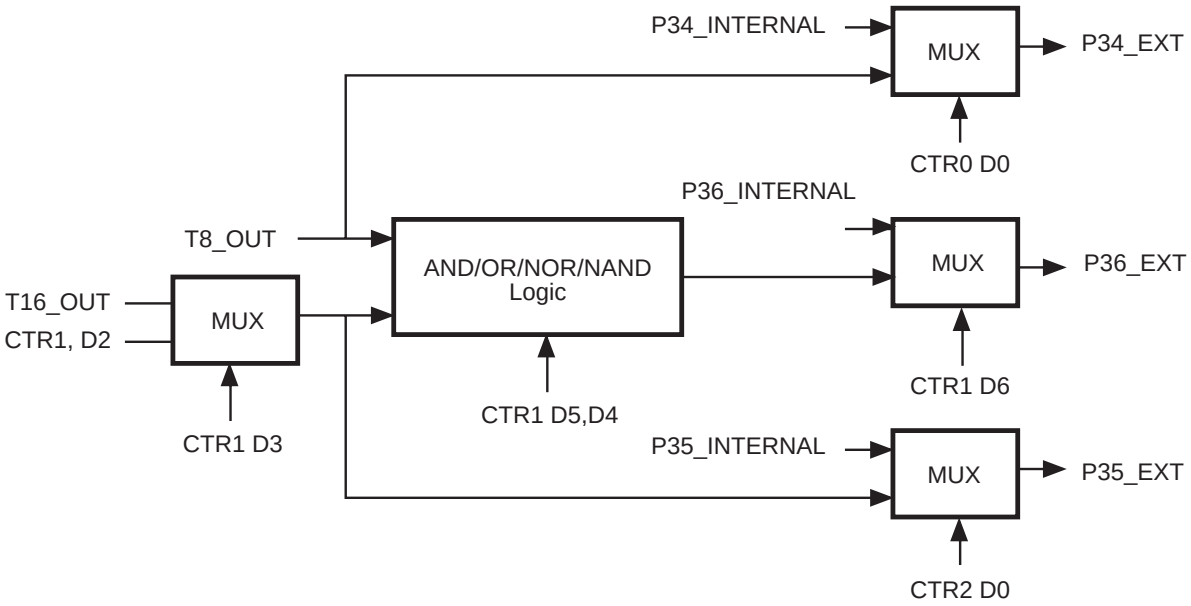


Figure 36. Output Circuit

Interrupts

The Z86E7X has five different interrupts. The interrupts are maskable and prioritized, as shown in Figure 37. The five sources are divided as follows: three sources are claimed by Port 3 lines P33–P31 and the remaining two by the counter/timers (see Table 26). The Interrupt Mask Register globally or individually enables or disables the five interrupt requests.

WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as shown in Table 29.

Table 29. WDT Time Select

D1	D0	Time-Out of Internal RC OSC	Time-Out of XTAL Clock
0	0	5 ms min	256 TpC
0	1	10 ms min	512 TpC
1	0	20 ms min	1024 TpC
1	1	80 ms min	4096 TpC

Notes:
TpC = XTAL clock cycle
The default on reset is 10 ms.

WDTMR During HALT (D2)

This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1.

WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Since the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during STOP. The default is 1.

Clock Source for WDT (D4)

This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed, and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator. See Figure 44.

Table 32 lists the timing of the programming waveform.

Table 32. Timing of Programming Waveform

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup Time	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		µs
7	Data Hold Time	2		µs
8	/OE Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	/PGM Setup Time	2		µs
14	Address to /OE Setup Time	2		µs
15	Option Program Pulse Width	78		ms

Figure 45 shows the EPROM read timing diagram. Figure 46 on page 79 shows the EPROM program and verify timing diagram. Figure 47 on page 80 shows the programming EPROM, RAM protect, and 16K size selection timing diagram.

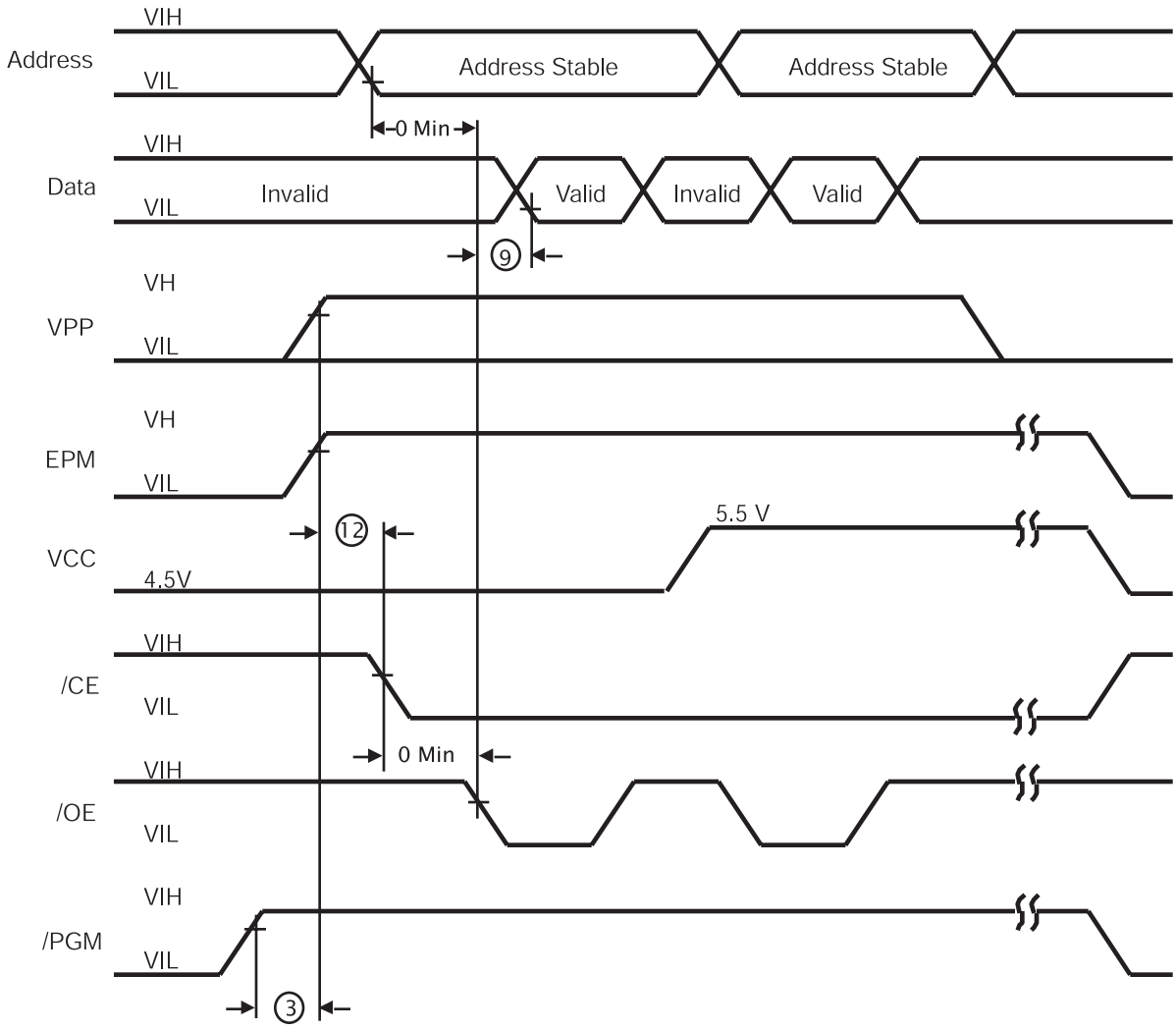


Figure 45. EPROM Read

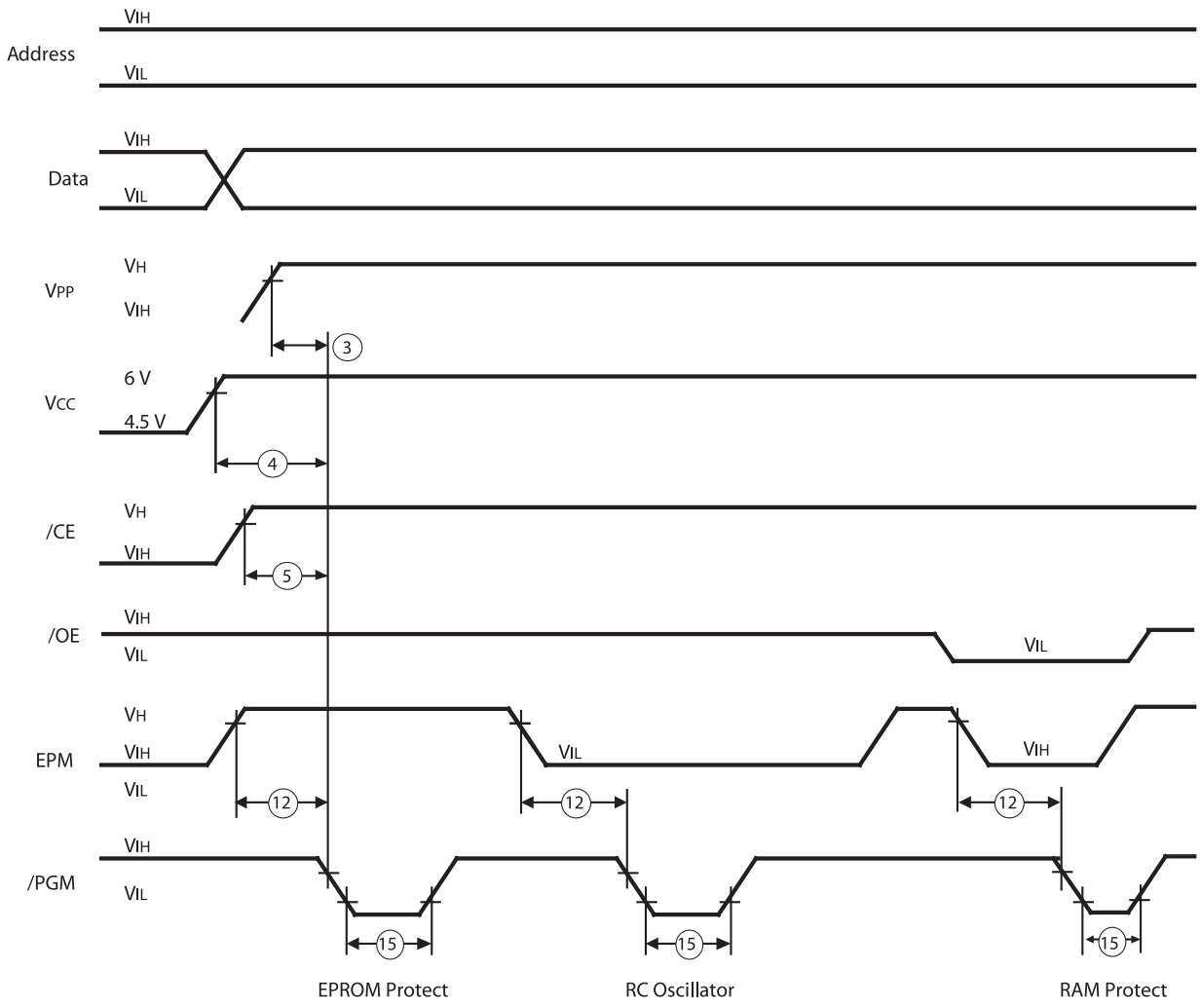


Figure 47. Programming EPROM, RAM Protect, and 16K Size Selection

Figure 48 shows the programming flowchart.

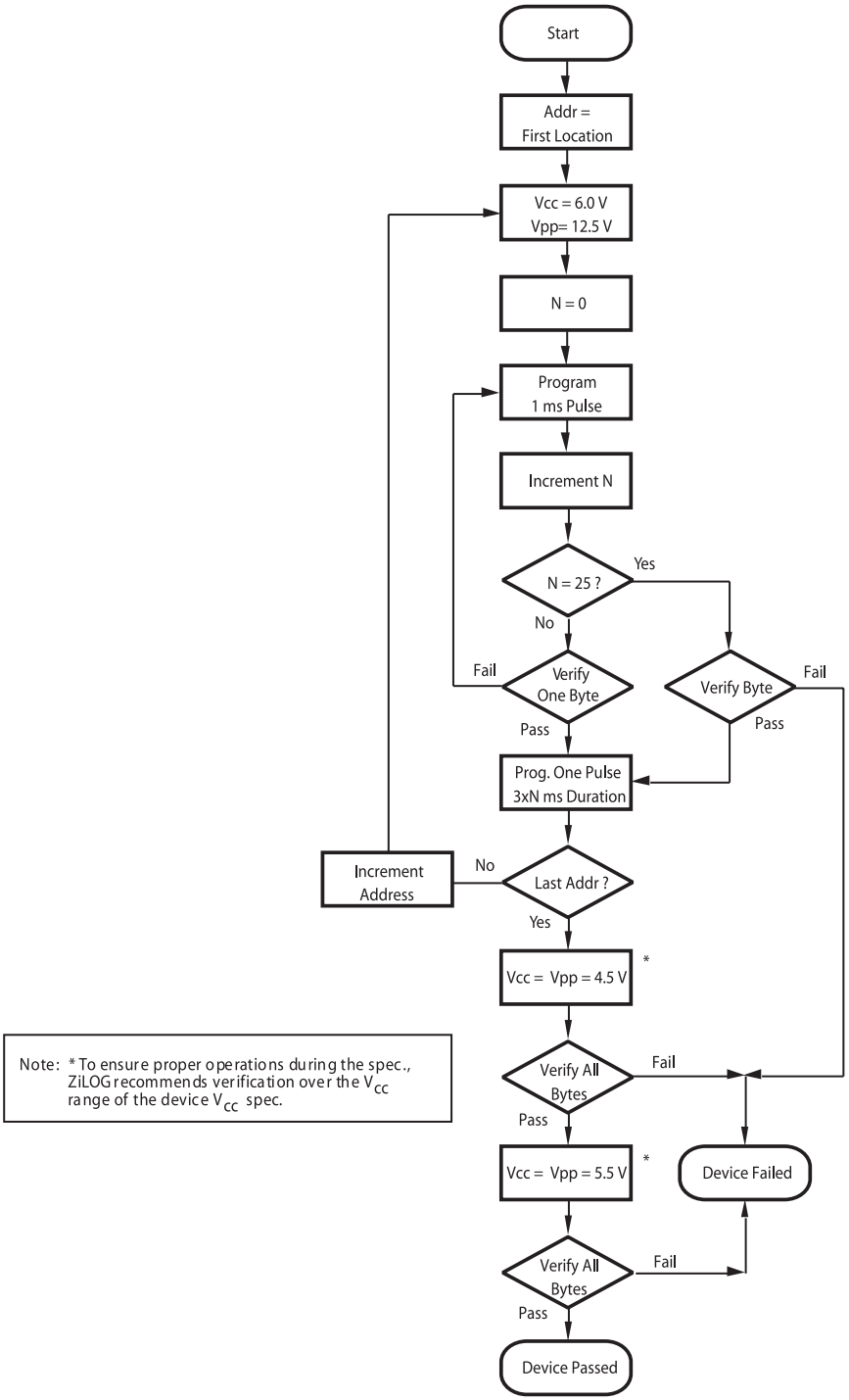


Figure 48. Programming Flowchart

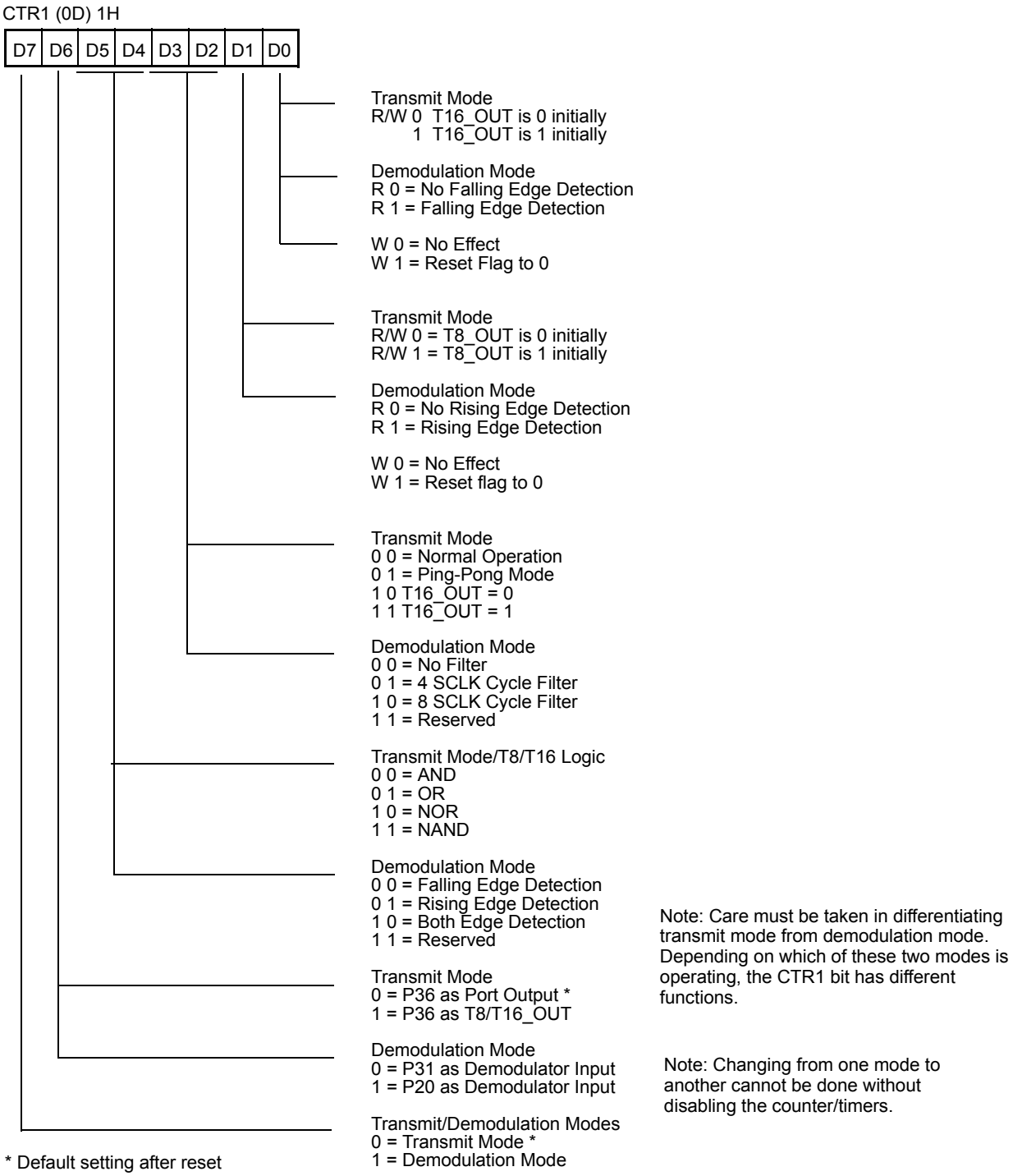


Figure 50. T8 and T16 Common Control Functions—(0D) 1H: Read/Write

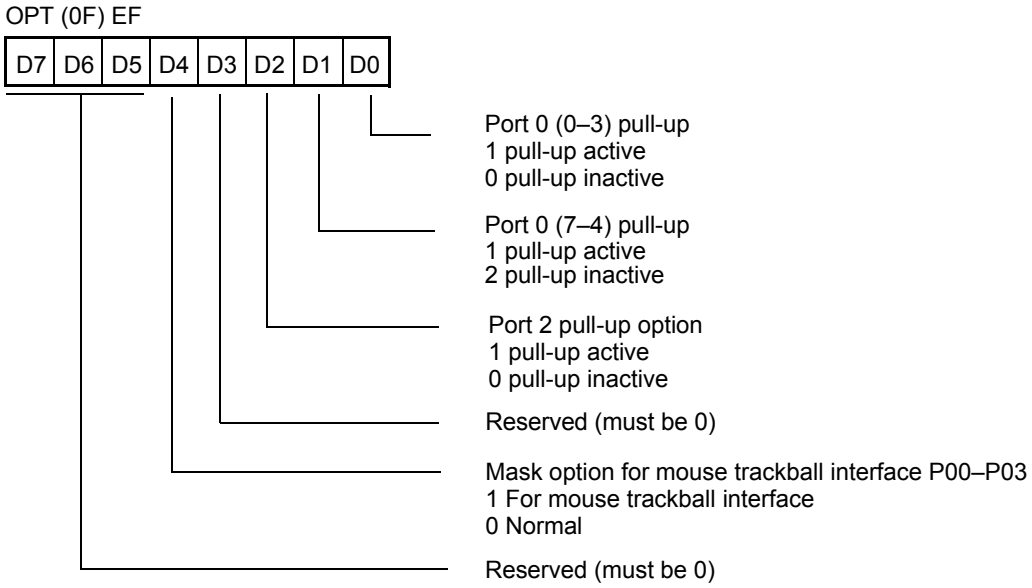
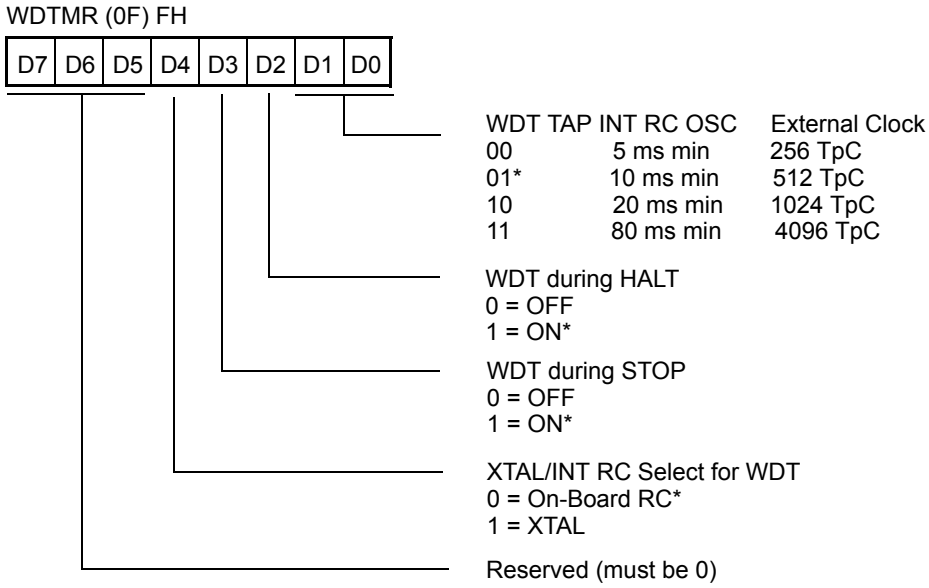


Figure 54. Option Bit Register



* Default setting after reset

Figure 55. Watch-Dog Timer Mode Register—(F) 0FH: Write Only