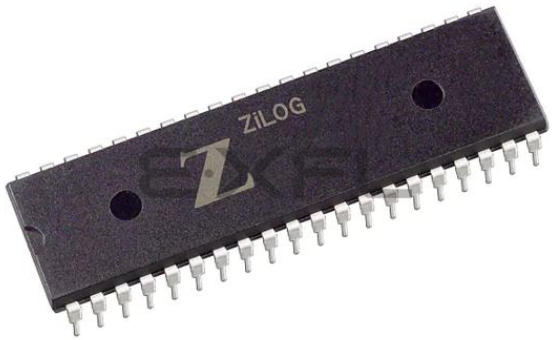

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	31
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	748 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e7216psg

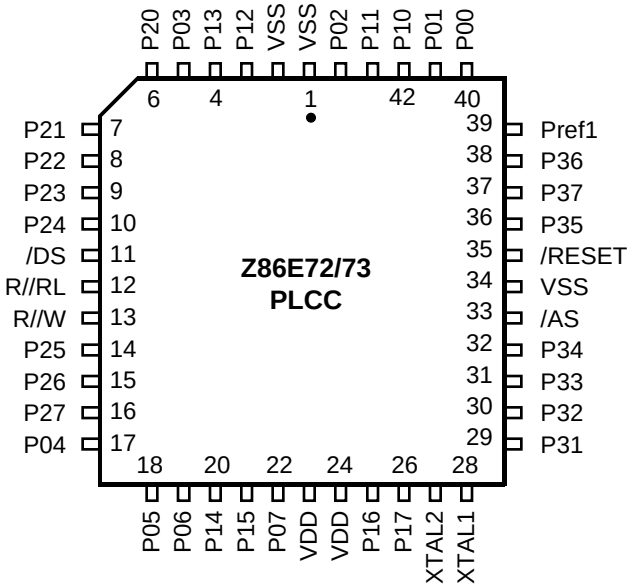


Figure 5. 44-Pin PLCC Pin Assignments (Standard Mode)

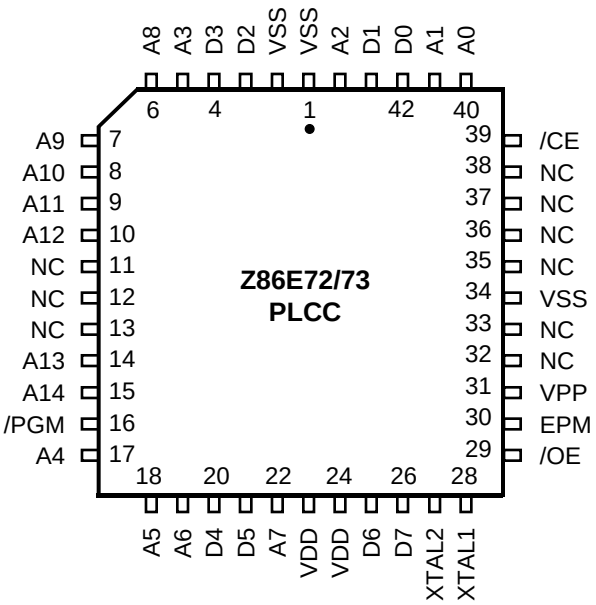


Figure 6. 44-Pin PLCC Pin Assignments (EPROM Mode)

Table 3. Pin Identification (Standard Mode) (Continued)

40-Pin DIP #	44-Pin PLCC #	44-Pin LQFP #	Symbol	Direction	Description
29	43	26	P11	Input/Output	Port 1 can be configured as multiplexed A7–A0/D7–D0 external program ROM Address/Data Bus
32	3	30	P12	Input/Output	
33	4	31	P13	Input/Output	
8	20	3	P14	Input/Output	.
9	21	4	P15	Input/Output	
12	25	8	P16	Input/Output	
13	26	9	P17	Input/Output	
35	6	33	P20	Input/Output	Port 2 pins are individually configurable as input or output
36	7	34	P21	Input/Output	
37	8	35	P22	Input/Output	
38	9	36	P23	Input/Output	
39	10	37	P24	Input/Output	
2	14	41	P25	Input/Output	
3	15	42	P26	Input/Output	
4	16	43	P27	Input/Output	
16	29	12	P31	Input	IRQ2/Modulator input
17	30	13	P32	Input	IRQ0
18	31	14	P33	Input	IRQ1
19	32	15	P34	Output	T8 output
22	36	19	P35	Output	T16 output
24	38	21	P36	Output	T8/T16 output
23	37	20	P37	Output	
20	33	16	/AS	Output	Address Strobe
40	11	38	/DS	Output	Data Strobe
1	13	40	R//W	Output	Read/Write
21	35	18	/RESET	Input	Reset
15	28	11	XTAL1	Input	Crystal, Oscillator Clock

Table 10. Additional Timing (Continued)

				T_A = 0°C to +70°C			
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
6	TpTi	Timer Input Period	3.0 V 5.5 V	8TpC 8TpC			1
7	TrTin,TfTi	Timer Input Rise and Fall Timers	3.0 V 5.5 V	100 70		ns ns	1 1
8A	TwIL	Interrupt Request Low Time	3.0 V 5.5 V	100 70		ns ns	1, 2 1, 2
8B	TwIL	Int. Request Low Time	4.5 V 5.5 V	3TpC 5TpC			1, 3 1, 3
9	TwIH	Interrupt Request Input High Time	4.5 V 5.5 V	5TpC 5TpC			1, 2 1, 2
10	Twsm	Stop-Mode Recovery Width Spec	3.0 V 5.5 V 3.0 V 5.5 V	12 12 5TpC 5TpC		ns ns	7 7 6 6
11	Tost	Oscillator Start-up Time	3.0 V 5.5 V		5TpC 5TpC		4
12	Twdt	Watch-Dog Timer Delay Time (5 ms)	3.0 V 5.5 V	12 5	75 20	ms ms	
		(10 ms)	3.0 V 5.5 V	25 10	150 40	ms ms	
		(20 ms)	3.0 V 5.5 V	50 20	300 80	ms ms	
		(80 ms)	3.0 V 5.5 V	225 80	1200 320	ms ms	

Notes:
1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. Interrupt request through Port 3 (P30).
4. SMR – D5 = 0
5. Reg. WDTMR
6. Reg. SMR – D5 = 0
7. Reg. SMR – D5 = 1

Figure 12 shows the input handshake timing, and Figure 13 shows the output handshake timing. Table 11 describes the handshake timing.

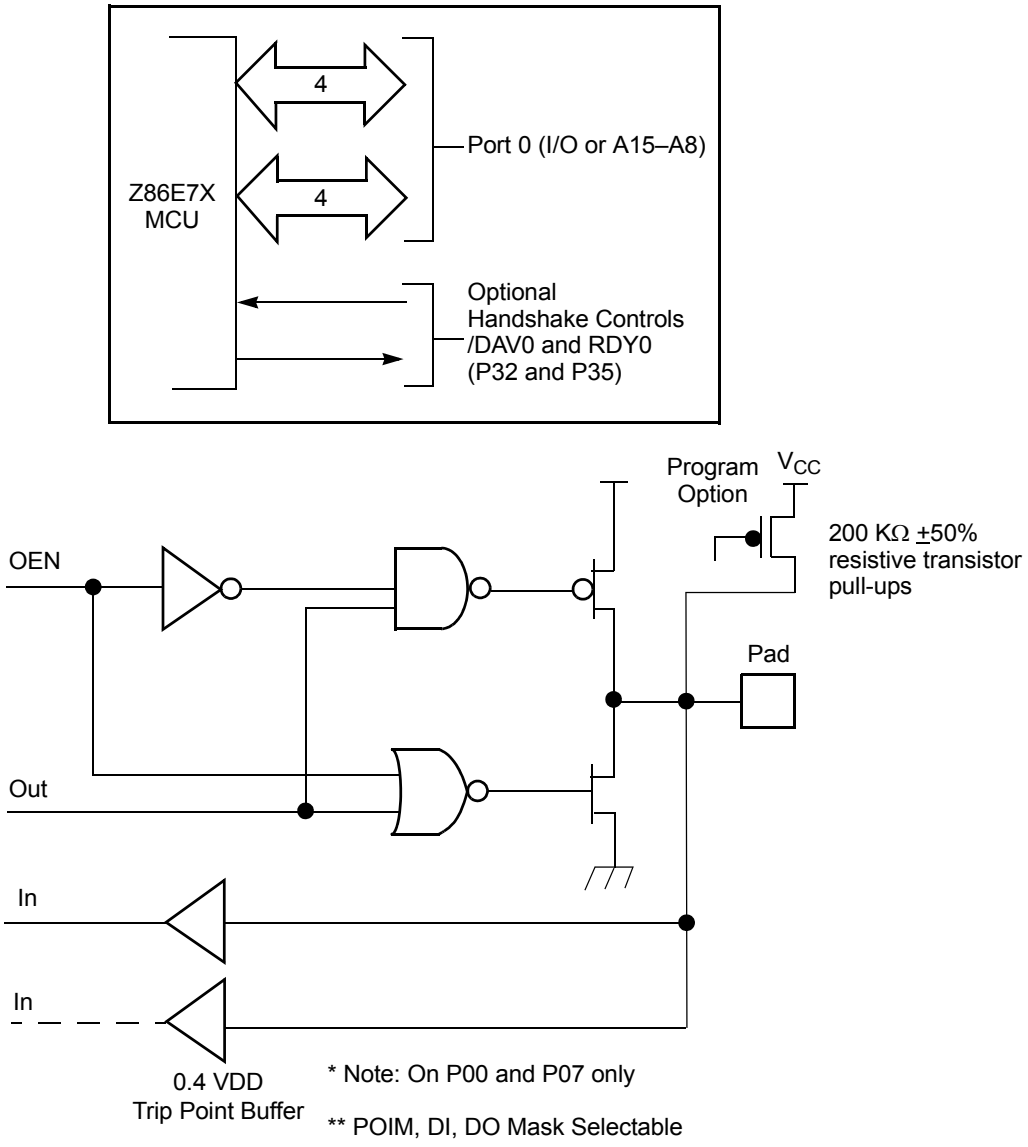


Figure 14. Port 0 Configuration

The upper nibble of the register pointer (Figure 23 on page 42) selects which working register group of 16 bytes in the register file, out of the possible 256, is accessed. The lower nibble selects the expanded register file bank and, in the case of the Z86E7X family, banks 0, F, and D are implemented. A 0h in the lower nibble allows the normal register file (bank 0) to be addressed, but any other value from 1h to Fh exchanges the lower 16 registers to an expanded register bank.

For example, Z86E73 (see Figure 22):

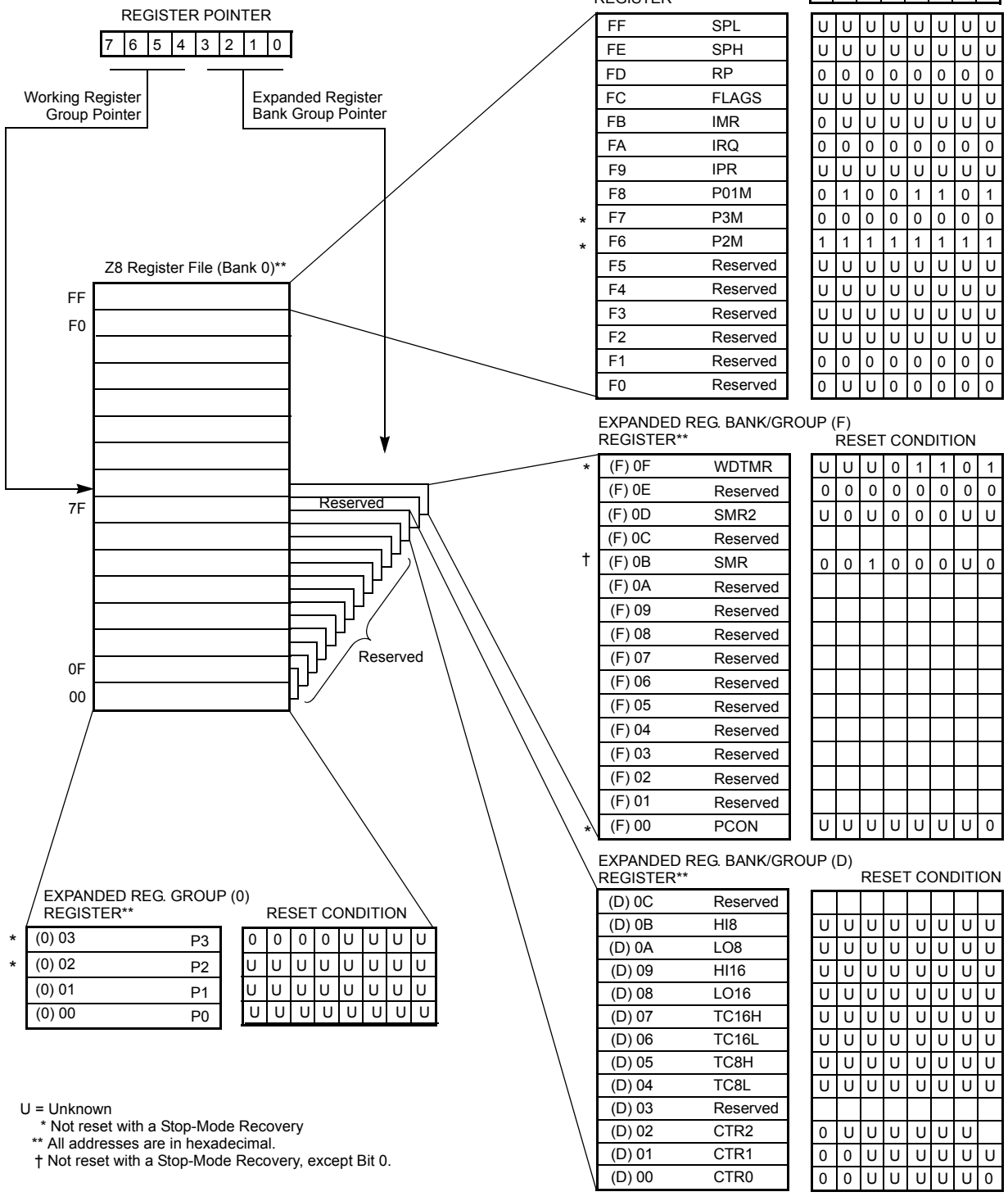
```
R253 RP = 00H
     R0 = Port0
     R1 = Port1
     R2 = Port2
     R3 = Port3
```

But if:

```
R253 RP = 0DH
     R0 = CTRL0
     R1 = CTRL1
     R2 = CTRL2
     R3 = Reserved
```

The counter/timers are mapped into ERF group D. Access is easily done using the following example:

```
LD          RP,#0Dh     ; Select ERF D for access and register
                        ; Bank 0 as the working register group.
LD          R0,#xx      ; access CTRL0
LD          1,#xx       ; access CTRL1
LD          RP,#7Dh     ; Select expanded register group (ERF)
                        ; group D for access and register
                        ; Bank 7 as the working register bank.
LD          R1,2        ; CTRL2→register 71H
```



U = Unknown
* Not reset with a Stop-Mode Recovery
** All addresses are in hexadecimal.
† Not reset with a Stop-Mode Recovery, except Bit 0.

Figure 22. Expanded Register File Architecture

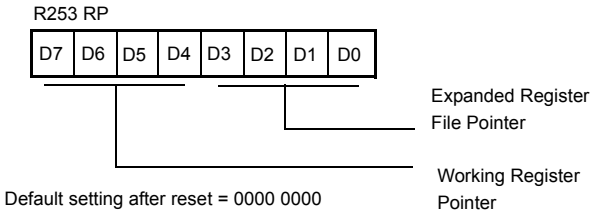


Figure 23. Register Pointer

Register File

The register file (bank 0) consists of 4 I/O port registers, 236 general-purpose registers, and 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), plus two expanded registers groups (Banks D and F). Instructions can access registers directly or indirectly through an 8-bit address field. This allows a short, 4-bit register address using the register pointer (Figure 24). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The register pointer addresses the starting location of the active working register group.

Note: Working register group E0–EF of Bank 0 are only accessed through working registers and indirect addressing modes.

Table 13. Expanded Register Group D (Continued)

(D) 09h	HI16
(D) 08h	LO16
(D) 07h	TC16H
(D) 06h	TC16L
(D) 05h	TC8H
(D) 04h	TC8L
(D) 03h	Reserved
(D) 02h	CTR2
(D) 01h	CTR1
(D) 00h	CTR0

HI8(D)0Bh Register

This register (Table 14) holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 1.

Table 14. HI8(D)0Bh Register

Field	Bit Position	Value	Description
T8_Capture_HI	76543210	R/W	Captured Data No Effect

L08(D)0Ah Register

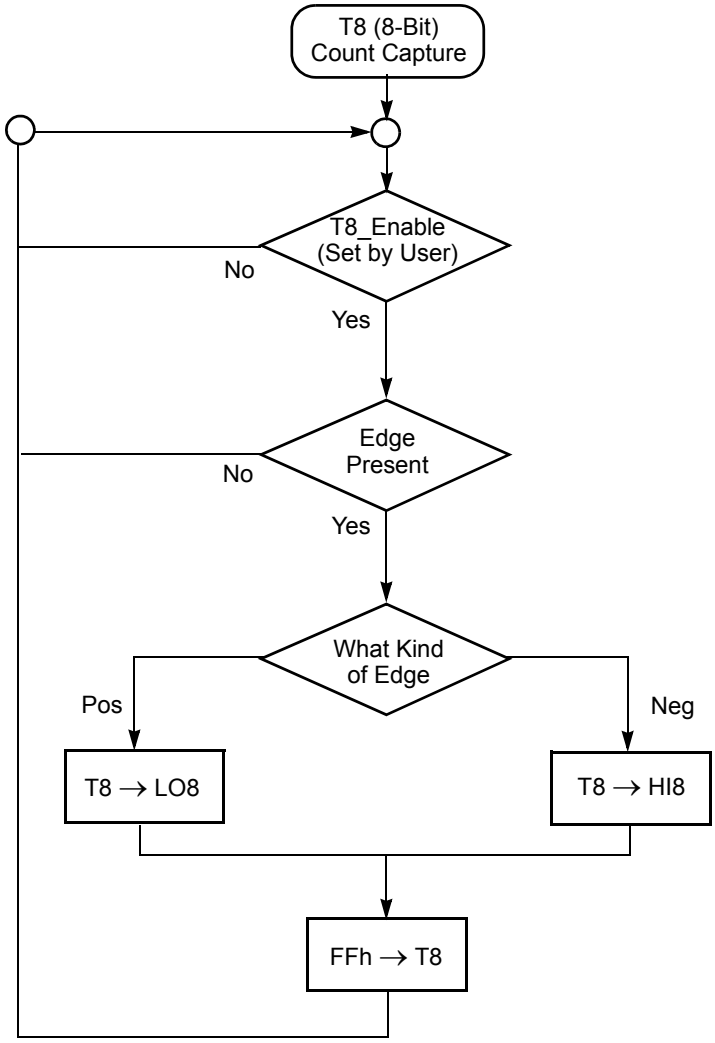
This register (Table 15) holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 0.

Table 15. LO8(D)0Ah Register

Field	Bit Position	Value	Description
T8_Capture_L0	76543210	R/W	Captured Data No Effect

T8 Demodulation Mode

You need to program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1 D5, D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1 D5, D4) is detected during counting, the current value of T8 is one's complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if negative edge, HI8. One of the edge-detect status bits (CTR1 D1, D0) is set, and an interrupt can be generated if enabled (CTR0 D2). Meanwhile, T8 is loaded with FFh and starts counting again. When T8 reaches 0, the time-out status bit (CTR0 D5) is set, an interrupt can be generated if enabled (CTR0 D1), and T8 continues counting from FFh (see Figure 30 and Figure 31).



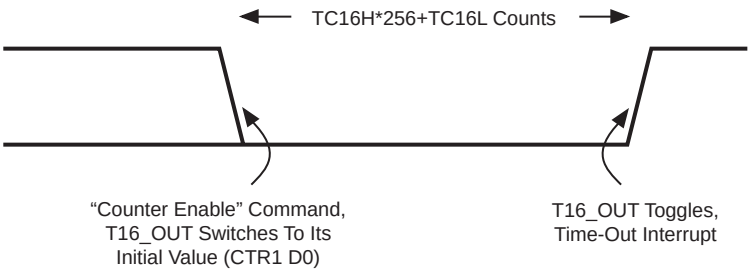


Figure 33. T16_OUT in Single-Pass Mode

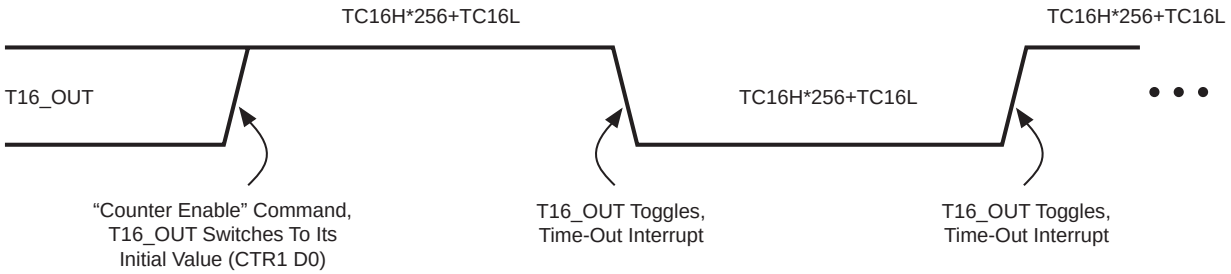


Figure 34. T16_OUT in Modulo-N Mode

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded. To ensure known operation, do not load these registers at the time the values are to be loaded into the counter/timer. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFh to FFFEh. Transition from 0 to FFFFh is not a time-out condition.

T16 Demodulation Mode

You need to program TC16L and TC16H to FFh. After T16 is enabled, when the first edge (rising, falling or both depending on CTR1, D5, D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1 D5, D4) is detected during counting, the current count in T16 is one's complemented and put into HI16 and LO16. When data is captured, one of the edge-detect status bits (CTR1 D1, D0) is set, and an interrupt is generated if enabled (CTR2 D2). T16 is loaded with FFFFh and starts again.

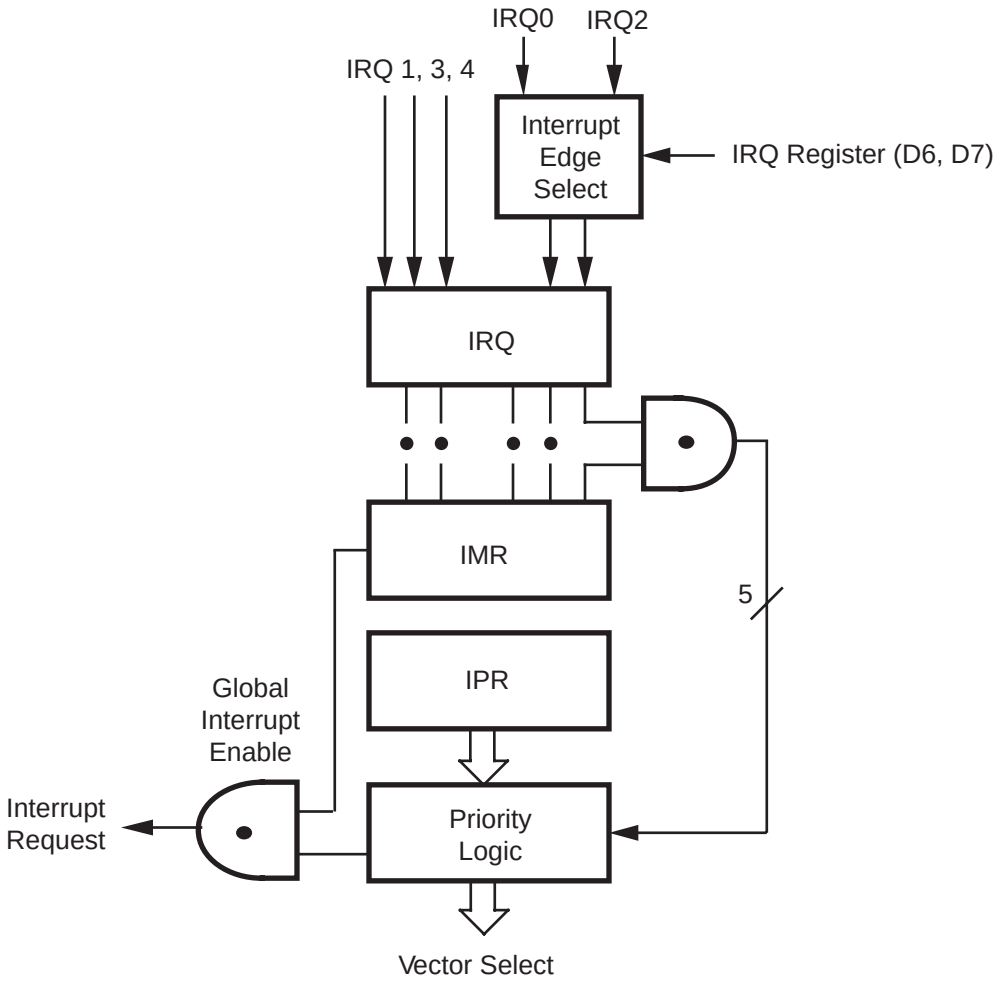


Figure 37. Interrupt Block Diagram

Table 26. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rising Falling Edge Triggered
IRQ1	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	/DAV2, IRQ2, T_{IN}	4,5	External (P31), Rising Falling Edge Triggered
IRQ3	T16	6, 7	Internal
IRQ4	T8	8, 9	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86E7X interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered and are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 27.

Table 27. IRQ Register

IRQ		Interrupt Edge	
D7	**D6**	**IRQ2 (P31)**	**IRQ0 (P32)**
0	0	F	F
0	1	F	R
1	0	F	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge
In analog mode, the Stop-Mode Recovery sources selected by the SMR register are connected to the IRQ1 input. Any of the Stop-Mode Recovery sources for SMR (except P31, P32, and P33) can be used to generate IRQ1 (falling edge triggered).

Clock

The Z86E7X on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ohms. The Z86E7X on-chip oscillator can be driven with a cost-effective RC network or other suitable external clock source.

EPROM Programming

Table 31 describes the programming and test modes.

Table 31. Programming and Test Modes

	Device Pins									
User/Test Mode Device Pin # User Modes	**P33 V_{PP}**	**P32 EPM**	**Pref1 /CE**	**P31 /OE**	**P20 /PGM**	**Addr**	**V_{CC}**	**Port 1 CNFG DATA**	**Test ADDR A0–A3**	**Note**
EPROM Read	V_{CC}	V_H	V_{IL}	V_{IL}	V_{IH}	Addr	3.0 V	Out	XX	
Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	V_{IL}	Addr	6.0 V	In	XX	
Program Verify	V_{PP}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	Addr	6.0 V	Out	XX	
RC Option	V_{PP}	V_{CC}	V_H	V_{IH}	V_{IL}	XX	6.0 V	XX	XX	
Margin Read	V_{VA}	V_H	V_{IL}	V_H	V_{IH}	Addr	6.0 V	Out	00	1
Shadow Row Rd	V_{CC}	V_H	V_{IL}	V_{IL}	V_{IH}	COL	3.0 V	Out	01	1
Shadow Row Prg	V_{PP}	V_H	V_{IL}	V_{IH}	V_{IL}	COL	6.0 V	In	01	1
Shadow Row Ver	V_{PP}	V_H	V_{IL}	V_{IL}	V_{IH}	COL	6.0 V	Out	01	1
Shadow Col Rd	V_{CC}	V_H	V_{IL}	V_{IL}	V_{IH}	ROW	3.0 V	Out	02	1
Shadow Col Prg	V_{PP}	V_H	V_{IL}	V_{IH}	V_{IL}	ROW	6.0 V	In	03	1
Shadow Col Ver	V_{PP}	V_H	V_{IL}	V_{IL}	V_{IH}	ROW	6.0 V	Out	02	1
Page Prg 2 Byte	V_{PP}	V_H	V_{IL}	V_{IH}	V_{IL}	TBD	6.0 V	In	04	1
Page Prg 4 Byte	V_{PP}	V_H	V_{IL}	V_{IH}	V_{IL}	TBD	6.0 V	In	05	1
Page Prg 8 Byte	V_{PP}	V_H	V_{IL}	V_{IH}	V_{IL}	TBD	6.0 V	In	06	1
Page Prg 16 Byte	V_{PP}	V_H	V_{IL}	V_{IH}	V_{IL}	TBD	6.0 V	In	07	1

Notes:
1. All test modes are entered by first setting up the corresponding test address and then latching the address by bringing the /OE to V_H and then to V_{IL}, except for the margin read which requires /OE to be kept at V_H.

V_{VA} = Variable from V_{CC} to V_{PP}
V_{PP} = 12.5 V ± 0.5 V
V_H = 12.5 V ± 0. 5 V
V_{IH} = 3 V
V_{IL} = 0 V
XX = Irrelevant
I_{PP} during programming = 40 mA maximum
I_{CC} during programming, verify, or read = 40 mA maximum.

Table 32 lists the timing of the programming waveform.

Table 32. Timing of Programming Waveform

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup Time	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		µs
7	Data Hold Time	2		µs
8	/OE Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	/PGM Setup Time	2		µs
14	Address to /OE Setup Time	2		µs
15	Option Program Pulse Width	78		ms

Figure 45 shows the EPROM read timing diagram. Figure 46 on page 79 shows the EPROM program and verify timing diagram. Figure 47 on page 80 shows the programming EPROM, RAM protect, and 16K size selection timing diagram.

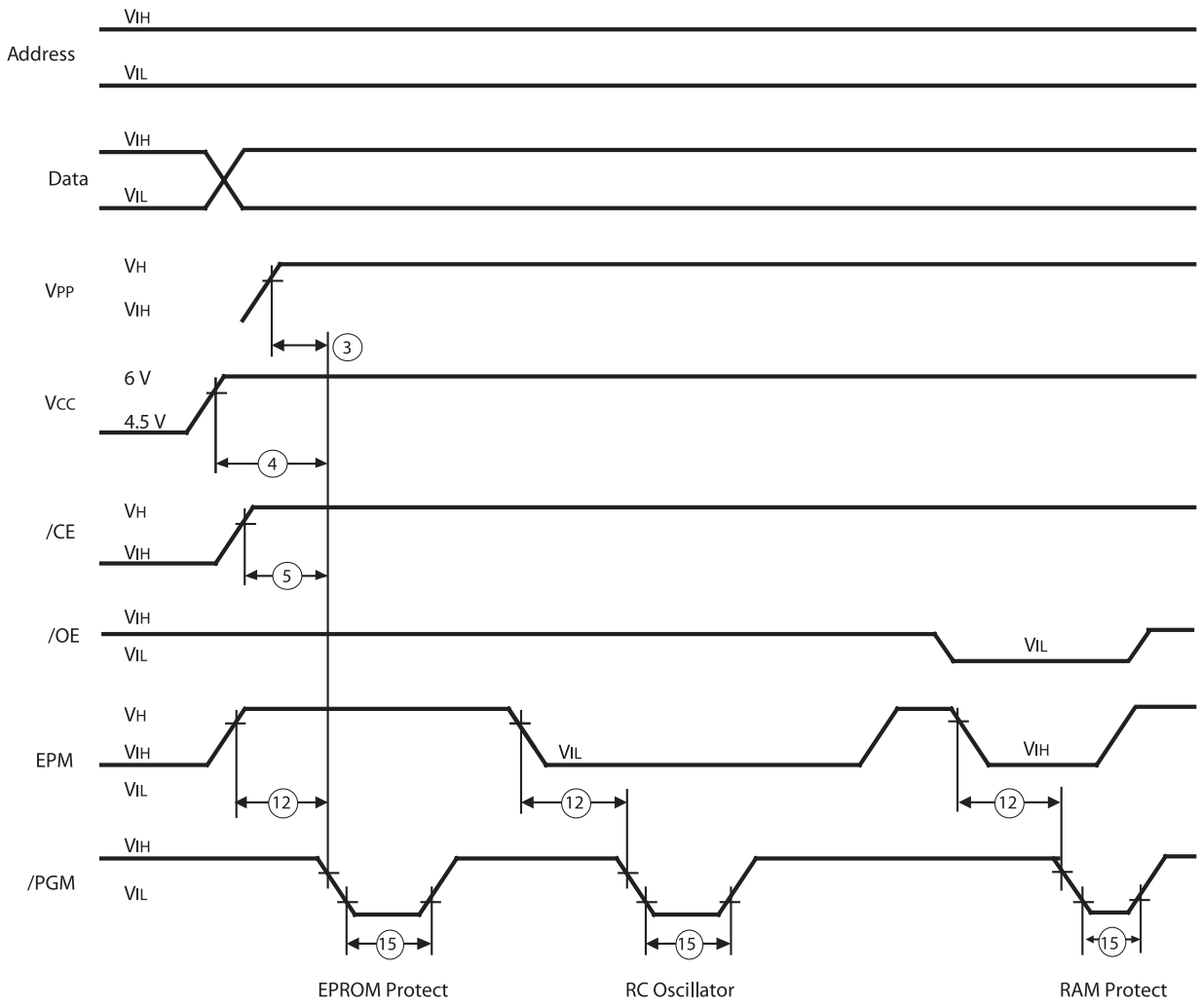


Figure 47. Programming EPROM, RAM Protect, and 16K Size Selection

Figure 48 shows the programming flowchart.

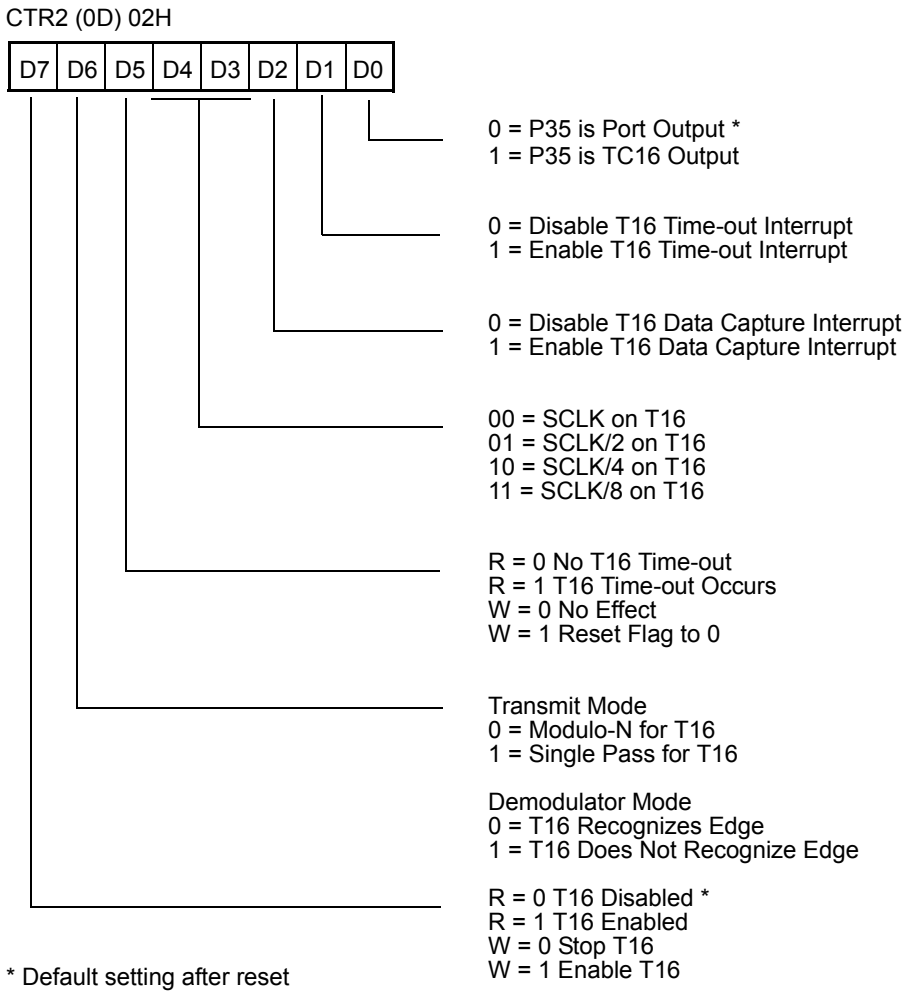


Figure 51. T16 Control Register—(0D) 2H: Read/Write Except Where Noted

Z8 Standard Control Register Diagrams

Figure 58 through Figure 66 show the Z8 standard control register diagrams.

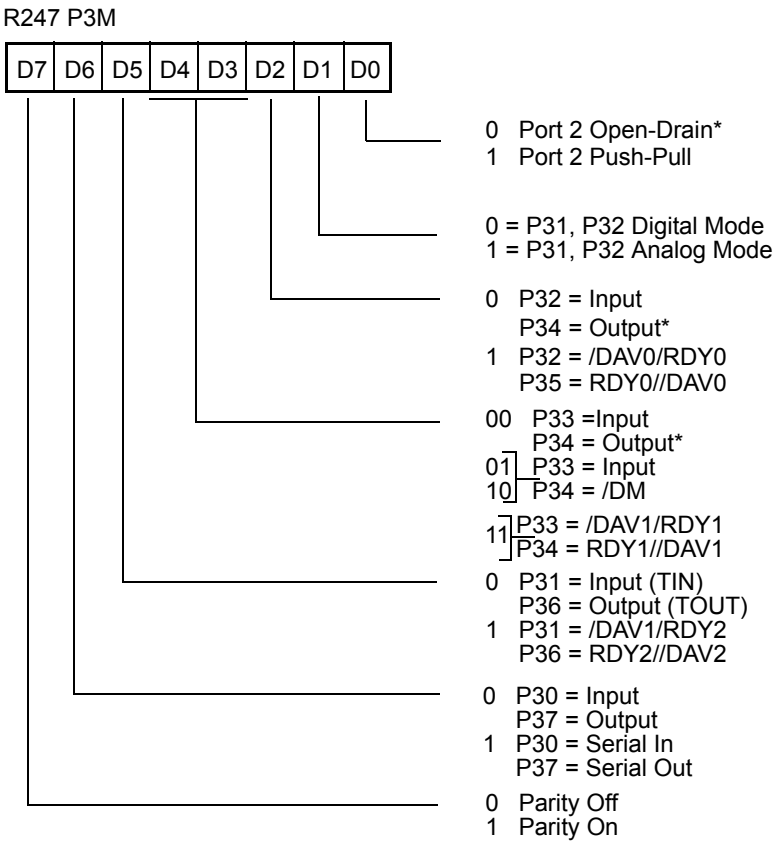


Figure 58. Port 3 Mode Register—F7H: Write Only

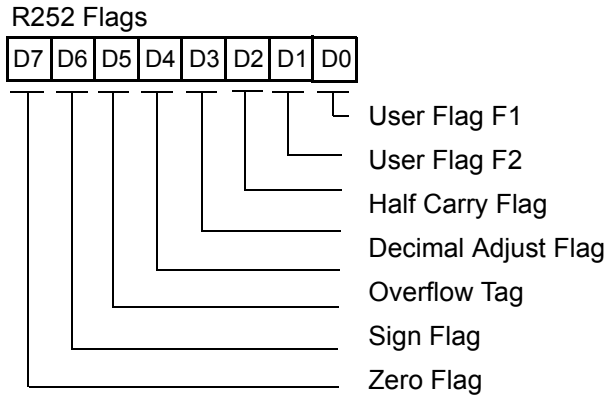


Figure 63. Flag Register—(0) FCH: Read/Write

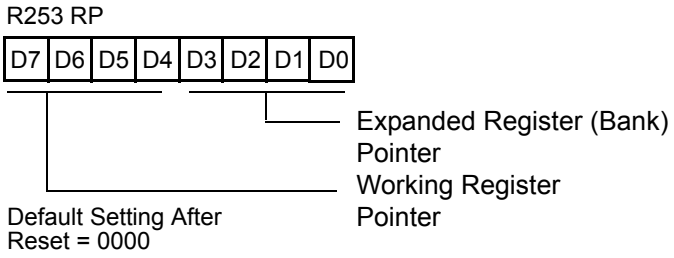


Figure 64. Register Pointer—(0) FDH: Read/Write

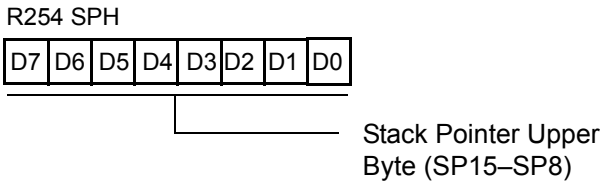


Figure 65. Stack Pointer High—(0) FEH: Read/Write

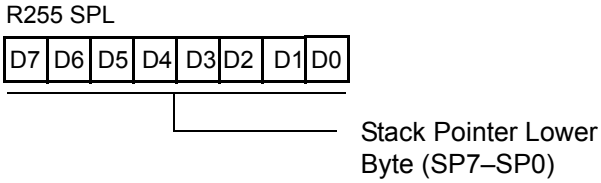
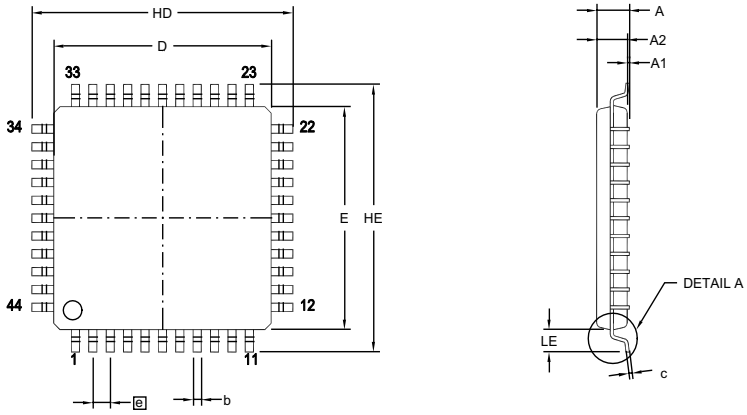


Figure 66. Stack Pointer Low—(0) FFH: Read/Write



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.40	1.60	0.055	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.30	0.45	0.012	0.018
c	0.09	0.20	0.004	0.008
HD	11.75	12.25	0.463	0.482
D	9.90	10.10	0.390	0.398
HE	11.75	12.25	0.463	0.482
E	9.90	10.10	0.390	0.398
e	0.80 BSC		0.031 BSC	
L	0.45	0.75	0.018	0.030
LE	1.00 REF		0.039 REF	

1. CONTROLLING DIMENSIONS : mm
2. MAX. COPLANARITY : .10mm / 0.004"

Figure 68. 44-Pin LQFP Package Diagram