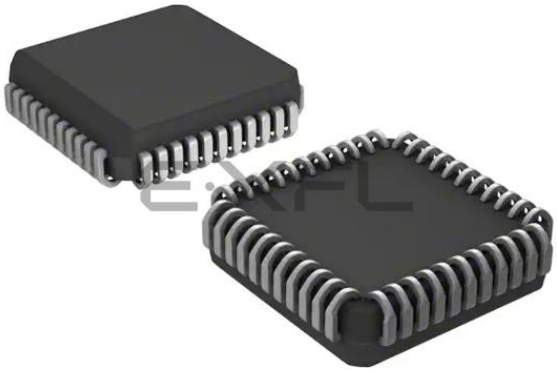

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	31
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	748 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e7216vsc00tr

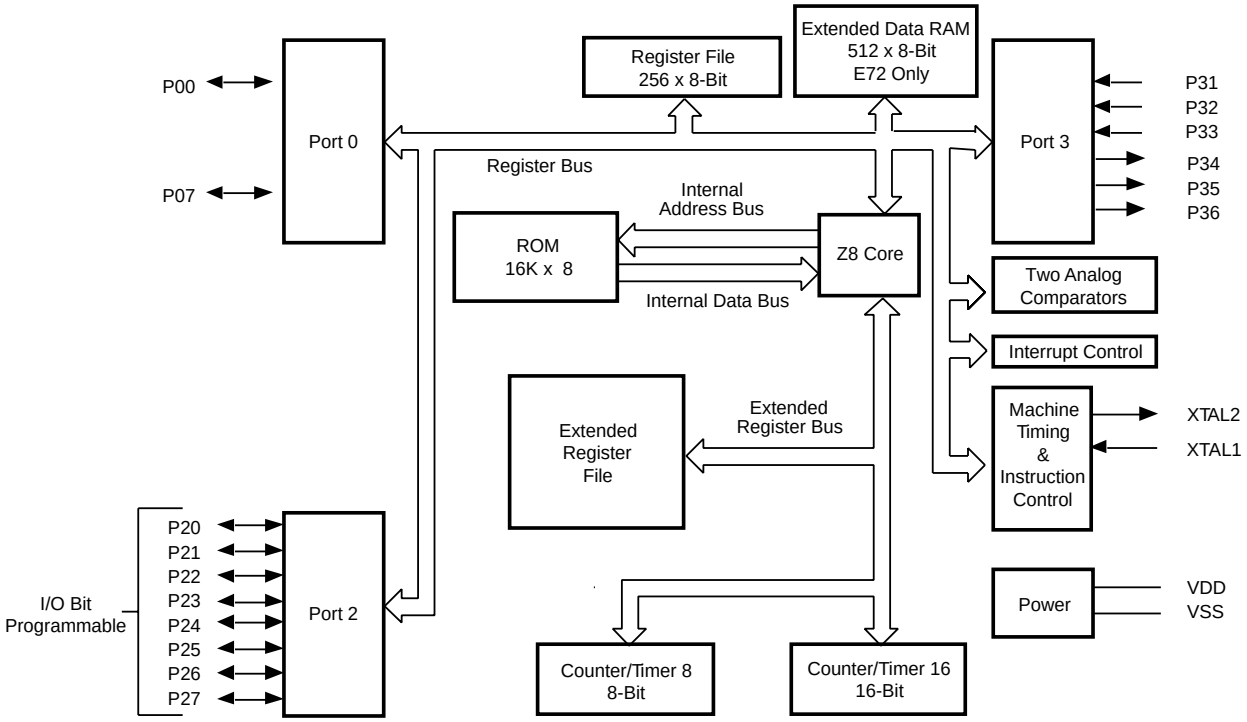


Figure 2. Z86E7X Functional Block Diagram

Pin Description

Figure 3 shows the pin assignments for the standard mode of the 40-pin dual in-line package (DIP). Figure 4 on page 6 shows the pin assignments for the electronically programmable read-only memory (EPROM) mode of the 40-pin DIP.

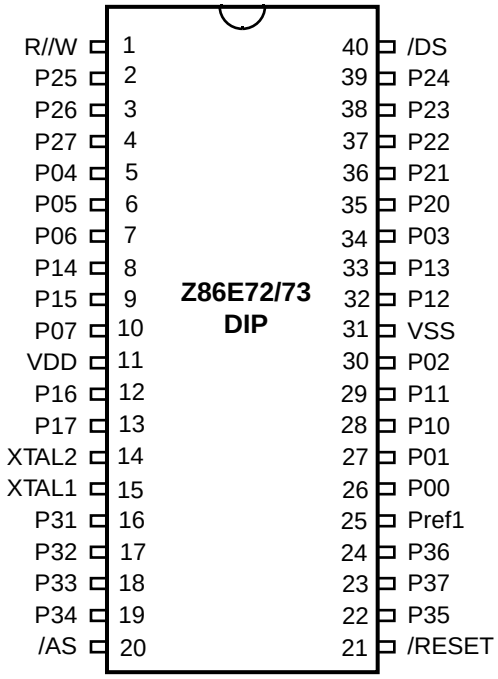


Figure 3. 40-Pin DIP Pin Assignments (Standard Mode)

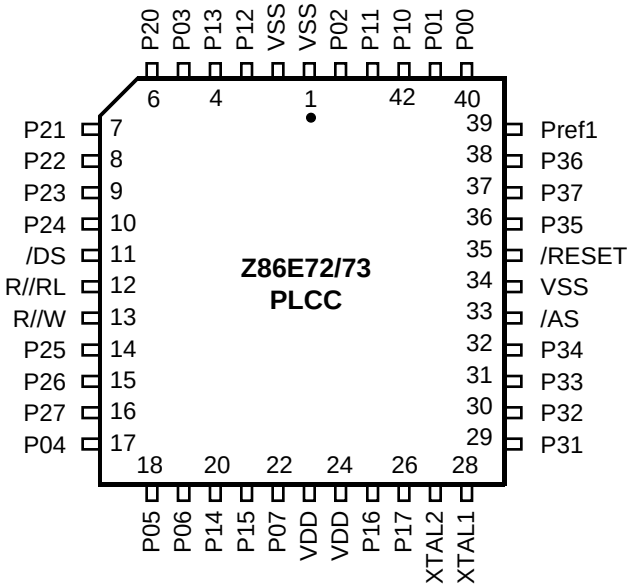


Figure 5. 44-Pin PLCC Pin Assignments (Standard Mode)

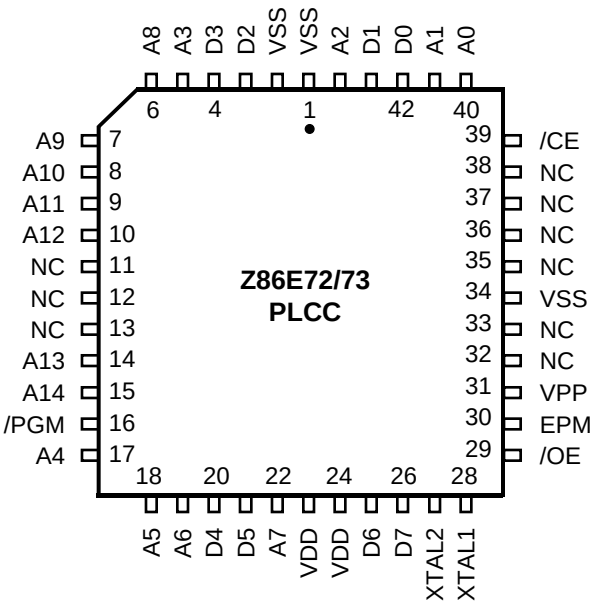


Figure 6. 44-Pin PLCC Pin Assignments (EPROM Mode)

Table 4. Z86E72/73 40-Pin DIP Identification—EPROM Mode (Continued)

40-Pin #	Symbol	Function	Direction
34	A3	Address 3	Input
35–39	A8–A12	Address 8, 9, 10, 11, 12	Input
40	N/C	Not Connected	

Table 5. Z86E72/73 44-Pin LQFP/PLCC Pin Identification—EPROM Mode

44-Pin LQFP	44-Pin PLCC	Symbol	Function	Direction
1–2	18–19	A5–A6	Address 5, 6	Input
3–4	20–21	D4–D5	Data 4, 5	Input/Output
5	22	A7	Address 7	Input
6–7	23–24	V_{DD}	Power Supply	
8–9	25–26	D6–D7	Data 6, 7	Input/Output
10	27	XTAL2	Crystal Oscillator Clock	
11	28	XTAL1	Crystal Oscillator Clock	
12	29	/OE	Output Enable	Input
13	30	EPM	EPROM Prog. Mode	Input
14	31	V_{PP}	Prog. Voltage	Input
15–16	32–33	N/C	Not Connected	
17	34	V_{SS}	Ground	
18–21	35–38	N/C	Not Connected	
22	39	/CE	Chip Select	Input
23–24	40–41	A0–A1	Address 0, 1	Input
25–26	42–43	D0–D1	Data 0, 1	Input/Output
27	44	A2	Address 2	Input
28–29	1–2	V_{SS}	Ground	
30–31	3–4	D2–D3	Data 2, 3	Input/Output
32	5	A3	Address 3	Input
33–37	6–10	A8–A12	Address 8, 9, 10, 11, 12	Input
38–40	11–13	N/C	Not Connected	

Table 8. DC Characteristics (Continued)

Sym.	Parameter	V_{CC}	T_A = 0 °C to +70 °C Min	Max	Typical @ 25°C	Units	Conditions
V_{RAM}	Static RAM Data Retention Voltage	Vram			0.5	V	Worst case 0.8 V guaranteed by design only Note 6

Notes:	ICC1	Typ	Max	Unit	Frequency
	Crystal/Resonator	3.0 mA	5	mA	8.0 MHz
	External Clock Drive	0.3 mA	5	mA	8.0 MHz

1. All outputs unloaded, inputs at rail
2. CL1 = CL2 = 100 pF
3. Same as note [4] except inputs at V_{CC}
4. The V_{LV} increases as the temperature decreases.
5. Oscillator stopped
6. Oscillator does not stop when V_{CC} falls below V_{LV} threshold.
7. 32 kHz clock driver input
8. For analog comparator, inputs when analog comparators are enabled
9. WDT, Comparators, Low Voltage Detection, and ADC (if applicable) are disabled. The IC might draw more current if any of the above peripherals is enabled.

* All outputs excluding P00, P01, P36, and P37

/RESET (Input, Active Low)

Reset initializes the MCU. Reset is accomplished either through Power-On, Watch-Dog Timer, Stop-Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the reset line need to be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally. There is no condition internal to the Z86E7X that does not allow an external reset to occur.

After the POR time, /RESET is a Schmitt-triggered input. To avoid asynchronous and noisy reset problems, the Z86E7X is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks or for the duration of the external reset, whichever is longer.

During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. Program execution begins at location 000CH, 5–10 TpC cycles after the RST is released. For Power-On Reset, the typical reset output time is 5 ms.

Note: The Z86E7X devices do not have internal pull resistors on Port 3 inputs.

The upper nibble of the register pointer (Figure 23 on page 42) selects which working register group of 16 bytes in the register file, out of the possible 256, is accessed. The lower nibble selects the expanded register file bank and, in the case of the Z86E7X family, banks 0, F, and D are implemented. A 0h in the lower nibble allows the normal register file (bank 0) to be addressed, but any other value from 1h to Fh exchanges the lower 16 registers to an expanded register bank.

For example, Z86E73 (see Figure 22):

```
R253 RP = 00H
     R0 = Port0
     R1 = Port1
     R2 = Port2
     R3 = Port3
```

But if:

```
R253 RP = 0DH
     R0 = CTRL0
     R1 = CTRL1
     R2 = CTRL2
     R3 = Reserved
```

The counter/timers are mapped into ERF group D. Access is easily done using the following example:

```
LD          RP,#0Dh     ; Select ERF D for access and register
                        ; Bank 0 as the working register group.
LD          R0,#xx      ; access CTRL0
LD          1,#xx       ; access CTRL1
LD          RP,#7Dh     ; Select expanded register group (ERF)
                        ; group D for access and register
                        ; Bank 7 as the working register bank.
LD          R1,2        ; CTRL2→register 71H
```

Table 13. Expanded Register Group D (Continued)

(D) 09h	HI16
(D) 08h	LO16
(D) 07h	TC16H
(D) 06h	TC16L
(D) 05h	TC8H
(D) 04h	TC8L
(D) 03h	Reserved
(D) 02h	CTR2
(D) 01h	CTR1
(D) 00h	CTR0

HI8(D)0Bh Register

This register (Table 14) holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 1.

Table 14. HI8(D)0Bh Register

Field	Bit Position	Value	Description
T8_Capture_HI	76543210	R/W	Captured Data No Effect

L08(D)0Ah Register

This register (Table 15) holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 0.

Table 15. LO8(D)0Ah Register

Field	Bit Position	Value	Description
T8_Capture_L0	76543210	R/W	Captured Data No Effect

HI16(D)09h Register

This register (Table 16) holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Table 16. HI16(D)09h Register

Field	Bit Position	Value	Description
T16_Capture_HI	76543210	R/W	Captured Data No Effect

L016(D)08h Register

This register (Table 17) holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Table 17. LO16(D)08h Register

Field	Bit Position	Value	Description
T16_Capture_LO	76543210	R/W	Captured Data No Effect

TC16H(D)07h Register

Table 18 describes the Counter/Timer2 MS-Byte Hold Register.

Table 18. TC16H(D)07h Register

Field	Bit Position	Value	Description
T16_Data_HI	76543210	R/W	Data

TC16L(D)06h Register

Table 19 describes the Counter/Timer2 LS-Byte Hold Register.

Table 19. TC16L(D)06h Register

Field	Bit Position	Value	Description
T16_Data_LO	76543210	R/W	Data

Table 23. CTR1(D)01h Register (Continued)

Field	Bit Position		Value	Description
Initial_T8_Out/Rising_Edge	------1-			Transmit Mode
		R/W	0	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/Falling _Edge	-------0			Transmit Mode
		R/W	0	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

Note: * Indicates the value upon Power-On Reset.

Mode

If it is 0, the counter/timers are in the transmit mode; otherwise, they are in the demodulation mode.

P36_Out/Demodulator_Input

In transmit mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In demodulation mode, this bit defines whether the input signal to the counter/timers is from P20 or P31.

T8/T16_Logic/Edge _Detect

In transmit mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In demodulation mode, this field defines which edge needs to be detected by the edge detector.

Transmit_Submode/Glitch Filter

In transmit mode, this field defines whether T8 and T16 are in the “Ping-Pong” mode or in independent normal operation mode. Setting this field to “Normal

CTR2(D)02h Register

Table 24 describes the Counter/Timer16 Control Register.

Table 24. CTR2(D)02h Register

Field	Bit Position		Value	Description
T16_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Submode/Modulo-N	-6------	R/W		Transmit Mode
			0	Modulo-N
			1	Single Pass
				Demodulation Mode
			0	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
Time_Out	--5-----	R	0	No Counter Time-Out
			1	Counter Time-Out Occurred
		W	0	No Effect
			1	Reset Flag to 0
T16 _Clock	---43---	R/W	00	SCLK
			01	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	-----2--	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	------1-	R/W	0	Disable Time-Out Int.
			1	Enable Time-Out Int.
P35_Out	-------0	R/W	0*	P35 as Port Output
			1	T16 Output on P35

Note: * Indicates the value upon Power-On Reset.

T16_Enable

This field enables T16 when set to 1.

Single/Modulo-N

In transmit mode, when set to 0, the counter reloads the initial value when terminal count is reached. When set to 1, the counter stops when the terminal count is reached.

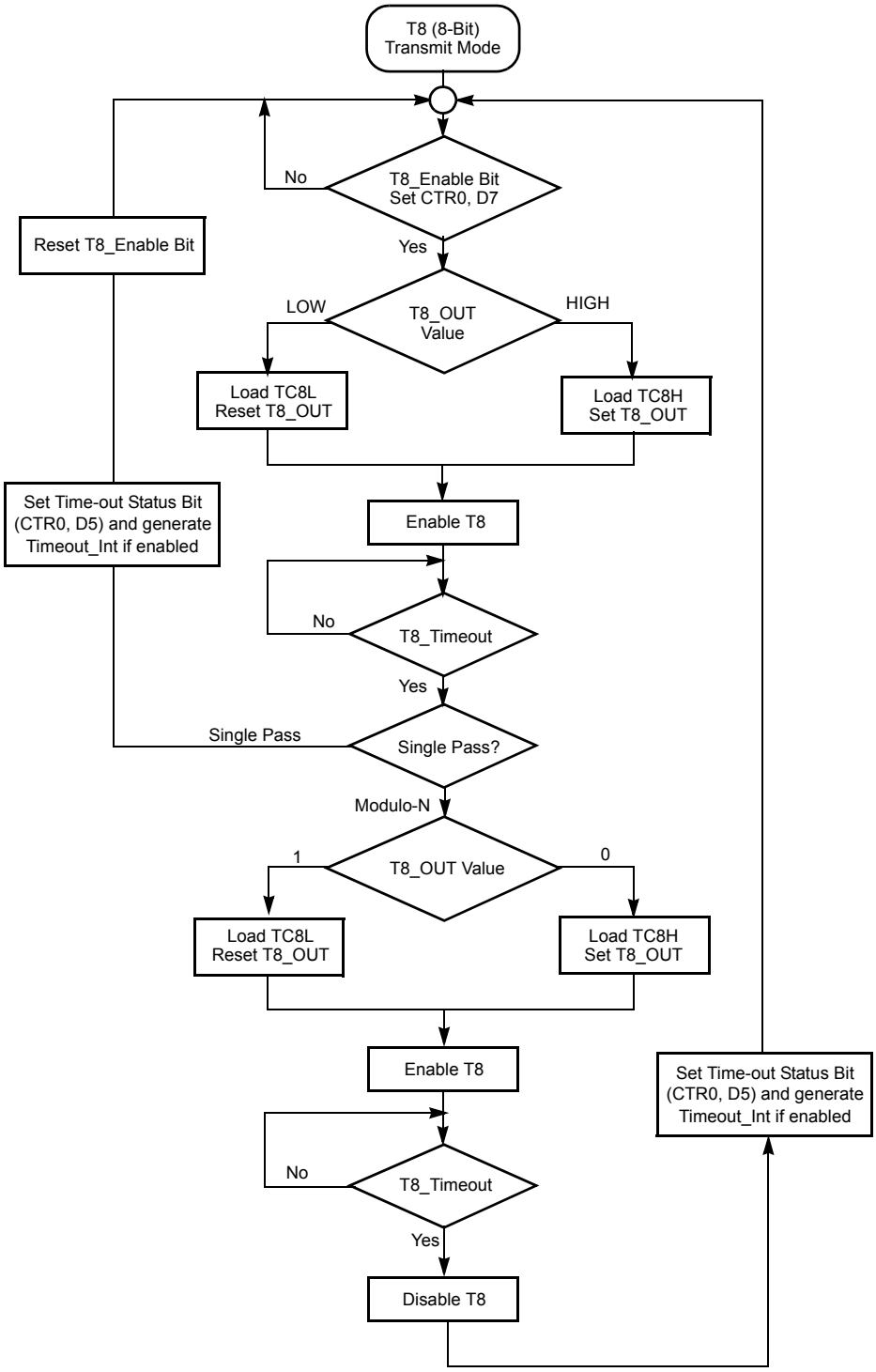


Figure 27. Transmit Mode Flowchart

If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A time out of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If D6 bit of CTR2 is toggled (by writing a 0 and then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both, depending on CTR1 D5, D4) but continues to ignore subsequent edges.

When T16 reaches 0, it continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt time-out can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in transmit mode. T8 and T16 need to be programmed in Single-Pass Mode (CTR0 D6, CTR2 D6), and Ping-Pong Mode needs to be programmed in CTR1 D3, D2. You can begin the operation by enabling either T8 or T16 (CTR0 D7 or CTR2 D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1 D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled and T16 is enabled. T16_OUT switches to its initial value (CTR1 D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, and the whole cycle repeats. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0 D1, CTR2 D1). To stop the Ping-Pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 35.

Note: Enabling Ping-Pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and then reset the status flags before instituting this operation.

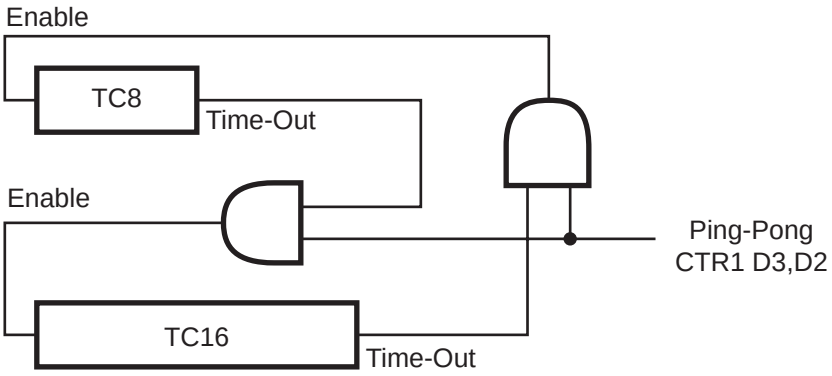


Figure 35. Ping-Pong Mode

Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the port to its standard I/O configuration.

Port 0 Output Mode (D2)

Bit 2 controls the output mode of Port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

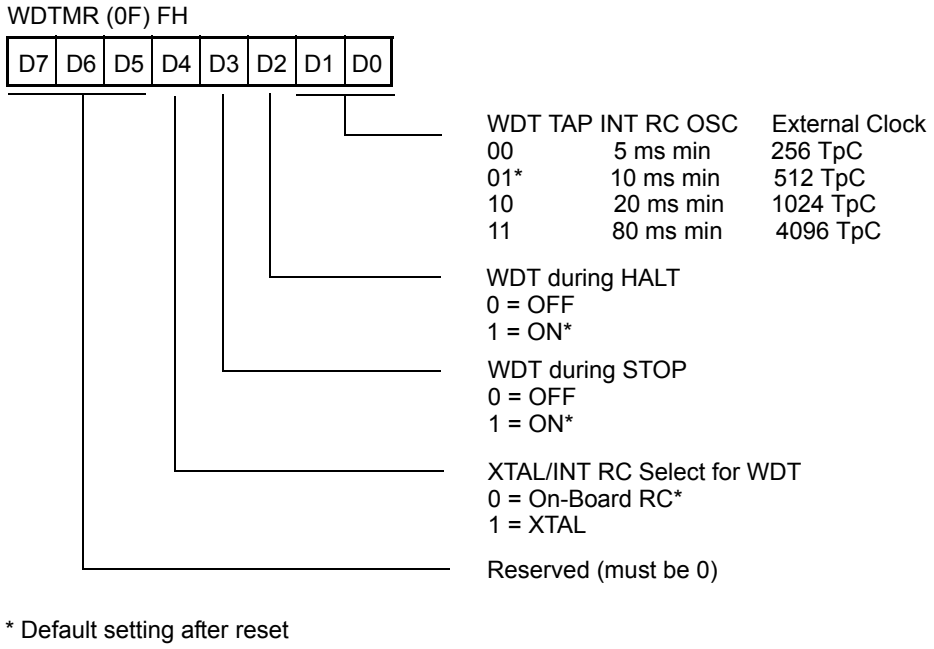
Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 40). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop-Mode Recovery signal. Bit D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

Watch-Dog Timer Mode Register (WDTMR)

The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source is selected with bit 4 of the WDT register. Bit 0 and 1 control a tap circuit that determines the time-out period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during STOP. Bits 5 through 7 are reserved. See Figure 43.



* Default setting after reset

Figure 43. Watch-Dog Timer Mode Register—Write Only

This register is accessible only during the first 60 processor cycles (SCLK) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 40 on page 68). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register Group at address location 0FH. It is organized as shown in Figure 43.

WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as shown in Table 29.

Table 29. WDT Time Select

D1	D0	Time-Out of Internal RC OSC	Time-Out of XTAL Clock
0	0	5 ms min	256 TpC
0	1	10 ms min	512 TpC
1	0	20 ms min	1024 TpC
1	1	80 ms min	4096 TpC

Notes:
TpC = XTAL clock cycle
The default on reset is 10 ms.

WDTMR During HALT (D2)

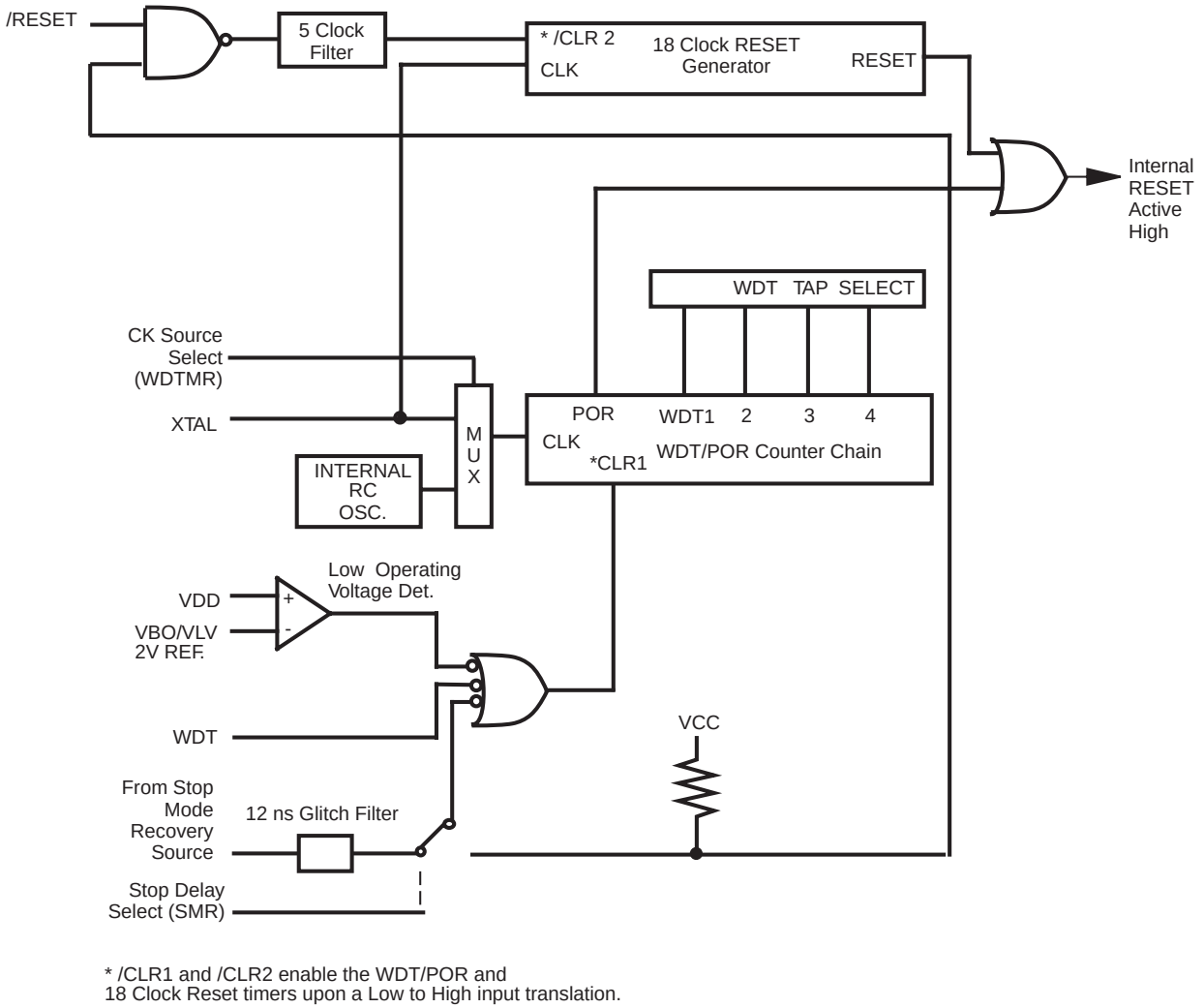
This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1.

WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Since the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during STOP. The default is 1.

Clock Source for WDT (D4)

This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed, and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator. See Figure 44.



* /CLR1 and /CLR2 enable the WDT/POR and
18 Clock Reset timers upon a Low to High input translation.

Figure 44. Resets and WDT

Low-Voltage Protection

An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below V_{LV} (Low Voltage). The minimum operating voltage varies with the temperature and operating frequency, while V_{LV} varies with temperature only.

Note: The LVD flag will be valid after enabling the detection for 20 μS (design estimation, not tested in production). LVD does not work at STOP mode. It must be disabled during STOP mode in order to reduce current.

Software-Selectable Options

There are four Software-Selectable Options to choose from based on the ROM-based parts mask options. Register (F0) EH OTP byte is where these options are controlled. These options are listed in Table 30.

Table 30. Software-Selectable Options

Bit Name	Reg(0F)EH
Port 0 Pull-ups (lower nibble)	On/Off
Port 0 Pull-ups (upper nibble)	On/Off
Port 2 Pull-ups	On/Off
Mouse/Normal	M/N

Note: The RC oscillator Xtal1/2 option is invoked during OTP programming as a user-selectable item.

Low-Voltage Detection

The device functions normally above 3.0 V under all conditions. The minimum functionality point below 3 V is to be defined. The V_{LV} is a function of temperature and process parameters. The device is forced into reset when V_{CC} drops below the V_{LV} voltage level.

Table 32 lists the timing of the programming waveform.

Table 32. Timing of Programming Waveform

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup Time	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		µs
7	Data Hold Time	2		µs
8	/OE Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	/PGM Setup Time	2		µs
14	Address to /OE Setup Time	2		µs
15	Option Program Pulse Width	78		ms

Figure 45 shows the EPROM read timing diagram. Figure 46 on page 79 shows the EPROM program and verify timing diagram. Figure 47 on page 80 shows the programming EPROM, RAM protect, and 16K size selection timing diagram.