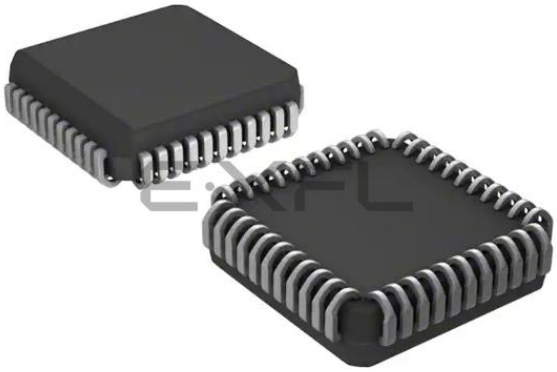

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	31
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	748 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e7216vsg

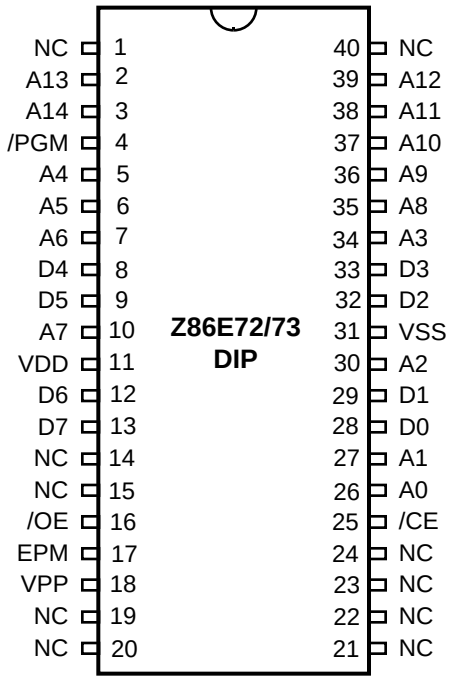


Figure 4. 40-Pin DIP Pin Assignments (EPROM Mode)

Figure 5 on page 7 shows the pin assignments for the standard mode of the 44-pin plastic leaded chip carrier (PLCC). Figure 6 on page 7 displays the pin assignments for the EPROM mode of the 44-pin PLCC.

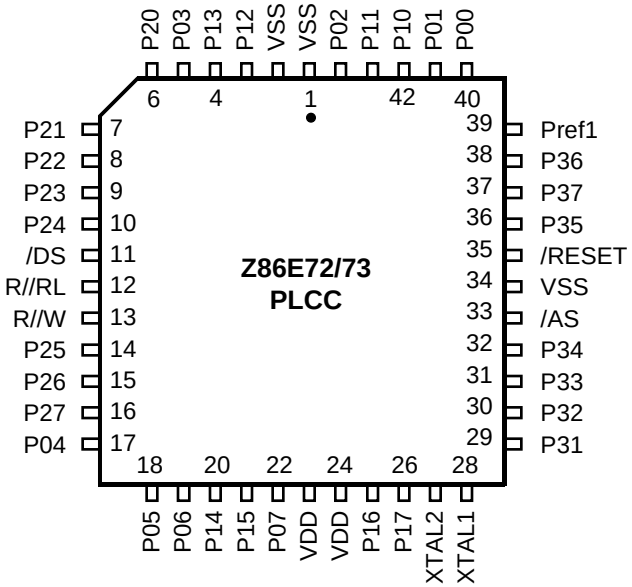


Figure 5. 44-Pin PLCC Pin Assignments (Standard Mode)

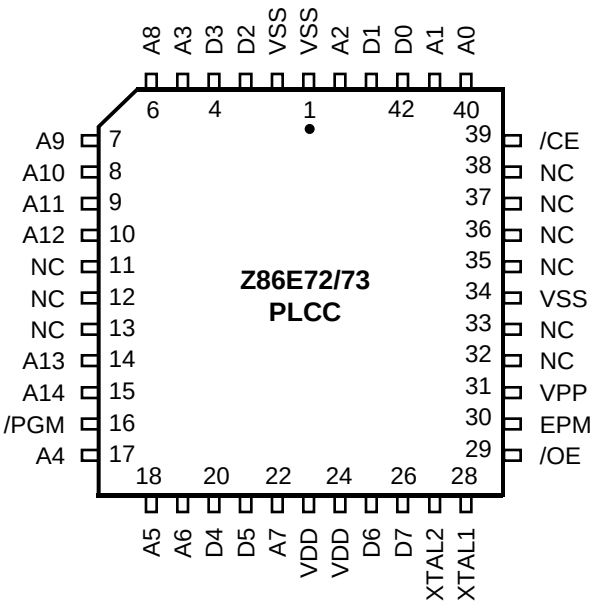


Figure 6. 44-Pin PLCC Pin Assignments (EPROM Mode)

Figure 7 displays the pin assignments for the standard mode of the 44-pin low-profile quad flat pack (LQFP). Figure 8 on page 9 shows the pin assignments for the EPROM mode of the 44-pin LQFP.

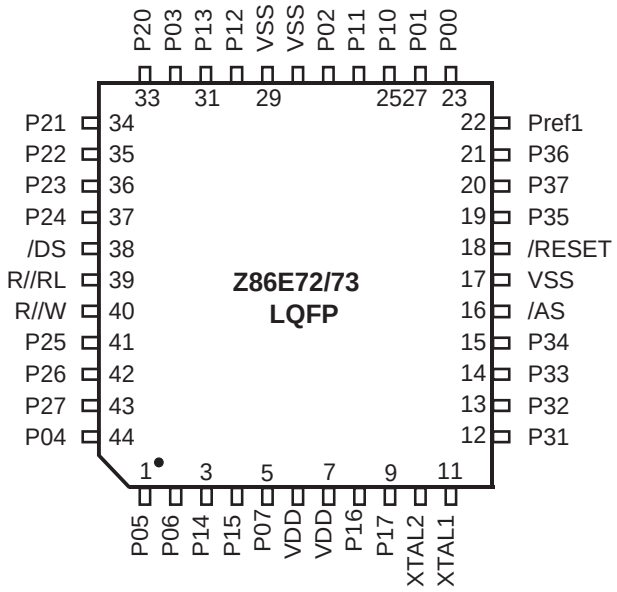


Figure 7. 44-Pin LQFP Pin Assignments (Standard Mode)

Table 8. DC Characteristics (Continued)

			T_A = 0 °C to +70 °C		Typical		
Sym.	**Parameter**	**V_{CC}**	**Min**	**Max**	**@ 25°C**	**Units**	**Conditions**
I_{IR}	Reset Input Current	3.0 V 5.5 V		–230 –400	–50 –80	µA µA	
I_{CC}	Supply Current (WDT off)	3.0 V 5.5 V		10 15	4 10	mA mA	@ 8.0 MHz @ 8.0 MHz
I_{CC1}	Standby Current (WDT Off)	3.0 V		3	1	mA	HALT Mode V_{IN} = 0 V, V_{CC} at 8.0 MHz, Notes 1, 2
		5.5 V		5	4	mA	HALT Mode V_{IN} = 0 V, V_{CC} @ 8.0 MHz, Notes 1, 2
		3.0 V		2	0.8	mA	Clock Divide-by-16 @ 8.0 MHz Notes 1, 2
		5.5 V		4	2.5	mA	Clock Divide-by-16 @ 8.0 MHz Notes 1, 2
I_{CC2}	Standby Current	3.0 V		8	2	µA	STOP Mode V_{IN} = 0 V, V_{CC} WDT is not Running Notes 3, 5, 9
		5.5 V		10	3	µA	STOP Mode V_{IN} = 0 V, V_{CC} WDT is not Running Notes 3, 5, 9
		3.0 V		500	310	µA	STOP Mode Notes 3, 5
		5.5 V		800	600	µA	V_{IN} = 0 V, V_{CC} WDT is Running
V_{ICR}	Input Common Mode Voltage Range	3.0 V 5.5 V	0 0	V_{CC}–1.0 V V_{CC}–1.0 V	V V		Note 8
V_{LV}	VCC Low-Voltage Detection			2.9 V	2.55 V		Note 6
T_{POR}	Power-On Reset	3.0 V 5.5 V	12 5	75 20	18 7	ms ms	

Table 9. External I/O or Memory Read and Write Timing

				T_A = 0 °C to +70 °C 16 MHz			
No.	**Symbol**	**Parameter**	**V_{CC}**	**Min.**	**Max.**	**Units**	**Notes**
1	TdA(AS)	Address Valid to /AS Rising Delay	3.0 V 5.5 V	55 55		ns ns	2
2	TdAS(A)	/AS Rising to Address Float Delay	3.0 V 5.5 V	70 70		ns ns	2
3	TdAS(DR)	/AS Rising to Read Data Required Valid	3.0 V 5.5 V		400 400	ns ns	1, 2 1, 2
4	TwAS	/AS Low Width	3.0 V 5.5 V	80 80		ns ns	2 2
5	Td	Address Float to /DS Falling	3.0 V 5.5 V	0 0		ns ns	
6	TwDSR	/DS (Read) Low Width	3.0 V 5.5 V	300 300		ns ns	1, 2
7	TwDSW	/DS (Write) Low Width	3.0 V 5.5 V	165 165		ns ns	1, 2
8	TdDSR(DR)	/DS Falling to Read Data Required Valid	3.0 V 5.5 V		260 260	ns ns	1, 2
9	ThDR(DS)	Read Data to /DS Rising Hold Time	3.0 V 5.5 V	0 0		ns ns	
10	TdDS(A)	/DS Rising to Address Active Delay	3.0 V 5.5 V	85 95		ns ns	2
11	TdDS(AS)	/DS Rising to /AS Falling Delay	3.0 V 5.5 V	60 70		ns ns	2
12	TdR/W(AS)	R//W Valid to /AS Rising Delay	3.0 V 5.5 V	70 70		ns ns	2
13	TdDS(R/W)	/DS Rising to R//W Not Valid	3.0 V 5.5 V	70 70		ns ns	2
14	TdDW(DSW)	Write Data Valid to /DS Falling (Write) Delay	3.0 V 5.5 V	80 80		ns ns	2
15	TdDS(DW)	/DS Rising to Write Data Not Valid Delay	3.0 V 5.5 V	70 80		ns ns	2
16	TdA(DR)	Address Valid to Read Data Required Valid	3.0 V 5.5 V		475 475	ns ns	1, 2

Pin Functions

/DS (Output, Active Low)

Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available before the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS (Output, Active Low)

Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant, crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

R//W Read/Write (Output, Write Low)

The R//W signal is Low when the CCP is writing to the external program or data memory.

R//RL (Input)

This pin, when connected to GND, disables the internal ROM and forces the device to function as a ROMless Z8.

Note: When left unconnected or pulled high to V_{CC}, the part functions normally as a Z8 ROM version.

Port 0 (P07–P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port or as an address port for interfacing external memory. The output drivers are push-pull. Port 0 is placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0. Handshake signal direction is

dictated by the I/O direction to Port 0 of the upper nibble P07–P04. The lower nibble must have the same direction as the upper nibble.

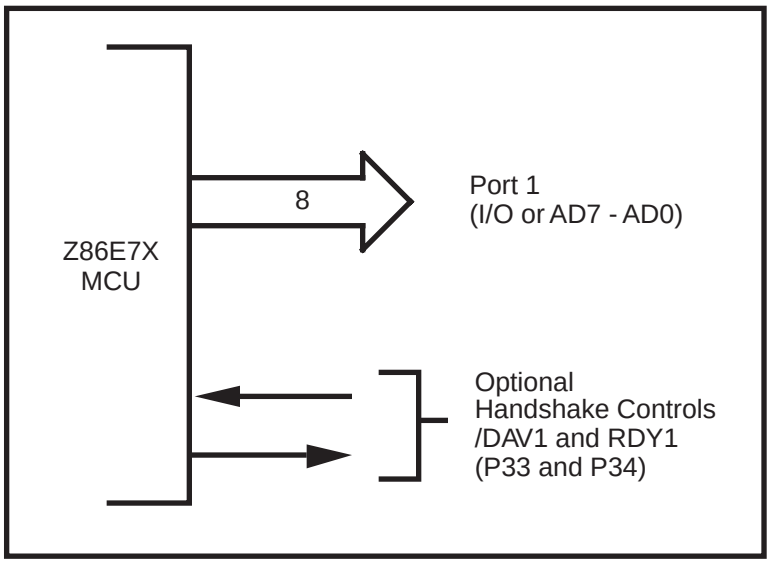
For external memory references, Port 0 can provide address bits A11–A8 (lower nibble) or A15–A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

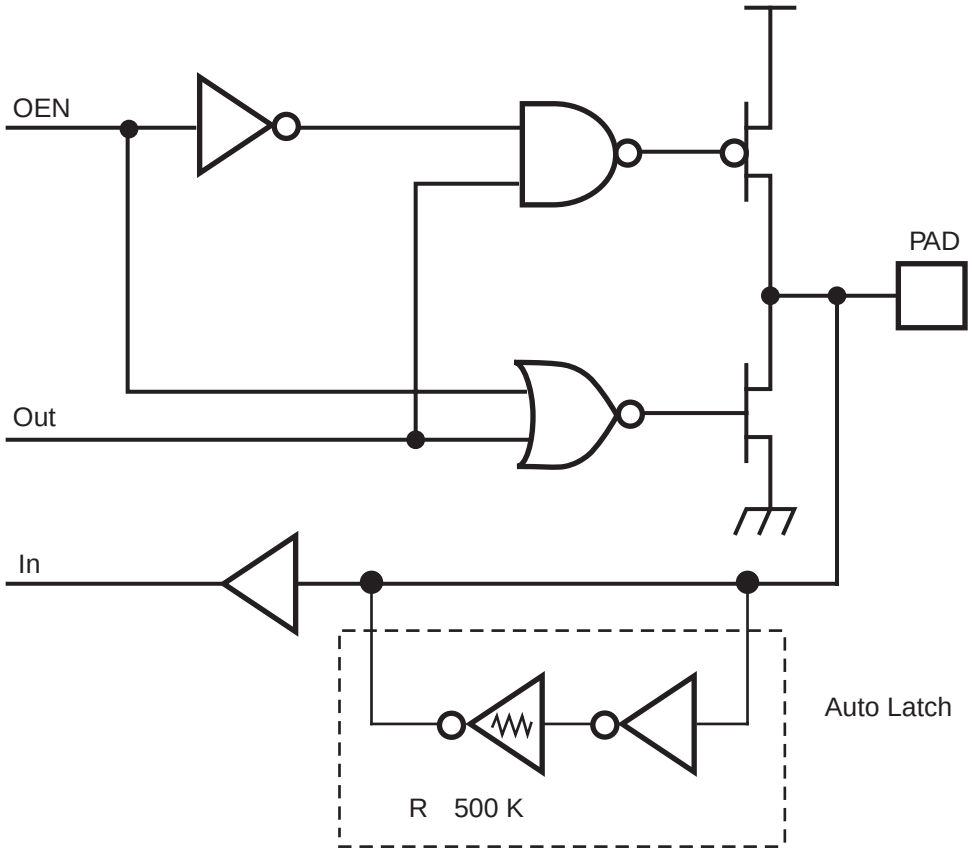
Port 0 is set in the High-Impedance Mode if selected as an address output state along with Port 1 and the control signals /AS, /DS, and R//W.

A software option is available to program 0.4 V_{DD} CMOS trip inputs on P00–P03. This allows direct interface to mouse/trackball IR sensors.

An optional 200±50% KΩ resistive transistor pull-up is available as a software option of all Port 0 bits with nibble select.

These pull-ups are disabled when configured (bit by bit) as an output. See Figure 14.


Z86E7X
MCU
8
Port 1
(I/O or AD7 - AD0)
Optional
Handshake Controls
/DAV1 and RDY1
(P33 and P34)


OEN
PAD
Out
In
Auto Latch
R 500 K

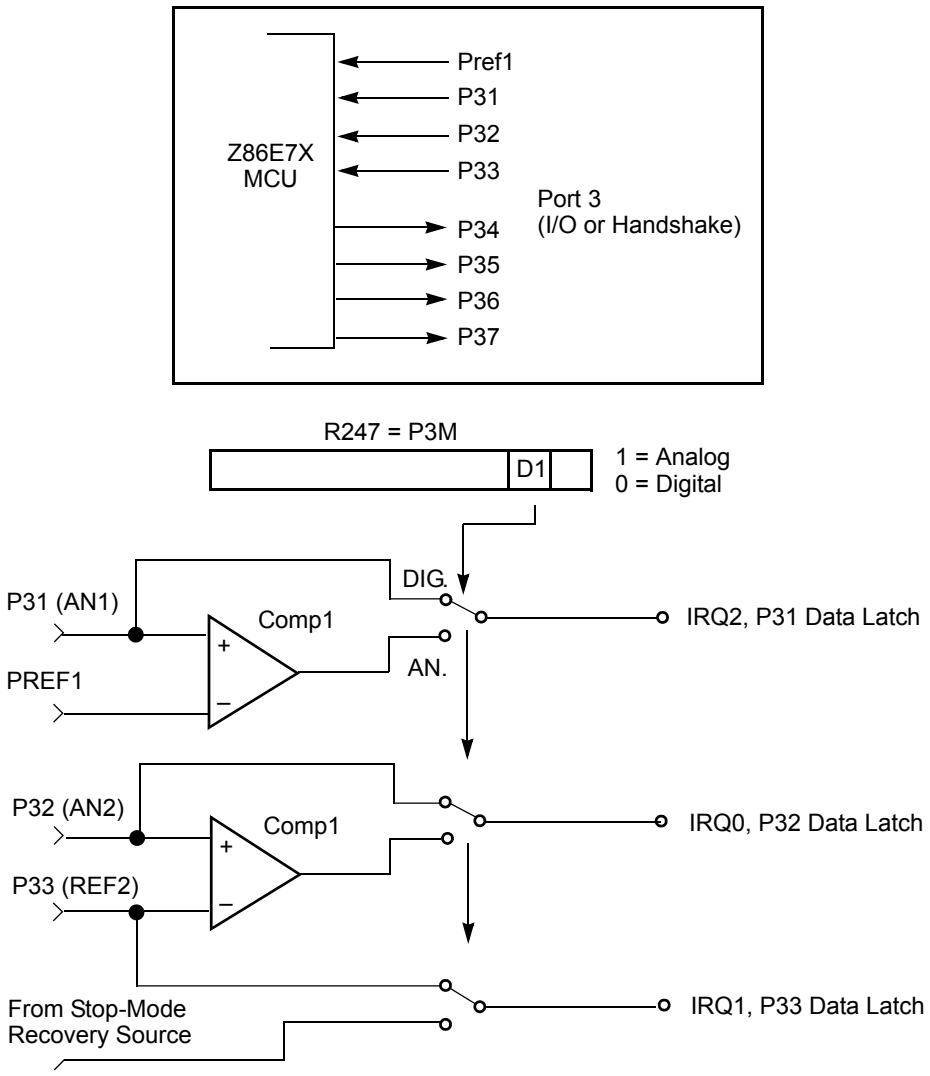


Figure 18. Port 3 Configuration

Comparator Outputs

These outputs can be programmed to be output on P34 and P37 through the PCON register (Figure 19).

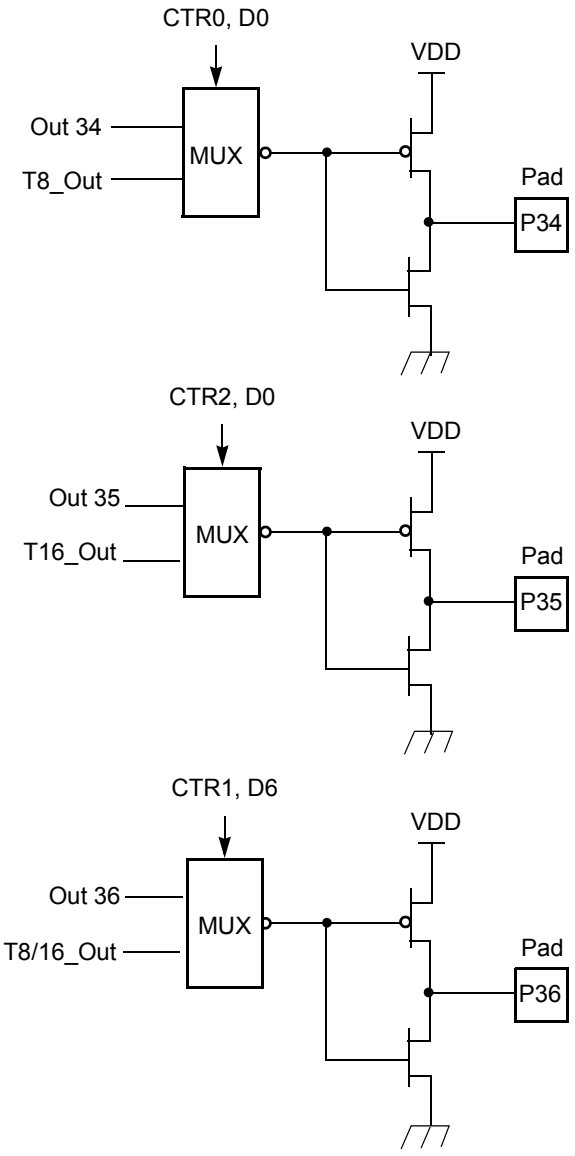


Figure 19. Port 3 Configuration

/RESET (Input, Active Low)

Reset initializes the MCU. Reset is accomplished either through Power-On, Watch-Dog Timer, Stop-Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the reset line need to be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally. There is no condition internal to the Z86E7X that does not allow an external reset to occur.

After the POR time, /RESET is a Schmitt-triggered input. To avoid asynchronous and noisy reset problems, the Z86E7X is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks or for the duration of the external reset, whichever is longer.

During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. Program execution begins at location 000CH, 5–10 TpC cycles after the RST is released. For Power-On Reset, the typical reset output time is 5 ms.

Note: The Z86E7X devices do not have internal pull resistors on Port 3 inputs.

Note: The Extended Data RAM cannot be used as STACK or instruction/code memory. Accessing the Extended Data RAM has the following condition: P01M register bits D4–D3 cannot be set to 11.

External Memory

The Z86E72/73 microcontrollers address up to 32 KB (minus FD00H–FFFFH) of external memory beginning at address 8000H (32K+1). External data memory is included with, or separated from, the external program memory space. /DM, an optional I/O function that is programmed to appear on P34, is used to distinguish between data and program memory space. The state of the /DM signal is controlled by the type of instruction being executed. An LDC op code references PROGRAM (/DM inactive) memory, and an LDE instruction references data (/DM active Low) memory. See Figure 21.

The upper nibble of the register pointer (Figure 23 on page 42) selects which working register group of 16 bytes in the register file, out of the possible 256, is accessed. The lower nibble selects the expanded register file bank and, in the case of the Z86E7X family, banks 0, F, and D are implemented. A 0h in the lower nibble allows the normal register file (bank 0) to be addressed, but any other value from 1h to Fh exchanges the lower 16 registers to an expanded register bank.

For example, Z86E73 (see Figure 22):

```
R253 RP = 00H
     R0 = Port0
     R1 = Port1
     R2 = Port2
     R3 = Port3
```

But if:

```
R253 RP = 0DH
     R0 = CTRL0
     R1 = CTRL1
     R2 = CTRL2
     R3 = Reserved
```

The counter/timers are mapped into ERF group D. Access is easily done using the following example:

```
LD          RP,#0Dh     ; Select ERF D for access and register
                        ; Bank 0 as the working register group.
LD          R0,#xx      ; access CTRL0
LD          1,#xx       ; access CTRL1
LD          RP,#7Dh     ; Select expanded register group (ERF)
                        ; group D for access and register
                        ; Bank 7 as the working register bank.
LD          R1,2        ; CTRL2→register 71H
```

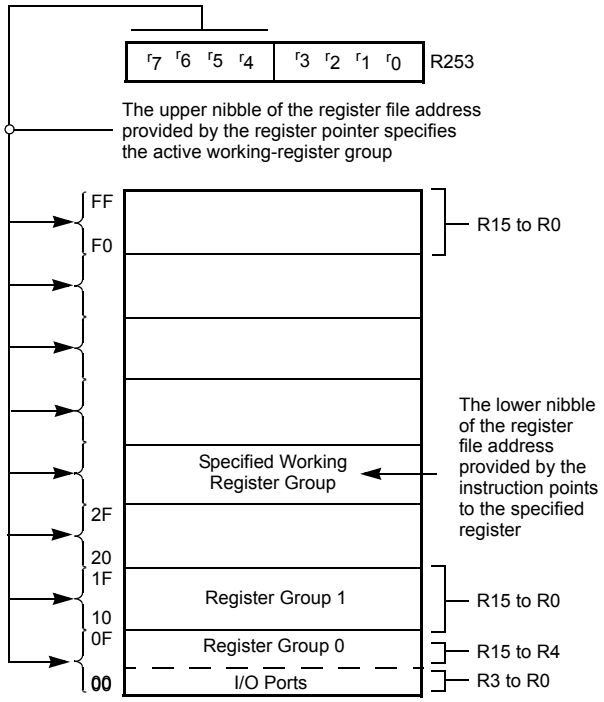


Figure 24. Register Pointer

Stack

The Z86E7X external data memory or the internal register file is used for the stack. An 8-bit stack pointer (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH is used as a general-purpose register only when using internal stacks.

Note: When SPH is used as a general-purpose register and Port 0 is in address mode, the contents of SPH are loaded into Port 0 whenever the internal stack is accessed.

Counter/Timer Register Description

Table 13 describes the expanded register group D.

Table 13. Expanded Register Group D

(D) 0Ch	Reserved
(D) 0Bh	HI8
(D) 0Ah	LO8

Starting Ping-Pong Mode

First, make sure both counter/timers are not running. Then set T8 into Single-Pass Mode (CTR0 D6), set T16 into Single-Pass Mode (CTR2 D6), and set Ping-Pong Mode (CTR1 D2, D3). These instructions do not have to be in any particular order. Finally, start Ping-Pong Mode by enabling either T8 (CTR0 D7) or T16 (CTR2 D7).

During Ping-Pong Mode

The enable bits of T8 and T16 (CTR0 D7, CTR2 D7) are alternately set and cleared by hardware. The time-out bits (CTR0 D5, CTR2 D5) are set every time the counter/timers reach the terminal count.

Output Circuit

Figure 36 shows the output circuit.

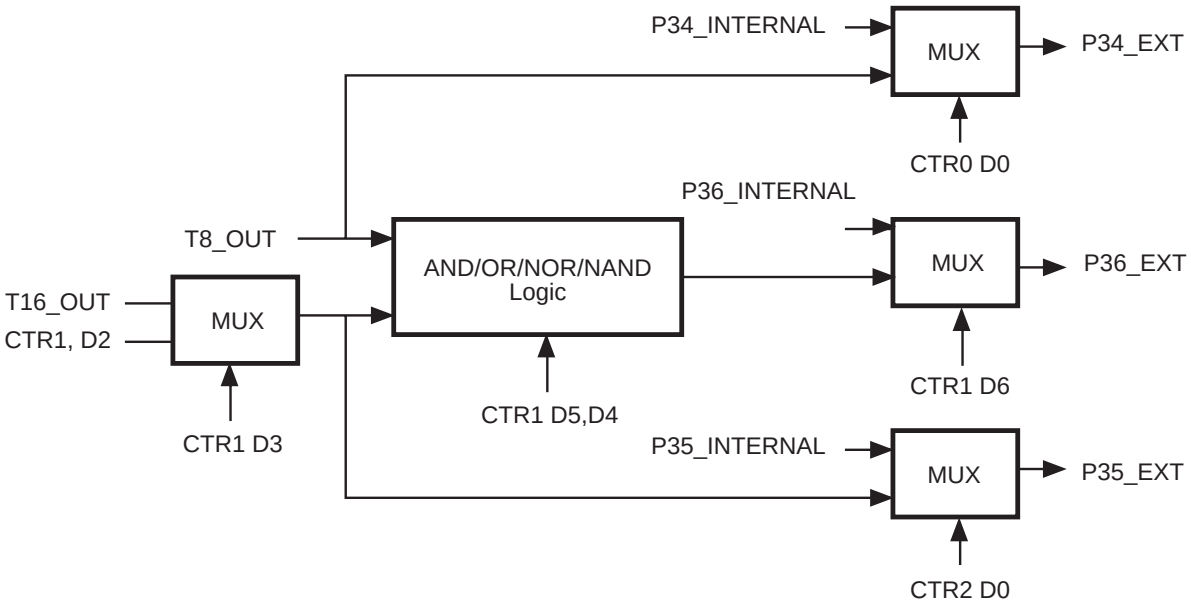


Figure 36. Output Circuit

Interrupts

The Z86E7X has five different interrupts. The interrupts are maskable and prioritized, as shown in Figure 37. The five sources are divided as follows: three sources are claimed by Port 3 lines P33–P31 and the remaining two by the counter/timers (see Table 26). The Interrupt Mask Register globally or individually enables or disables the five interrupt requests.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86E7X interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered and are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 27.

Table 27. IRQ Register

IRQ		Interrupt Edge	
D7	**D6**	**IRQ2 (P31)**	**IRQ0 (P32)**
0	0	F	F
0	1	F	R
1	0	F	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge
In analog mode, the Stop-Mode Recovery sources selected by the SMR register are connected to the IRQ1 input. Any of the Stop-Mode Recovery sources for SMR (except P31, P32, and P33) can be used to generate IRQ1 (falling edge triggered).

Clock

The Z86E7X on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ohms. The Z86E7X on-chip oscillator can be driven with a cost-effective RC network or other suitable external clock source.

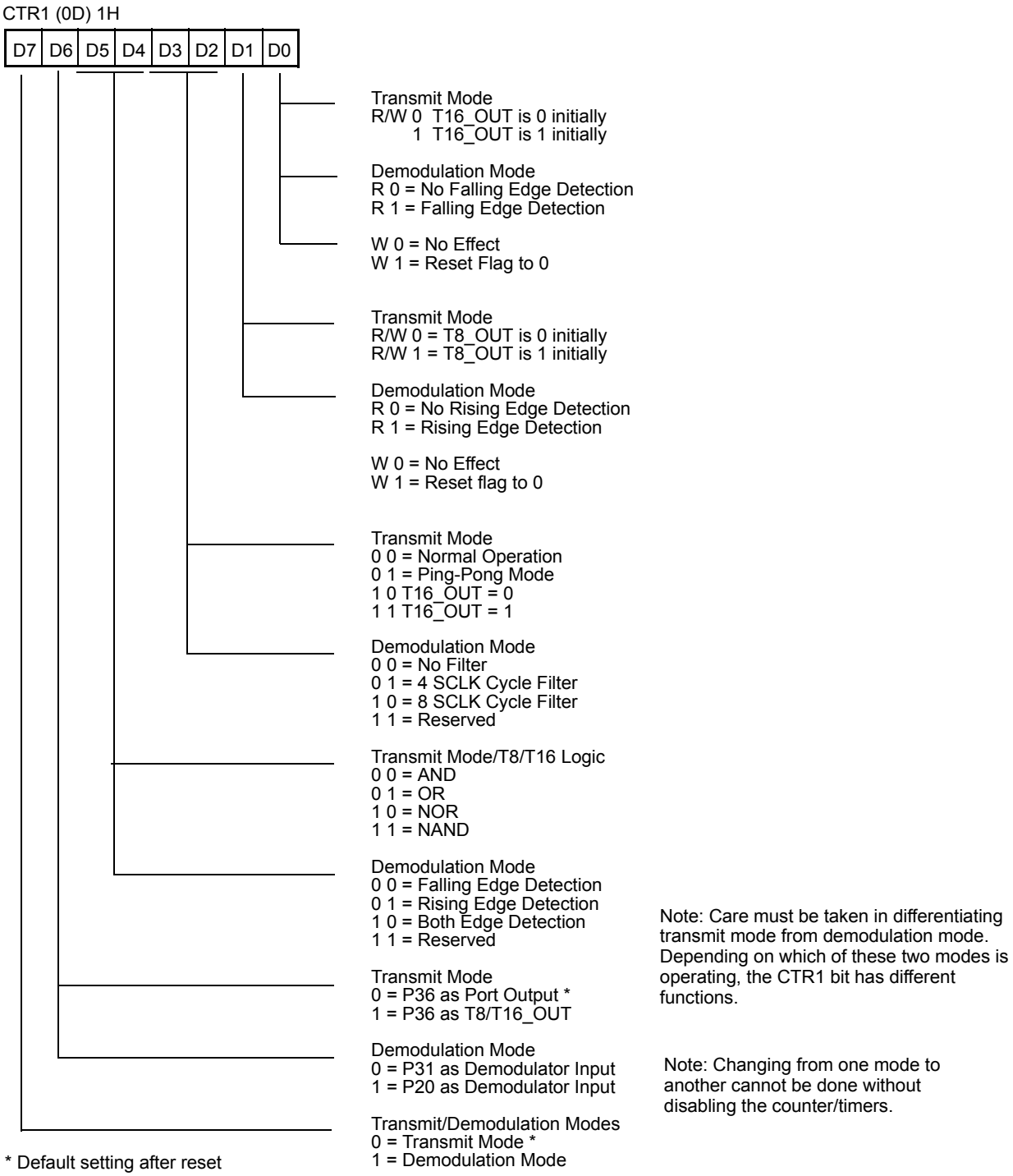


Figure 50. T8 and T16 Common Control Functions—(0D) 1H: Read/Write

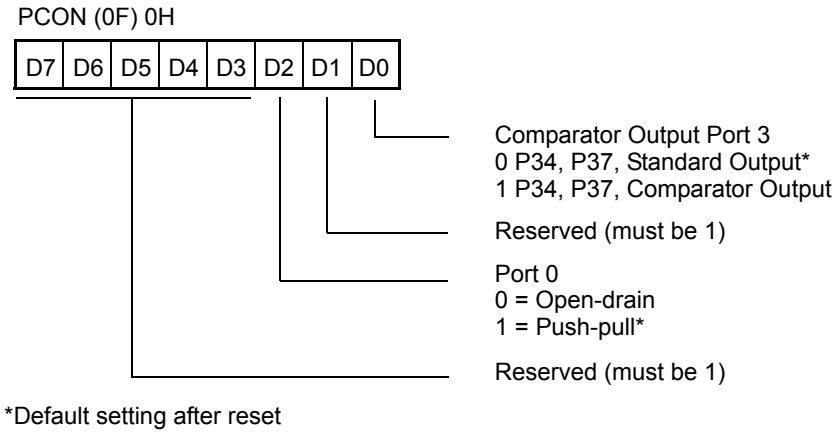


Figure 56. Port Configuration Register (PCON)—(0F) 0H: Write Only

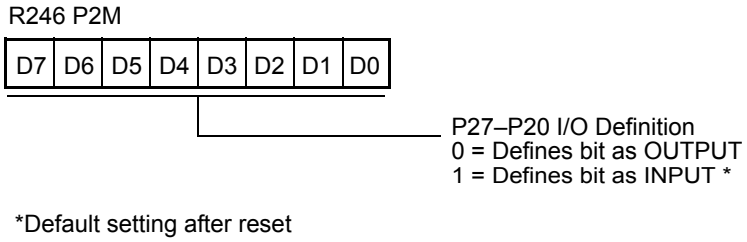


Figure 57. Port 2 Mode Register—F6H: Write Only

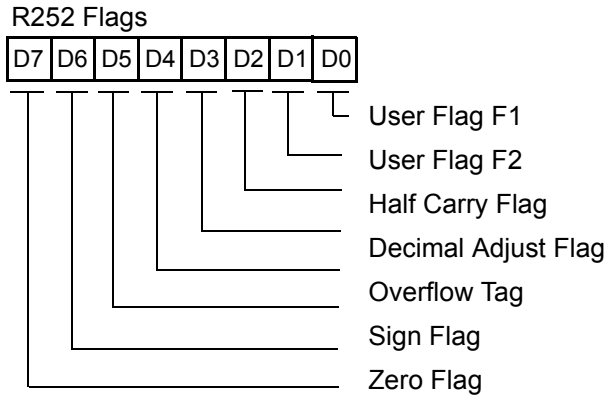


Figure 63. Flag Register—(0) FCH: Read/Write

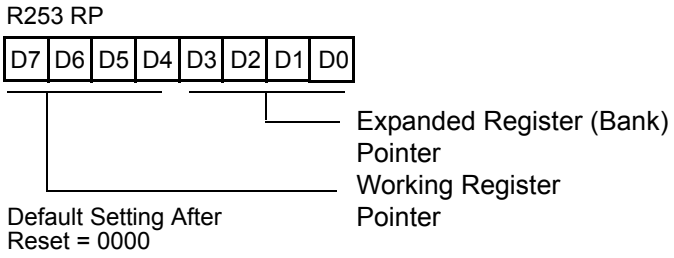


Figure 64. Register Pointer—(0) FDH: Read/Write

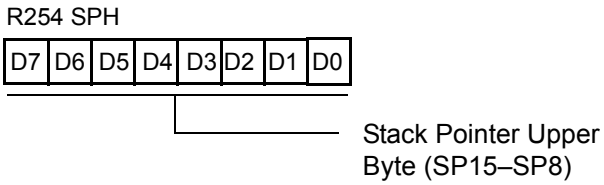


Figure 65. Stack Pointer High—(0) FEH: Read/Write

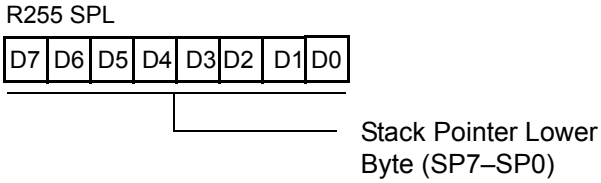


Figure 66. Stack Pointer Low—(0) FFH: Read/Write