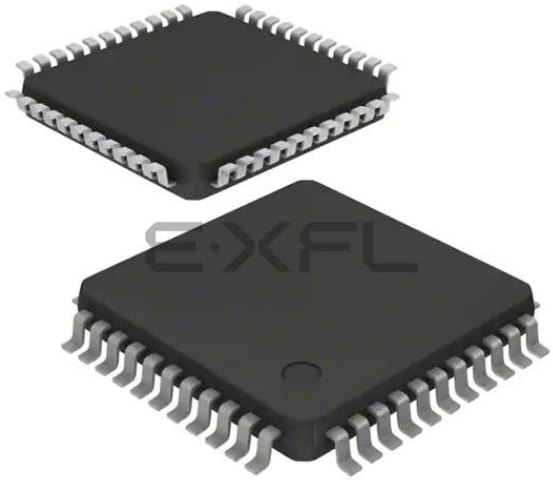

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e7316asg

Warning: DO NOT USE IN LIFE SUPPORT

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As used herein

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Table 3. Pin Identification (Standard Mode) (Continued)

40-Pin DIP #	44-Pin PLCC #	44-Pin LQFP #	Symbol	Direction	Description
29	43	26	P11	Input/Output	Port 1 can be configured as multiplexed A7–A0/D7–D0 external program ROM Address/Data Bus
32	3	30	P12	Input/Output	
33	4	31	P13	Input/Output	
8	20	3	P14	Input/Output	.
9	21	4	P15	Input/Output	
12	25	8	P16	Input/Output	
13	26	9	P17	Input/Output	
35	6	33	P20	Input/Output	Port 2 pins are individually configurable as input or output
36	7	34	P21	Input/Output	
37	8	35	P22	Input/Output	
38	9	36	P23	Input/Output	
39	10	37	P24	Input/Output	
2	14	41	P25	Input/Output	
3	15	42	P26	Input/Output	
4	16	43	P27	Input/Output	
16	29	12	P31	Input	IRQ2/Modulator input
17	30	13	P32	Input	IRQ0
18	31	14	P33	Input	IRQ1
19	32	15	P34	Output	T8 output
22	36	19	P35	Output	T16 output
24	38	21	P36	Output	T8/T16 output
23	37	20	P37	Output	
20	33	16	/AS	Output	Address Strobe
40	11	38	/DS	Output	Data Strobe
1	13	40	R//W	Output	Read/Write
21	35	18	/RESET	Input	Reset
15	28	11	XTAL1	Input	Crystal, Oscillator Clock

Table 8. DC Characteristics (Continued)

Sym.	Parameter	V_{CC}	T_A = 0 °C to +70 °C Min	Max	Typical @ 25°C	Units	Conditions
V_{RAM}	Static RAM Data Retention Voltage	Vram			0.5	V	Worst case 0.8 V guaranteed by design only Note 6

Notes:	ICC1	Typ	Max	Unit	Frequency
	Crystal/Resonator	3.0 mA	5	mA	8.0 MHz
	External Clock Drive	0.3 mA	5	mA	8.0 MHz

1. All outputs unloaded, inputs at rail
2. CL1 = CL2 = 100 pF
3. Same as note [4] except inputs at V_{CC}
4. The V_{LV} increases as the temperature decreases.
5. Oscillator stopped
6. Oscillator does not stop when V_{CC} falls below V_{LV} threshold.
7. 32 kHz clock driver input
8. For analog comparator, inputs when analog comparators are enabled
9. WDT, Comparators, Low Voltage Detection, and ADC (if applicable) are disabled. The IC might draw more current if any of the above peripherals is enabled.

* All outputs excluding P00, P01, P36, and P37

Table 9. External I/O or Memory Read and Write Timing

				T_A = 0 °C to +70 °C 16 MHz			
No.	**Symbol**	**Parameter**	**V_{CC}**	**Min.**	**Max.**	**Units**	**Notes**
1	TdA(AS)	Address Valid to /AS Rising Delay	3.0 V 5.5 V	55 55		ns ns	2
2	TdAS(A)	/AS Rising to Address Float Delay	3.0 V 5.5 V	70 70		ns ns	2
3	TdAS(DR)	/AS Rising to Read Data Required Valid	3.0 V 5.5 V		400 400	ns ns	1, 2 1, 2
4	TwAS	/AS Low Width	3.0 V 5.5 V	80 80		ns ns	2 2
5	Td	Address Float to /DS Falling	3.0 V 5.5 V	0 0		ns ns	
6	TwDSR	/DS (Read) Low Width	3.0 V 5.5 V	300 300		ns ns	1, 2
7	TwDSW	/DS (Write) Low Width	3.0 V 5.5 V	165 165		ns ns	1, 2
8	TdDSR(DR)	/DS Falling to Read Data Required Valid	3.0 V 5.5 V		260 260	ns ns	1, 2
9	ThDR(DS)	Read Data to /DS Rising Hold Time	3.0 V 5.5 V	0 0		ns ns	
10	TdDS(A)	/DS Rising to Address Active Delay	3.0 V 5.5 V	85 95		ns ns	2
11	TdDS(AS)	/DS Rising to /AS Falling Delay	3.0 V 5.5 V	60 70		ns ns	2
12	TdR/W(AS)	R//W Valid to /AS Rising Delay	3.0 V 5.5 V	70 70		ns ns	2
13	TdDS(R/W)	/DS Rising to R//W Not Valid	3.0 V 5.5 V	70 70		ns ns	2
14	TdDW(DSW)	Write Data Valid to /DS Falling (Write) Delay	3.0 V 5.5 V	80 80		ns ns	2
15	TdDS(DW)	/DS Rising to Write Data Not Valid Delay	3.0 V 5.5 V	70 80		ns ns	2
16	TdA(DR)	Address Valid to Read Data Required Valid	3.0 V 5.5 V		475 475	ns ns	1, 2

Table 9. External I/O or Memory Read and Write Timing (Continued)

				T_A = 0 °C to +70 °C 16 MHz			
No.	**Symbol**	**Parameter**	**V_{CC}**	**Min.**	**Max.**	**Units**	**Notes**
17	TdAS(DS)	/AS Rising to /DS Falling Delay	3.0 V 5.5 V	100 100		ns ns	2 2
18	TdDM(AS)	/DM Valid to /AS Falling Delay	3.0 V 5.5 V	55 55		ns ns	2
19	TdDS(DM)	/DS Rise to /DM Valid Delay	3.0 V 5.5 V	70 70		ns ns	
20	ThDS(A)	/DS Rise to Address Valid Hold Time	3.0 V 5.5 V	70 70		ns ns	

Notes:
1. When using extended memory timing, add 2 TpC.
2. Timing numbers given are for minimum TpC.

Standard Test Load

All timing references use 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.

Figure 11 shows additional timing. Table 10 describes the additional timing.

Pin Functions

/DS (Output, Active Low)

Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available before the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS (Output, Active Low)

Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant, crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

R//W Read/Write (Output, Write Low)

The R//W signal is Low when the CCP is writing to the external program or data memory.

R//RL (Input)

This pin, when connected to GND, disables the internal ROM and forces the device to function as a ROMless Z8.

Note: When left unconnected or pulled high to V_{CC}, the part functions normally as a Z8 ROM version.

Port 0 (P07–P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port or as an address port for interfacing external memory. The output drivers are push-pull. Port 0 is placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0. Handshake signal direction is

/RESET (Input, Active Low)

Reset initializes the MCU. Reset is accomplished either through Power-On, Watch-Dog Timer, Stop-Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the reset line need to be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally. There is no condition internal to the Z86E7X that does not allow an external reset to occur.

After the POR time, /RESET is a Schmitt-triggered input. To avoid asynchronous and noisy reset problems, the Z86E7X is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks or for the duration of the external reset, whichever is longer.

During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. Program execution begins at location 000CH, 5–10 TpC cycles after the RST is released. For Power-On Reset, the typical reset output time is 5 ms.

Note: The Z86E7X devices do not have internal pull resistors on Port 3 inputs.

Functional Description

The Z86E72/73 microcontrollers incorporate special functions to enhance the Z8's functionality in consumer and battery-operated applications.

Reset

The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source
- Low Voltage Detection
- External Reset

Program Memory

The Z86E72/73 microcontrollers address up to 16K/32 KB of internal program memory, with the remainder being external memory (Figure 20). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain five 16-bit vectors that correspond to the five available interrupts. Addresses of 16K/32K consist of on-chip OTP. At addresses 16K or 32K and greater, the Z86E72/73 microcontrollers execute external program memory fetches (see “External Memory” on page 38).

The upper nibble of the register pointer (Figure 23 on page 42) selects which working register group of 16 bytes in the register file, out of the possible 256, is accessed. The lower nibble selects the expanded register file bank and, in the case of the Z86E7X family, banks 0, F, and D are implemented. A 0h in the lower nibble allows the normal register file (bank 0) to be addressed, but any other value from 1h to Fh exchanges the lower 16 registers to an expanded register bank.

For example, Z86E73 (see Figure 22):

```
R253 RP = 00H
     R0 = Port0
     R1 = Port1
     R2 = Port2
     R3 = Port3
```

But if:

```
R253 RP = 0DH
     R0 = CTRL0
     R1 = CTRL1
     R2 = CTRL2
     R3 = Reserved
```

The counter/timers are mapped into ERF group D. Access is easily done using the following example:

```
LD          RP,#0Dh     ; Select ERF D for access and register
                        ; Bank 0 as the working register group.
LD          R0,#xx      ; access CTRL0
LD          1,#xx       ; access CTRL1
LD          RP,#7Dh     ; Select expanded register group (ERF)
                        ; group D for access and register
                        ; Bank 7 as the working register bank.
LD          R1,2        ; CTRL2→register 71H
```

Figure 22. Expanded Register File Architecture

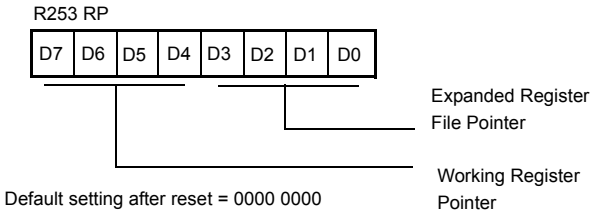

Figure 23. Register Pointer

Register File

The register file (bank 0) consists of 4 I/O port registers, 236 general-purpose registers, and 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), plus two expanded registers groups (Banks D and F). Instructions can access registers directly or indirectly through an 8-bit address field. This allows a short, 4-bit register address using the register pointer (Figure 24). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The register pointer addresses the starting location of the active working register group.

Note: Working register group E0–EF of Bank 0 are only accessed through working registers and indirect addressing modes.

HI16(D)09h Register

This register (Table 16) holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Table 16. HI16(D)09h Register

Field	Bit Position	Value	Description
T16_Capture_HI	76543210	R/W	Captured Data No Effect

L016(D)08h Register

This register (Table 17) holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Table 17. LO16(D)08h Register

Field	Bit Position	Value	Description
T16_Capture_LO	76543210	R/W	Captured Data No Effect

TC16H(D)07h Register

Table 18 describes the Counter/Timer2 MS-Byte Hold Register.

Table 18. TC16H(D)07h Register

Field	Bit Position	Value	Description
T16_Data_HI	76543210	R/W	Data

TC16L(D)06h Register

Table 19 describes the Counter/Timer2 LS-Byte Hold Register.

Table 19. TC16L(D)06h Register

Field	Bit Position	Value	Description
T16_Data_LO	76543210	R/W	Data

TC8H(D)05h Register

Table 20 describes the Counter/Timer8 High Hold Register.

Table 20. TC8H(D)05h Register

Field	Bit Position	Value	Description
T8_Level_HI	76543210	R/W	Data

TC8L(D)04h Register

Table 21 describes the Counter/Timer8 Low Hold Register.

Table 21. TC8L(D)04h Register

Field	Bit Position	Value	Description
T8_Level_LO	76543210	R/W	Data

CTR0(D)00h Register

Table 22 describes the Counter/Timer8 Control Register.

Table 22. CTR0(D)00h Register

Field	Bit Position		Value	Description
T8_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo	-6------	R/W	0	Modulo-N
			1	Single Pass
Time_Out	--5------	R	0	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
		W	1	Reset Flag to 0
T8 _Clock	---43---	R/W	0 0	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_MASK	-----2--	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.

In demodulation mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge, but ignores the subsequent edges. For details, see “T16 Demodulation Mode” on page 60.

Time_Out

This bit is set when T16 times out (terminal count reached). To reset it, a 1 must be written to this location.

T16_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask

Set this bit to allow interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask

Set this bit to allow interrupt when T16 times out.

P35_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

SMR2(F)0Dh Register

Table 25 describes Stop-Mode Recovery Register 2.

Table 25. SMR2(F)0Dh Register

Field	Bit Position		Value	Description
Reserved	7-------		0	Reserved (Must be 0)
Recovery Level	-6------	W	0* 1	Low High
Reserved	--5-----		0	Reserved (Must be 0)
Source	---432--	W	000* 001 010 011 100 101 110 111	A. POR Only B. NAND of P23–P20 C. NAND or P27–P20 D. NOR of P33–P31 E. NAND of P33–P31 F. NOR of P33–P31, P00, P07 G. NAND of P33–P31, P00, P07 H. NAND of P33–P31, P22–P20
Reserved	------10		00	Reserved (Must be 0)

Note: * Indicates the value upon Power-On Reset.

Starting Ping-Pong Mode

First, make sure both counter/timers are not running. Then set T8 into Single-Pass Mode (CTR0 D6), set T16 into Single-Pass Mode (CTR2 D6), and set Ping-Pong Mode (CTR1 D2, D3). These instructions do not have to be in any particular order. Finally, start Ping-Pong Mode by enabling either T8 (CTR0 D7) or T16 (CTR2 D7).

During Ping-Pong Mode

The enable bits of T8 and T16 (CTR0 D7, CTR2 D7) are alternately set and cleared by hardware. The time-out bits (CTR0 D5, CTR2 D5) are set every time the counter/timers reach the terminal count.

Output Circuit

Figure 36 shows the output circuit.

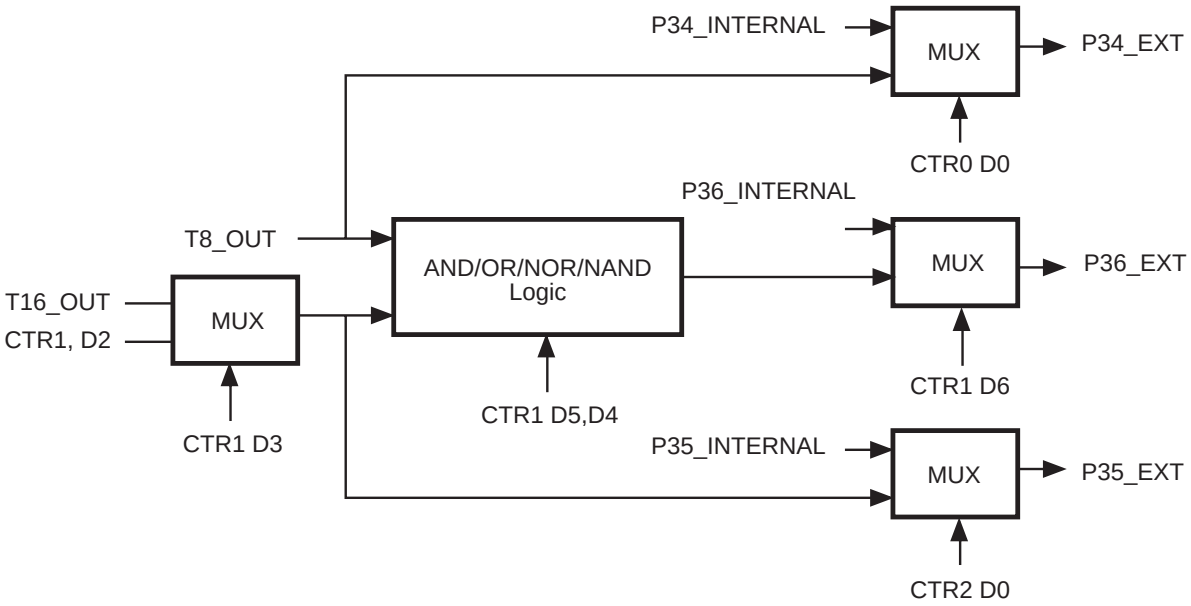

Figure 36. Output Circuit

Interrupts

The Z86E7X has five different interrupts. The interrupts are maskable and prioritized, as shown in Figure 37. The five sources are divided as follows: three sources are claimed by Port 3 lines P33–P31 and the remaining two by the counter/timers (see Table 26). The Interrupt Mask Register globally or individually enables or disables the five interrupt requests.

Expanded Register File Control Registers (0D)

Figure 49 through Figure 51 show the expanded register file control registers (0D).

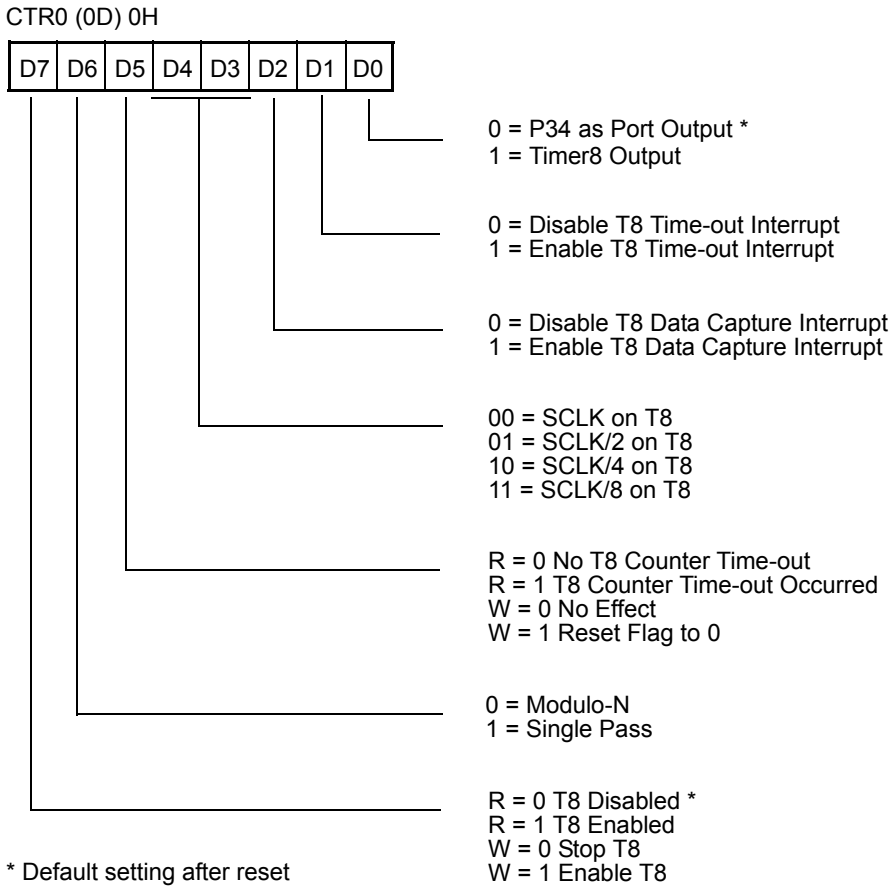

Figure 49. TC8 Control Register—(0D) 0H: Read/Write Except Where Noted

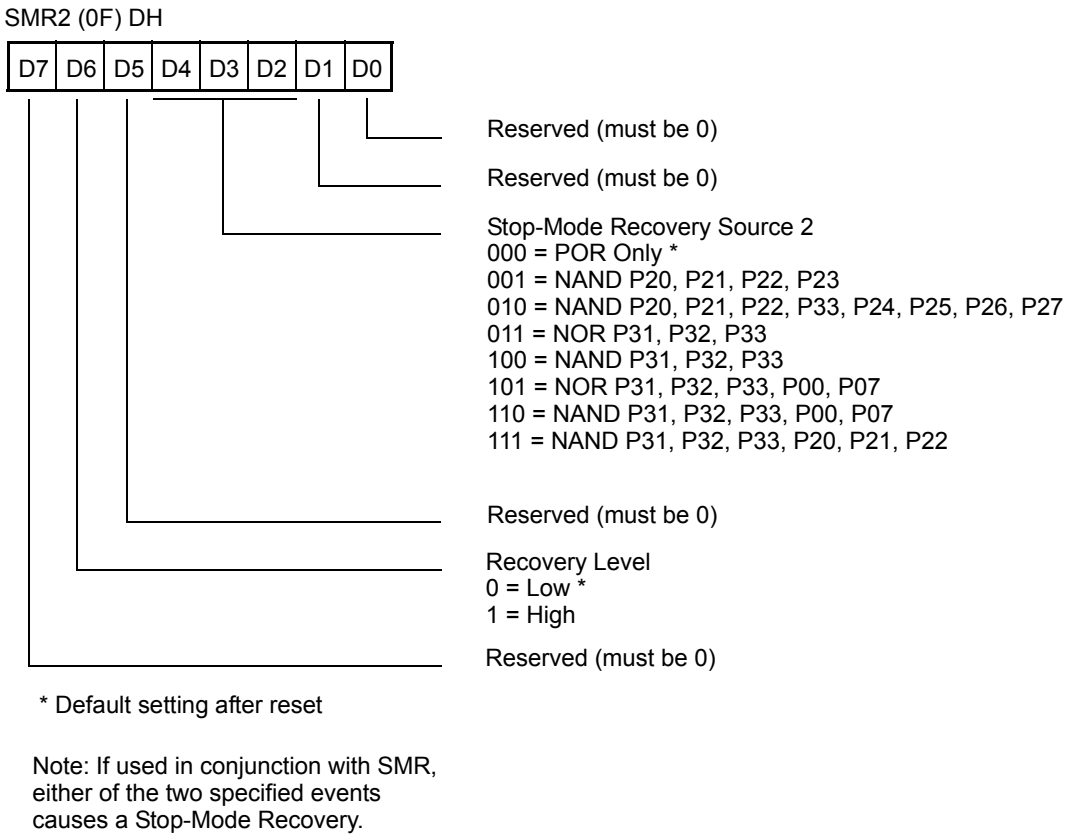

Figure 53. Stop-Mode Recovery Register 2—(0F) DH: D2–D4, D6 Write Only

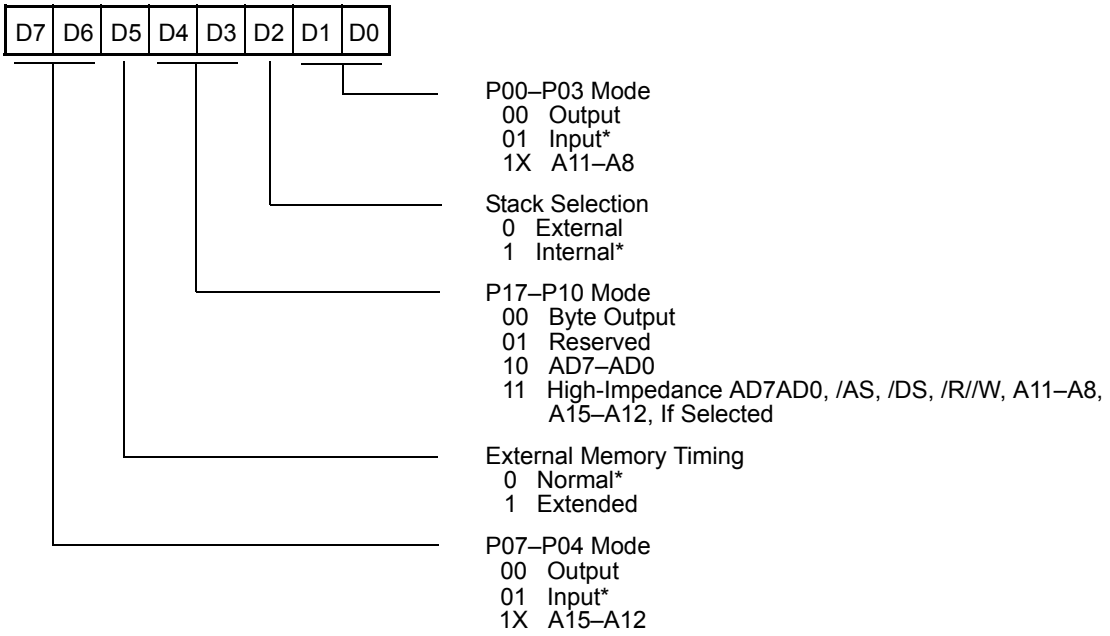

Figure 59. Port 0 and 1 Mode Register—F8H: Write Only

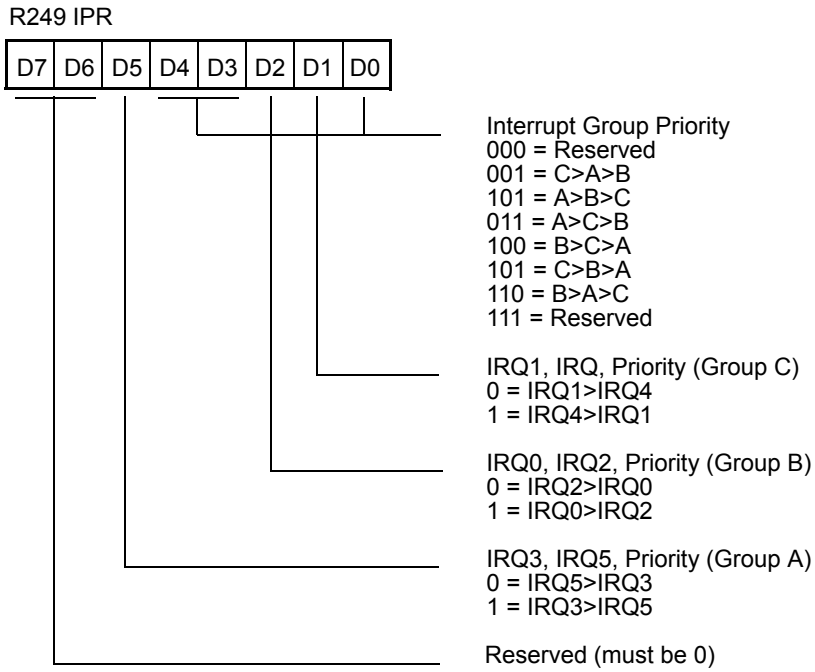

Figure 66. Stack Pointer Low—(0) FFH: Read/Write

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