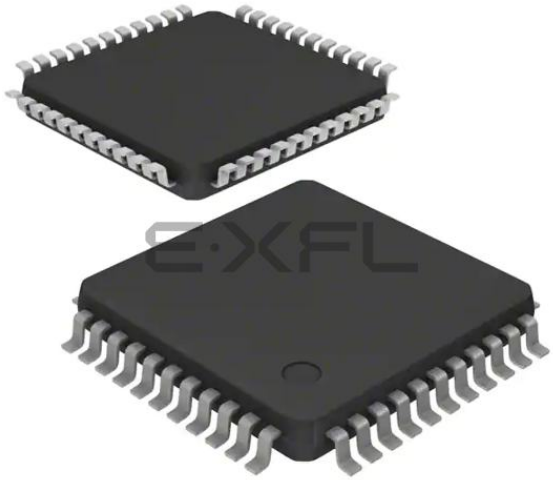

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e7316fsc

Table of Contents

Features

Table 1 lists some of the features of the Z86E72/73 microcontrollers.

Table 1. Z86E72/73 Features

Part	ROM (KB)	RAM* (Bytes)	I/O	Voltage Range
Z86E73	32	236	31	3.0 V to 5.5 V
Z86E72	16	748	31	3.0 V to 5.5 V

Note: *General-purpose

- Low power consumption—60 mW (typical)
- Two standby modes (typical)
  - STOP—2 μA
  - HALT—0.8 mA
- Special architecture to automate both generation and reception of complex pulses or signals:
  - One programmable 8-bit counter/timer with two capture registers
  - One programmable 16-bit counter/timer with one capture register
  - Programmable input glitch filter for pulse reception
- Five priority interrupts
  - Three external
  - Two assigned to counter/timers
- Two independent comparators with programmable interrupt polarity
- On-chip oscillator that accepts a crystal, ceramic resonator, LC, RC (mask option), or external clock drive
- Software-selectable 200±50% KΩ resistive transistor pull-ups on Port 0 and Port 2
  - Port 2 pull-ups are bit selectable
  - Pull-ups automatically disabled as outputs
- Software mouse/trackball interface on P00 through P03

General Description

The Z86E7X family are OTP-based members of the Z8® MCU single-chip family with 236 or 748 bytes of general-purpose RAM. The only differentiating factor between the E72/73 versions is the availability of RAM and ROM. This EPROM microcontroller family of OTP controllers also offers the use of external memory, which enables this Z8 microcontroller to be used where code flexibility is required. ZiLOG's CMOS microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and easy hardware/software system expansion along with cost-effective and low power consumption.

The Z86E7X architecture is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File to allow access to register-mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The Z8 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

Z8 applications demand powerful I/O capabilities. The Z86E7X family fulfills this with three package options in which the E72/73 versions provide 31 pins of dedicated input and output. These lines are grouped into four ports. Each port consists of eight lines (Port 3 has seven lines of I/O and one Pref comparator input) and is configurable under software control to provide timing, status signals, parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are five basic address spaces available to support a wide range of configurations: program memory, register file, Expanded Register File, Extended Data RAM, and external memory. The register file is composed of 256 bytes of RAM. It includes 4 I/O port registers, 16 control and status registers, and the rest are general-purpose registers. The Extended Data RAM adds 512 (E72) of usable general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86E7X family offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages (Figure 19 on page 34).

Note: All signals with a preceding front slash, “/”, are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Table 8. DC Characteristics (Continued)

			T_A = 0 °C to +70 °C		Typical		
Sym.	**Parameter**	**V_{CC}**	**Min**	**Max**	**@ 25°C**	**Units**	**Conditions**
I_{IR}	Reset Input Current	3.0 V 5.5 V		–230 –400	–50 –80	µA µA	
I_{CC}	Supply Current (WDT off)	3.0 V 5.5 V		10 15	4 10	mA mA	@ 8.0 MHz @ 8.0 MHz
I_{CC1}	Standby Current (WDT Off)	3.0 V		3	1	mA	HALT Mode V_{IN} = 0 V, V_{CC} at 8.0 MHz, Notes 1, 2
		5.5 V		5	4	mA	HALT Mode V_{IN} = 0 V, V_{CC} @ 8.0 MHz, Notes 1, 2
		3.0 V		2	0.8	mA	Clock Divide-by-16 @ 8.0 MHz Notes 1, 2
		5.5 V		4	2.5	mA	Clock Divide-by-16 @ 8.0 MHz Notes 1, 2
I_{CC2}	Standby Current	3.0 V		8	2	µA	STOP Mode V_{IN} = 0 V, V_{CC} WDT is not Running Notes 3, 5, 9
		5.5 V		10	3	µA	STOP Mode V_{IN} = 0 V, V_{CC} WDT is not Running Notes 3, 5, 9
		3.0 V		500	310	µA	STOP Mode Notes 3, 5
		5.5 V		800	600	µA	V_{IN} = 0 V, V_{CC} WDT is Running
V_{ICR}	Input Common Mode Voltage Range	3.0 V 5.5 V	0 0	V_{CC}–1.0 V V_{CC}–1.0 V	V V		Note 8
V_{LV}	VCC Low-Voltage Detection			2.9 V	2.55 V		Note 6
T_{POR}	Power-On Reset	3.0 V 5.5 V	12 5	75 20	18 7	ms ms	

Table 8. DC Characteristics (Continued)

Sym.	Parameter	V_{CC}	T_A = 0 °C to +70 °C Min	Max	Typical @ 25°C	Units	Conditions
V_{RAM}	Static RAM Data Retention Voltage	Vram			0.5	V	Worst case 0.8 V guaranteed by design only Note 6

Notes:	ICC1	Typ	Max	Unit	Frequency
	Crystal/Resonator	3.0 mA	5	mA	8.0 MHz
	External Clock Drive	0.3 mA	5	mA	8.0 MHz

1. All outputs unloaded, inputs at rail
2. CL1 = CL2 = 100 pF
3. Same as note [4] except inputs at V_{CC}
4. The V_{LV} increases as the temperature decreases.
5. Oscillator stopped
6. Oscillator does not stop when V_{CC} falls below V_{LV} threshold.
7. 32 kHz clock driver input
8. For analog comparator, inputs when analog comparators are enabled
9. WDT, Comparators, Low Voltage Detection, and ADC (if applicable) are disabled. The IC might draw more current if any of the above peripherals is enabled.

* All outputs excluding P00, P01, P36, and P37

Table 10. Additional Timing (Continued)

				T_A = 0°C to +70°C			
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
6	TpTi	Timer Input Period	3.0 V 5.5 V	8TpC 8TpC			1
7	TrTin,TfTi	Timer Input Rise and Fall Timers	3.0 V 5.5 V	100 70		ns ns	1 1
8A	TwIL	Interrupt Request Low Time	3.0 V 5.5 V	100 70		ns ns	1, 2 1, 2
8B	TwIL	Int. Request Low Time	4.5 V 5.5 V	3TpC 5TpC			1, 3 1, 3
9	TwIH	Interrupt Request Input High Time	4.5 V 5.5 V	5TpC 5TpC			1, 2 1, 2
10	Twsm	Stop-Mode Recovery Width Spec	3.0 V 5.5 V 3.0 V 5.5 V	12 12 5TpC 5TpC		ns ns	7 7 6 6
11	Tost	Oscillator Start-up Time	3.0 V 5.5 V		5TpC 5TpC		4
12	Twdt	Watch-Dog Timer Delay Time (5 ms)	3.0 V 5.5 V	12 5	75 20	ms ms	
		(10 ms)	3.0 V 5.5 V	25 10	150 40	ms ms	
		(20 ms)	3.0 V 5.5 V	50 20	300 80	ms ms	
		(80 ms)	3.0 V 5.5 V	225 80	1200 320	ms ms	

Notes:
1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. Interrupt request through Port 3 (P30).
4. SMR – D5 = 0
5. Reg. WDTMR
6. Reg. SMR – D5 = 0
7. Reg. SMR – D5 = 1

Figure 12 shows the input handshake timing, and Figure 13 shows the output handshake timing. Table 11 describes the handshake timing.

dictated by the I/O direction to Port 0 of the upper nibble P07–P04. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 can provide address bits A11–A8 (lower nibble) or A15–A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

Port 0 is set in the High-Impedance Mode if selected as an address output state along with Port 1 and the control signals /AS, /DS, and R//W.

A software option is available to program 0.4 V_{DD} CMOS trip inputs on P00–P03. This allows direct interface to mouse/trackball IR sensors.

An optional 200±50% KΩ resistive transistor pull-up is available as a software option of all Port 0 bits with nibble select.

These pull-ups are disabled when configured (bit by bit) as an output. See Figure 14.

Figure 16. Port 2 Configuration

The CCP wakes up with the 8 bits of Port 2 configured as inputs with open-drain outputs.

Port 2 also has an 8-bit input OR and an AND gate that can be used to wake up the part. P20 can be programmed to access the edge-selection circuitry.

Port 3 (P37–P31)

Port 3 is a 7-bit, CMOS-compatible port (see Figure 17). Port 3 consists of three fixed inputs (P33–P31) and four fixed outputs (P37–P34) and can be configured under software control for Input/Output, Interrupt, Port handshake, Data Memory functions, and output from the counter/timers. P31, P32, and P33 are standard CMOS inputs; outputs are push-pull.

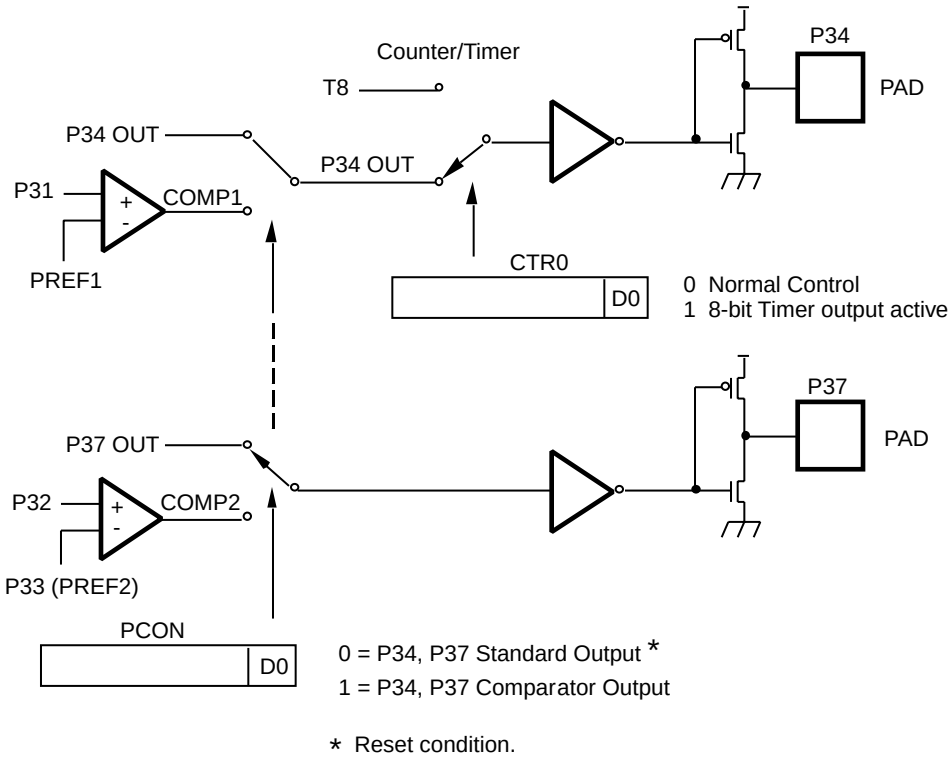


Figure 17. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32 with reference to the voltage on Pref1 and P33. The analog function is enabled by program-

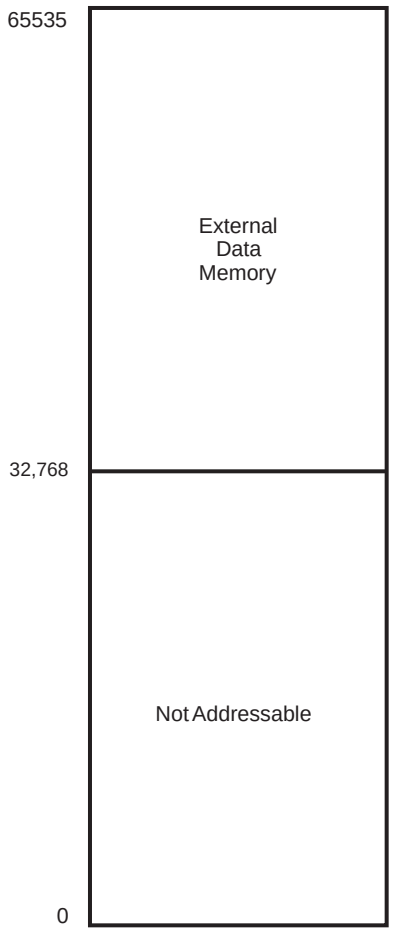


Figure 21. External Memory Map

Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8 register address space R0 through R15 has been implemented as 16 banks of 16 registers per bank. These register groups are known as the Expanded Register File (ERF).

Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

Note: The expanded register bank is also referred to as the expanded register group (see Figure 22).

Table 22. CTR0(D)00h Register (Continued)

Field	Bit Position		Value	Description
Counter_INT_Mask	------1-	R/W	0 1	Disable Time-Out Int. Enable Time-Out Int.
P34_Out	-------0	R/W	0* 1	P34 as Port Output T8 Output on P34

Note: *Indicates the value upon Power-On Reset

T8 Enable

This field enables T8 when set (written) to 1.

Single/Modulo-N

When set to 0 (modulo-n), the counter reloads the initial value when the terminal count is reached. When set to 1 (single pass), the counter stops when the terminal count is reached.

Time-Out

This bit is set when T8 times out (terminal count reached). To reset this bit, a 1 must be written to this location.

Notes: This is the only way to reset this status condition; therefore, you must reset this bit before using/enabling the counter/timers.

Care must be taken when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (demodulation mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers. For example, when the status of bit 5 is 1, a reset condition occurs.

T8 Clock

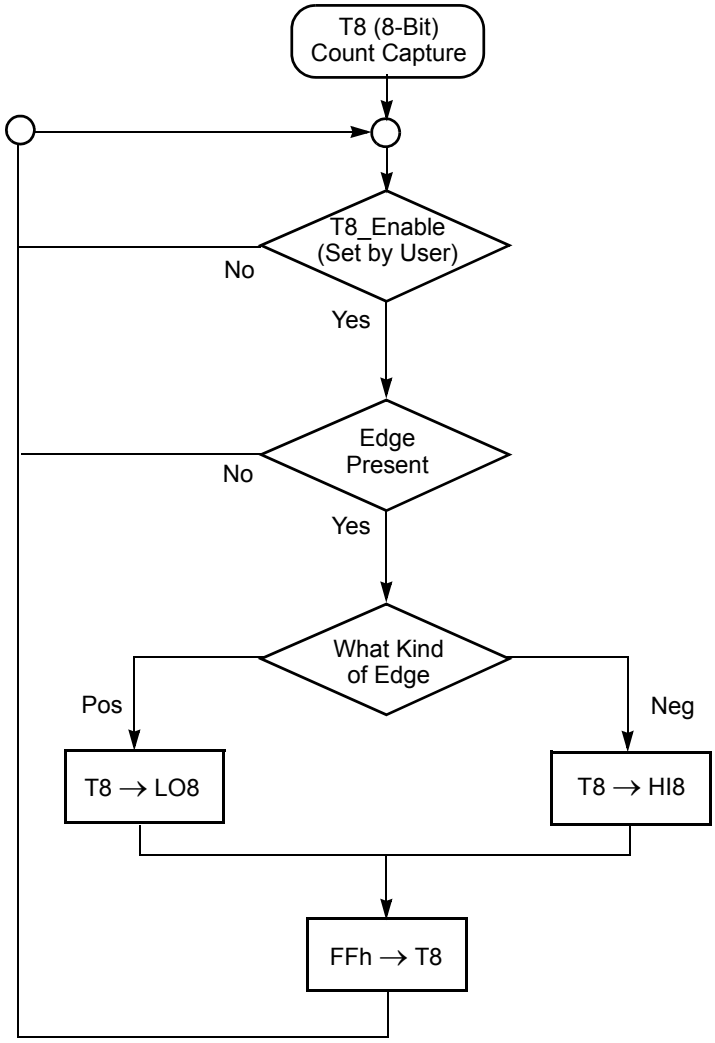
This bit defines the frequency of the input signal to T8.

Capture_INT_Mask

Set this bit to allow interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

T8 Demodulation Mode

You need to program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1 D5, D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1 D5, D4) is detected during counting, the current value of T8 is one's complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if negative edge, HI8. One of the edge-detect status bits (CTR1 D1, D0) is set, and an interrupt can be generated if enabled (CTR0 D2). Meanwhile, T8 is loaded with FFh and starts counting again. When T8 reaches 0, the time-out status bit (CTR0 D5) is set, an interrupt can be generated if enabled (CTR0 D1), and T8 continues counting from FFh (see Figure 30 and Figure 31).



Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the port to its standard I/O configuration.

Port 0 Output Mode (D2)

Bit 2 controls the output mode of Port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 40). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop-Mode Recovery signal. Bit D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

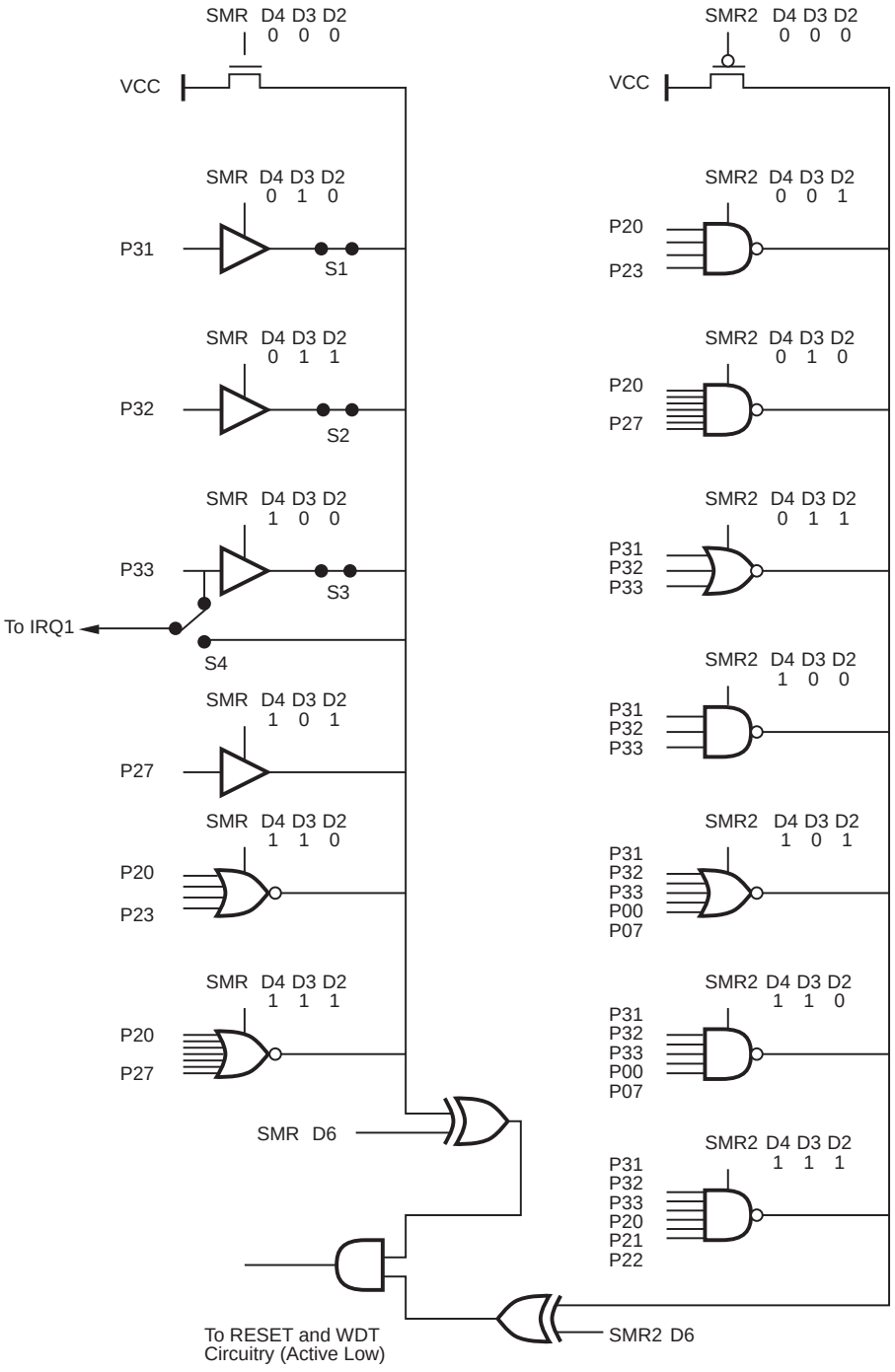


Figure 40. Stop-Mode Recovery Register

Stop-Mode Recovery Register 2 (SMR2)

This register (see Figure 42) determines the mode of STOP Mode recovery for SMR2.

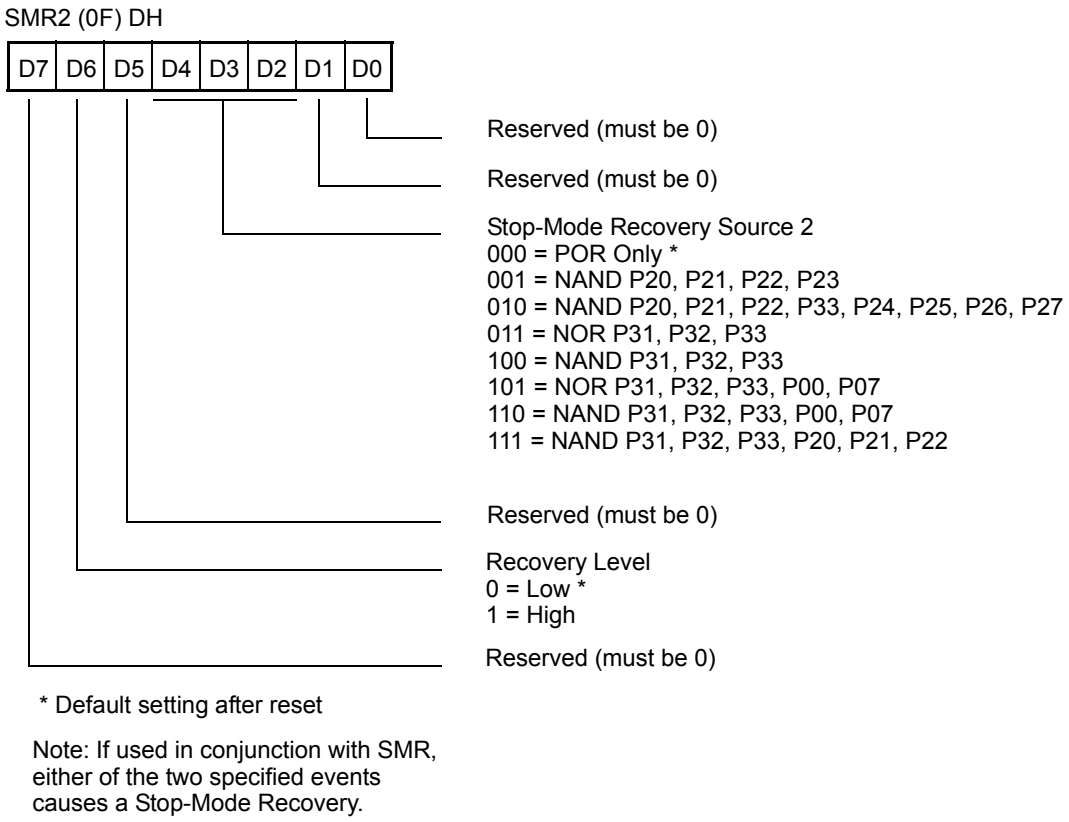


Figure 42. Stop-Mode Recovery Register 2—(0F) DH: D2–D4, D6 Write Only

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop-Mode Recovery.

Note: Port pins configured as outputs are ignored as a SMR or SMR2 recovery source. For example, if the NAND of P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.

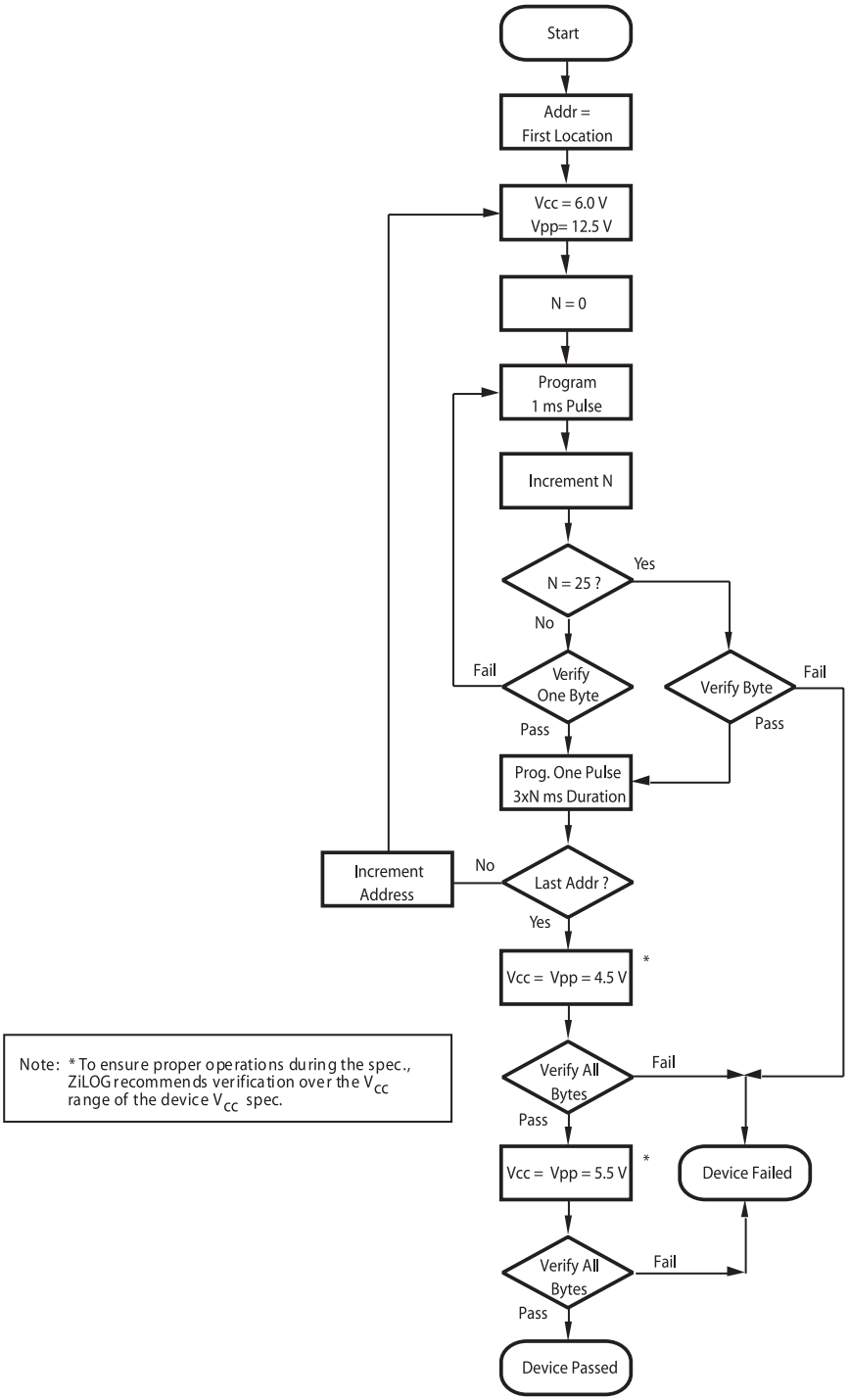


Figure 48. Programming Flowchart

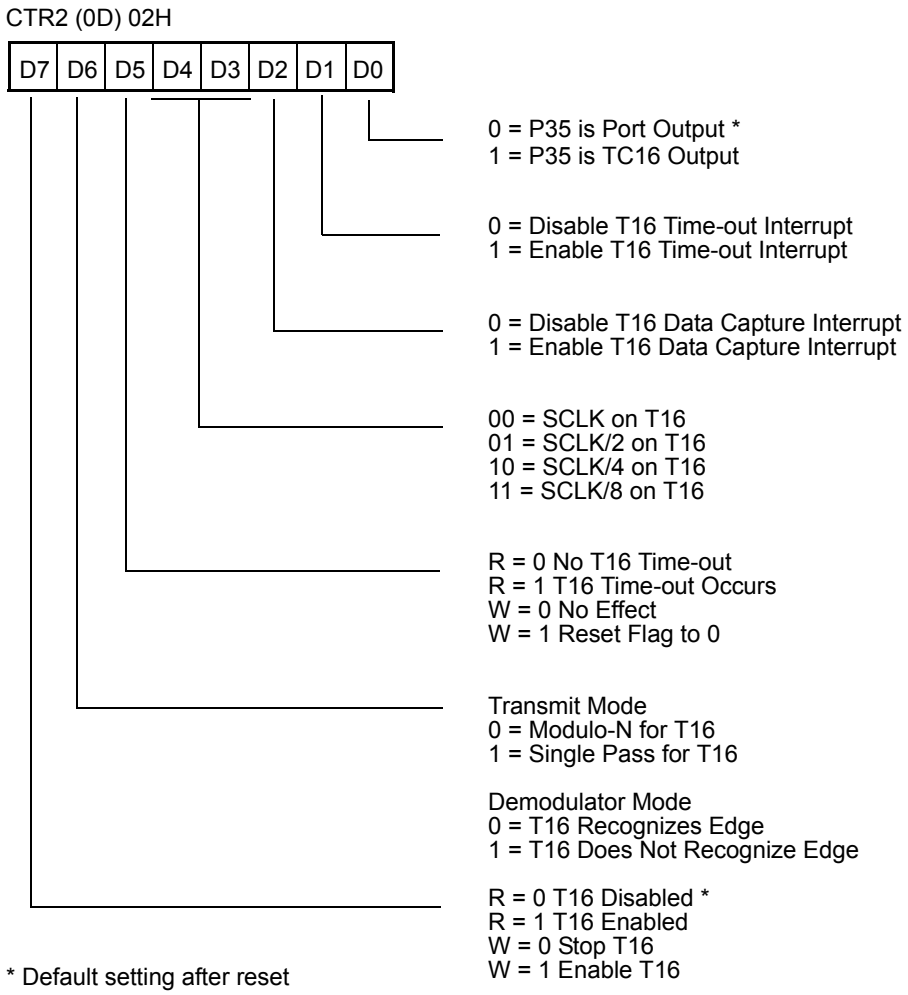


Figure 51. T16 Control Register—(0D) 2H: Read/Write Except Where Noted

Expanded Register File Control Registers (0F)

Figure 52 through Figure 57 show the expanded register file control registers (0F).

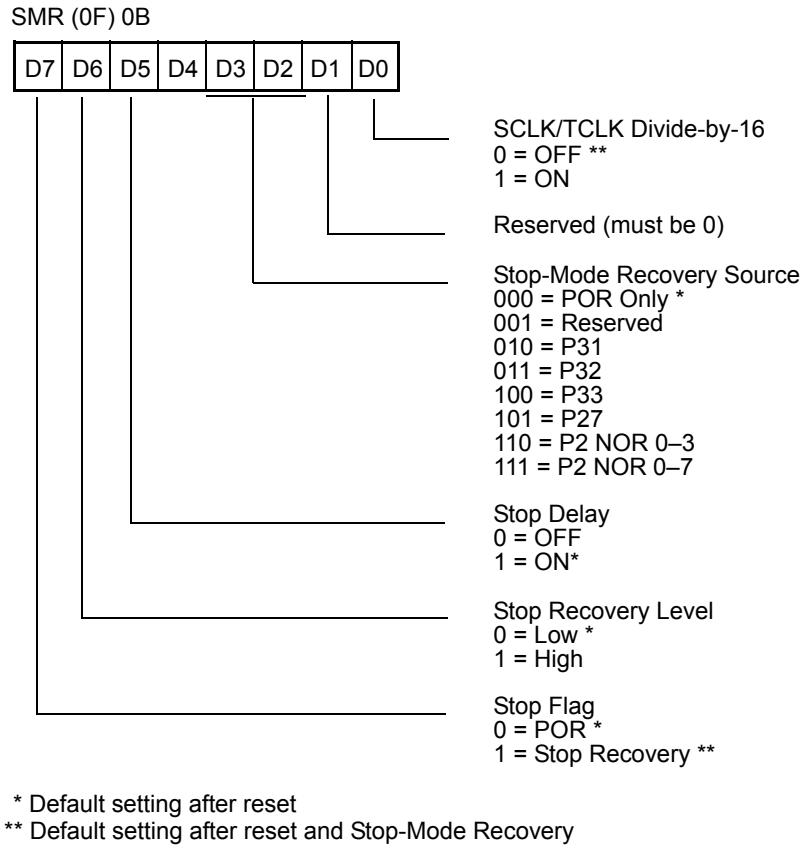
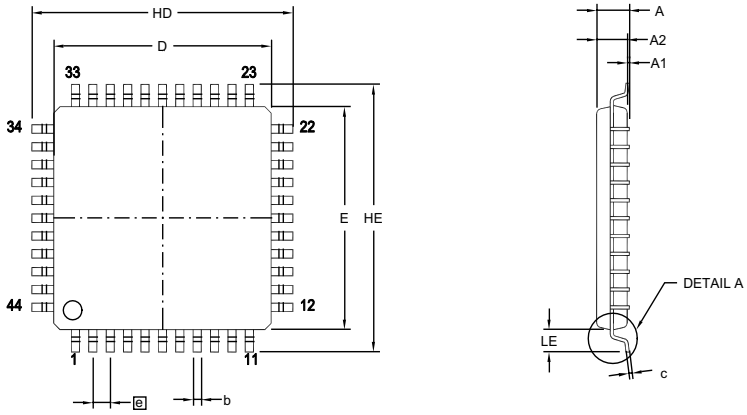


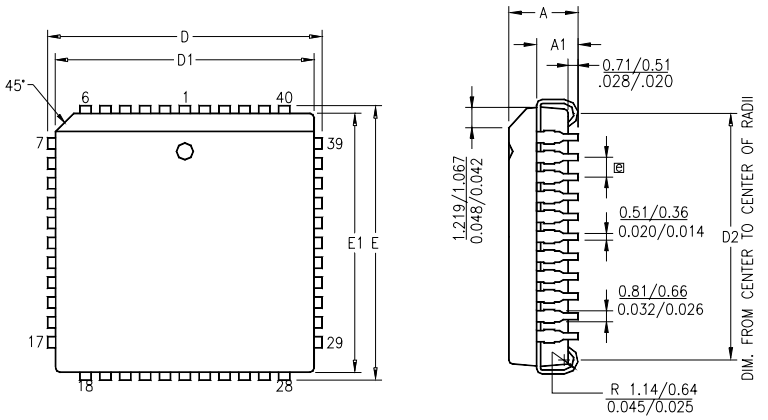
Figure 52. Stop-Mode Recovery Register—(F) 0BH: D6–D0=Write Only, D7=Read Only



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.40	1.60	0.055	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.30	0.45	0.012	0.018
c	0.09	0.20	0.004	0.008
HD	11.75	12.25	0.463	0.482
D	9.90	10.10	0.390	0.398
HE	11.75	12.25	0.463	0.482
E	9.90	10.10	0.390	0.398
e	0.80 BSC		0.031 BSC	
L	0.45	0.75	0.018	0.030
LE	1.00 REF		0.039 REF	

1. CONTROLLING DIMENSIONS : mm
2. MAX. COPLANARITY : .10mm / 0.004"

Figure 68. 44-Pin LQFP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 BSC		0.050 BSC	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM
INCH

Figure 69. 44-Pin PLCC Package Diagram

Ordering Information

Table 33 lists the ordering codes for the 16-MHz Z86E72/73.

Table 33. Ordering Codes

40-Pin DIP	44-Pin PLCC	44-Pin LQFP
Z86E7216PSC	Z86E7216VSC	Z86E7216ASC
Z86E7316PSC	Z86E7316VSC	Z86E7316ASC

Figure 70 shows an example of what the ordering codes represent.

Example:

Z 86E73 16 P S C is a Z86E73, 16 MHz, DIP, 0 °C to +70 °C, Plastic Standard

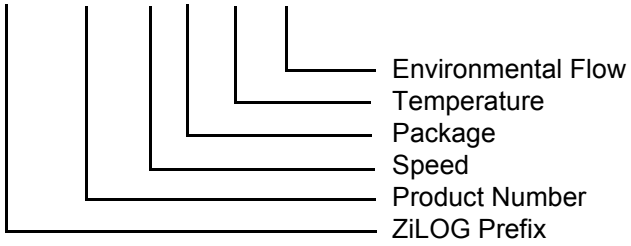


Figure 70. Ordering Codes Example

For fast results, contact your local ZiLOG sales office for assistance in ordering the part wanted.

Package

P = Plastic DIP
A = Low-profile Quad Flat Pack
V = Plastic Chip Carrier

Temperature

S = 0 °C to +70 °C

Speed

16 = 16 MHz

Environmental

C = Plastic Standard