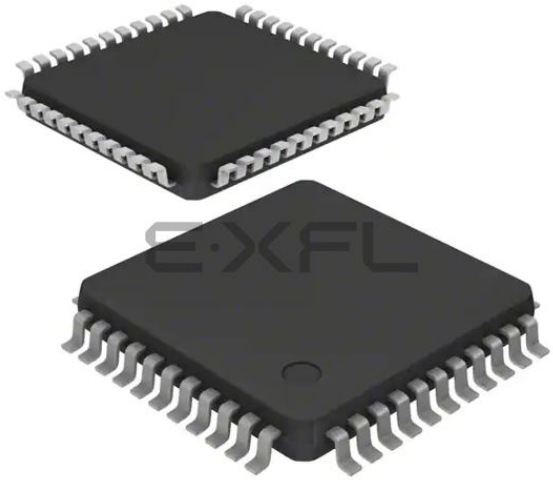

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e7316fsc00tr

Warning: DO NOT USE IN LIFE SUPPORT

LIFE SUPPORT POLICY

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As used herein

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

Document Disclaimer

Features

Table 1 lists some of the features of the Z86E72/73 microcontrollers.

Table 1. Z86E72/73 Features

Part	ROM (KB)	RAM* (Bytes)	I/O	Voltage Range
Z86E73	32	236	31	3.0 V to 5.5 V
Z86E72	16	748	31	3.0 V to 5.5 V

Note: *General-purpose

- Low power consumption—60 mW (typical)
- Two standby modes (typical)
  - STOP—2 μA
  - HALT—0.8 mA
- Special architecture to automate both generation and reception of complex pulses or signals:
  - One programmable 8-bit counter/timer with two capture registers
  - One programmable 16-bit counter/timer with one capture register
  - Programmable input glitch filter for pulse reception
- Five priority interrupts
  - Three external
  - Two assigned to counter/timers
- Two independent comparators with programmable interrupt polarity
- On-chip oscillator that accepts a crystal, ceramic resonator, LC, RC (mask option), or external clock drive
- Software-selectable 200±50% KΩ resistive transistor pull-ups on Port 0 and Port 2
  - Port 2 pull-ups are bit selectable
  - Pull-ups automatically disabled as outputs
- Software mouse/trackball interface on P00 through P03

Table 8. DC Characteristics (Continued)

			T_A = 0 °C to +70 °C		Typical		
Sym.	**Parameter**	**V_{CC}**	**Min**	**Max**	**@ 25°C**	**Units**	**Conditions**
I_{IR}	Reset Input Current	3.0 V 5.5 V		–230 –400	–50 –80	µA µA	
I_{CC}	Supply Current (WDT off)	3.0 V 5.5 V		10 15	4 10	mA mA	@ 8.0 MHz @ 8.0 MHz
I_{CC1}	Standby Current (WDT Off)	3.0 V		3	1	mA	HALT Mode V_{IN} = 0 V, V_{CC} at 8.0 MHz, Notes 1, 2
		5.5 V		5	4	mA	HALT Mode V_{IN} = 0 V, V_{CC} @ 8.0 MHz, Notes 1, 2
		3.0 V		2	0.8	mA	Clock Divide-by-16 @ 8.0 MHz Notes 1, 2
		5.5 V		4	2.5	mA	Clock Divide-by-16 @ 8.0 MHz Notes 1, 2
I_{CC2}	Standby Current	3.0 V		8	2	µA	STOP Mode V_{IN} = 0 V, V_{CC} WDT is not Running Notes 3, 5, 9
		5.5 V		10	3	µA	STOP Mode V_{IN} = 0 V, V_{CC} WDT is not Running Notes 3, 5, 9
		3.0 V		500	310	µA	STOP Mode Notes 3, 5
		5.5 V		800	600	µA	V_{IN} = 0 V, V_{CC} WDT is Running
V_{ICR}	Input Common Mode Voltage Range	3.0 V 5.5 V	0 0	V_{CC}–1.0 V V_{CC}–1.0 V	V V		Note 8
V_{LV}	VCC Low-Voltage Detection			2.9 V	2.55 V		Note 6
T_{POR}	Power-On Reset	3.0 V 5.5 V	12 5	75 20	18 7	ms ms	

Table 8. DC Characteristics (Continued)

Sym.	Parameter	V_{CC}	T_A = 0 °C to +70 °C Min	Max	Typical @ 25°C	Units	Conditions
V_{RAM}	Static RAM Data Retention Voltage	Vram			0.5	V	Worst case 0.8 V guaranteed by design only Note 6

Notes:	ICC1	Typ	Max	Unit	Frequency
	Crystal/Resonator	3.0 mA	5	mA	8.0 MHz
	External Clock Drive	0.3 mA	5	mA	8.0 MHz

1. All outputs unloaded, inputs at rail
2. CL1 = CL2 = 100 pF
3. Same as note [4] except inputs at V_{CC}
4. The V_{LV} increases as the temperature decreases.
5. Oscillator stopped
6. Oscillator does not stop when V_{CC} falls below V_{LV} threshold.
7. 32 kHz clock driver input
8. For analog comparator, inputs when analog comparators are enabled
9. WDT, Comparators, Low Voltage Detection, and ADC (if applicable) are disabled. The IC might draw more current if any of the above peripherals is enabled.

* All outputs excluding P00, P01, P36, and P37

Pin Functions

/DS (Output, Active Low)

Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available before the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS (Output, Active Low)

Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant, crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

R//W Read/Write (Output, Write Low)

The R//W signal is Low when the CCP is writing to the external program or data memory.

R//RL (Input)

This pin, when connected to GND, disables the internal ROM and forces the device to function as a ROMless Z8.

Note: When left unconnected or pulled high to V_{CC}, the part functions normally as a Z8 ROM version.

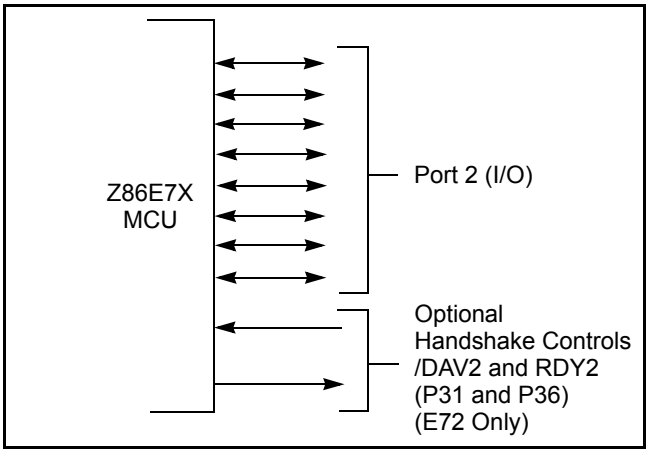
Port 0 (P07–P00)

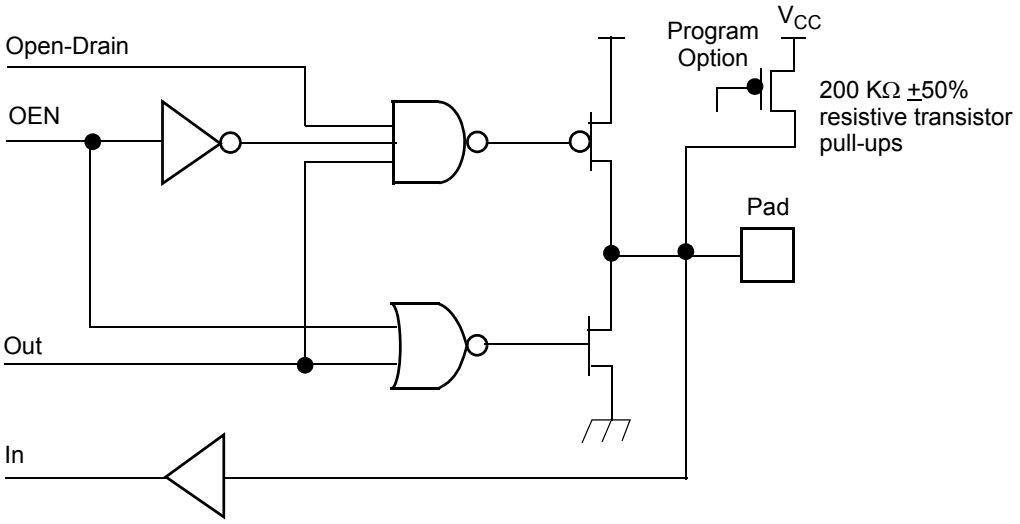
Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port or as an address port for interfacing external memory. The output drivers are push-pull. Port 0 is placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0. Handshake signal direction is

Figure 15. Port 1 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 16). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A software option is available to connect eight 200 KΩ (±50%) pull-up resistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. Port 2 can be placed under handshake control. In this configuration, Port 3 lines, P31 and P36 are used as the handshake controls lines /DAV2 and RDY2. The handshake signal assignment for Port 3, lines P31 and P36 is dictated by the direction (input or output) assigned to Bit 7, Port 2.





ming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge-triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge-detection circuit is through P31 or P20 (see “CTR1(D)01h Register” on page 48).

Port 3 provides the following control functions: handshake for Ports 0, 1, and 2 (/DAV and RDY); three external interrupt request signals (IRQ2–IRQ0); Data Memory Select (/DM). See Table 12.

Table 12. Pin Assignments

Pin	I/O	C/T	Comp.	Int.	P0 HS	P1 HS	P2 HS	Ext
Pref1	IN		RF1					
P31	IN	IN	AN1	IRQ2			D/R	
P32	IN		AN2	IRQ0	D/R			
P33	IN		RF2	IRQ1		D/R		
P34	OUT	T8	A01			R/D		D/M
P35	OUT	T16			R/D			
P36	OUT	T8/16					R/D	
P37	OUT		A02					
P20	I/O	IN						

Notes:
HS = Handshake Signals
D = /DAV
R = RDY

Port 3 also provides output for each of the counter/timers and the AND/OR Logic. Control is performed by programming bits D5–D4 of CTRI, bit 0 of CTR0, and bit 0 of CTR2.

Comparator Inputs

In Analog Mode, Port 3 (P31 and P32) has a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as shown in Figure 18. In digital mode, P33 is used as D3 of the Port 3 input register which then generates IRQ1 as shown in Figure 23.

Note: Comparators are disabled/powered down by entering STOP Mode. For P31–P33 to be used as a Stop-Mode recovery source, these inputs must be placed into digital mode.

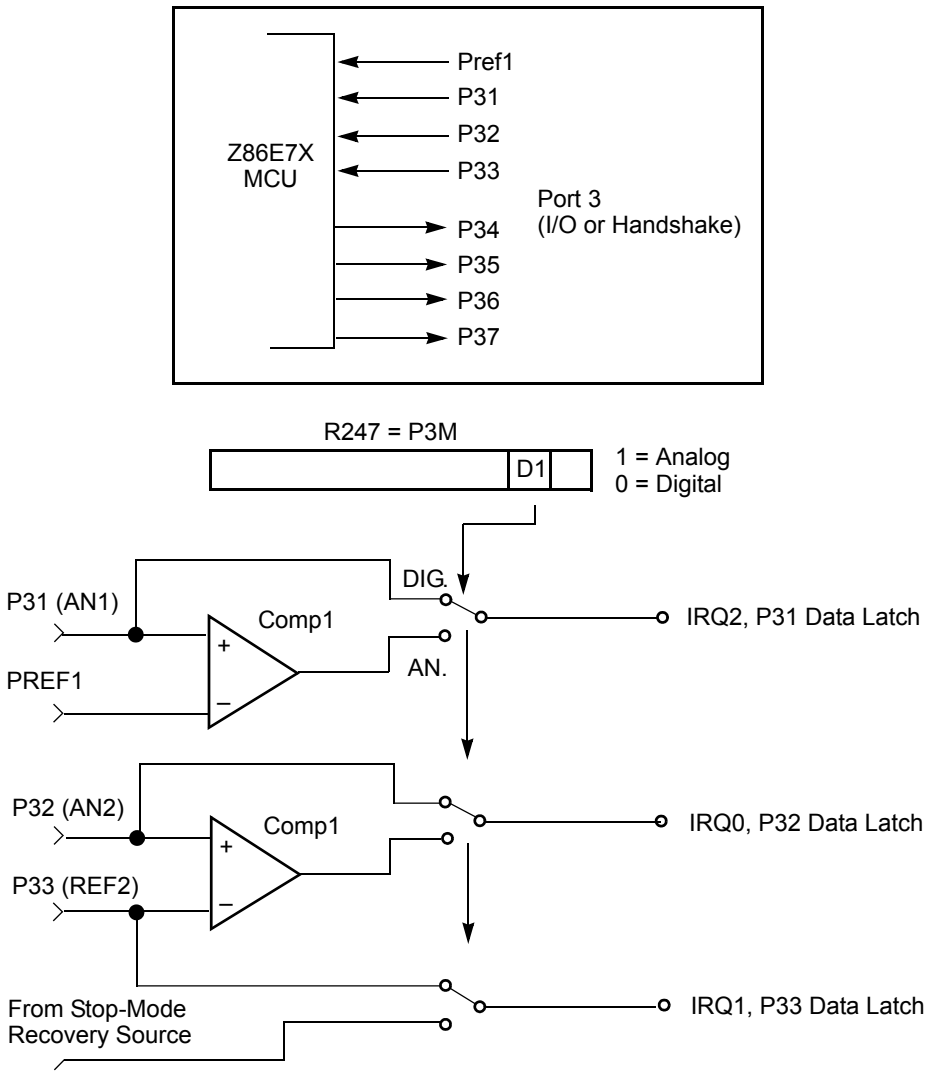
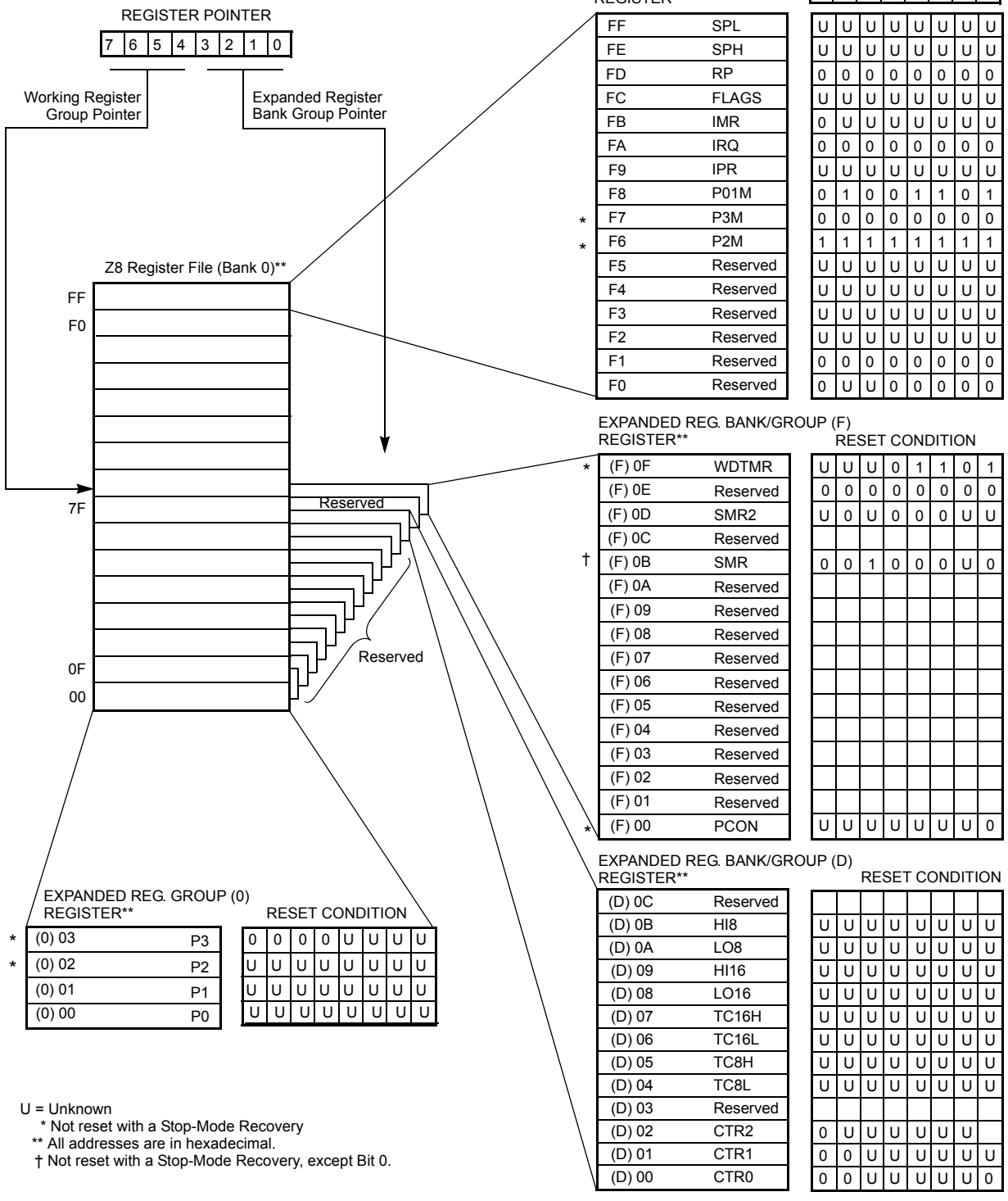


Figure 18. Port 3 Configuration

Comparator Outputs

These outputs can be programmed to be output on P34 and P37 through the PCON register (Figure 19).



U = Unknown
* Not reset with a Stop-Mode Recovery
** All addresses are in hexadecimal.
† Not reset with a Stop-Mode Recovery, except Bit 0.

Figure 22. Expanded Register File Architecture

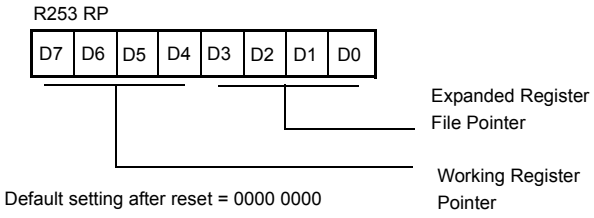


Figure 23. Register Pointer

Register File

The register file (bank 0) consists of 4 I/O port registers, 236 general-purpose registers, and 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), plus two expanded registers groups (Banks D and F). Instructions can access registers directly or indirectly through an 8-bit address field. This allows a short, 4-bit register address using the register pointer (Figure 24). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The register pointer addresses the starting location of the active working register group.

Note: Working register group E0–EF of Bank 0 are only accessed through working registers and indirect addressing modes.

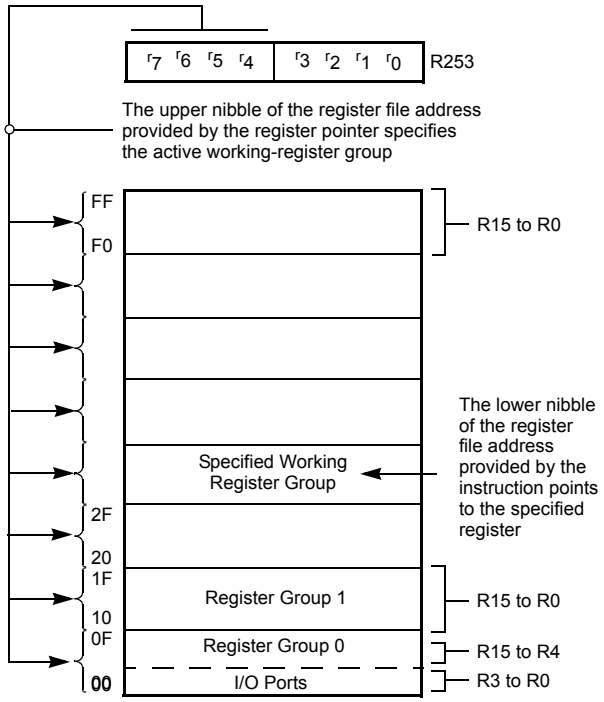


Figure 24. Register Pointer

Stack

The Z86E7X external data memory or the internal register file is used for the stack. An 8-bit stack pointer (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH is used as a general-purpose register only when using internal stacks.

Note: When SPH is used as a general-purpose register and Port 0 is in address mode, the contents of SPH are loaded into Port 0 whenever the internal stack is accessed.

Counter/Timer Register Description

Table 13 describes the expanded register group D.

Table 13. Expanded Register Group D

(D) 0Ch	Reserved
(D) 0Bh	HI8
(D) 0Ah	LO8

In demodulation mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge, but ignores the subsequent edges. For details, see “T16 Demodulation Mode” on page 60.

Time_Out

This bit is set when T16 times out (terminal count reached). To reset it, a 1 must be written to this location.

T16_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask

Set this bit to allow interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask

Set this bit to allow interrupt when T16 times out.

P35_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

SMR2(F)0Dh Register

Table 25 describes Stop-Mode Recovery Register 2.

Table 25. SMR2(F)0Dh Register

Field	Bit Position		Value	Description
Reserved	7-------		0	Reserved (Must be 0)
Recovery Level	-6------	W	0* 1	Low High
Reserved	--5-----		0	Reserved (Must be 0)
Source	---432--	W	000* 001 010 011 100 101 110 111	A. POR Only B. NAND of P23–P20 C. NAND or P27–P20 D. NOR of P33–P31 E. NAND of P33–P31 F. NOR of P33–P31, P00, P07 G. NAND of P33–P31, P00, P07 H. NAND of P33–P31, P22–P20
Reserved	------10		00	Reserved (Must be 0)

Note: * Indicates the value upon Power-On Reset.

Starting Ping-Pong Mode

First, make sure both counter/timers are not running. Then set T8 into Single-Pass Mode (CTR0 D6), set T16 into Single-Pass Mode (CTR2 D6), and set Ping-Pong Mode (CTR1 D2, D3). These instructions do not have to be in any particular order. Finally, start Ping-Pong Mode by enabling either T8 (CTR0 D7) or T16 (CTR2 D7).

During Ping-Pong Mode

The enable bits of T8 and T16 (CTR0 D7, CTR2 D7) are alternately set and cleared by hardware. The time-out bits (CTR0 D5, CTR2 D5) are set every time the counter/timers reach the terminal count.

Output Circuit

Figure 36 shows the output circuit.

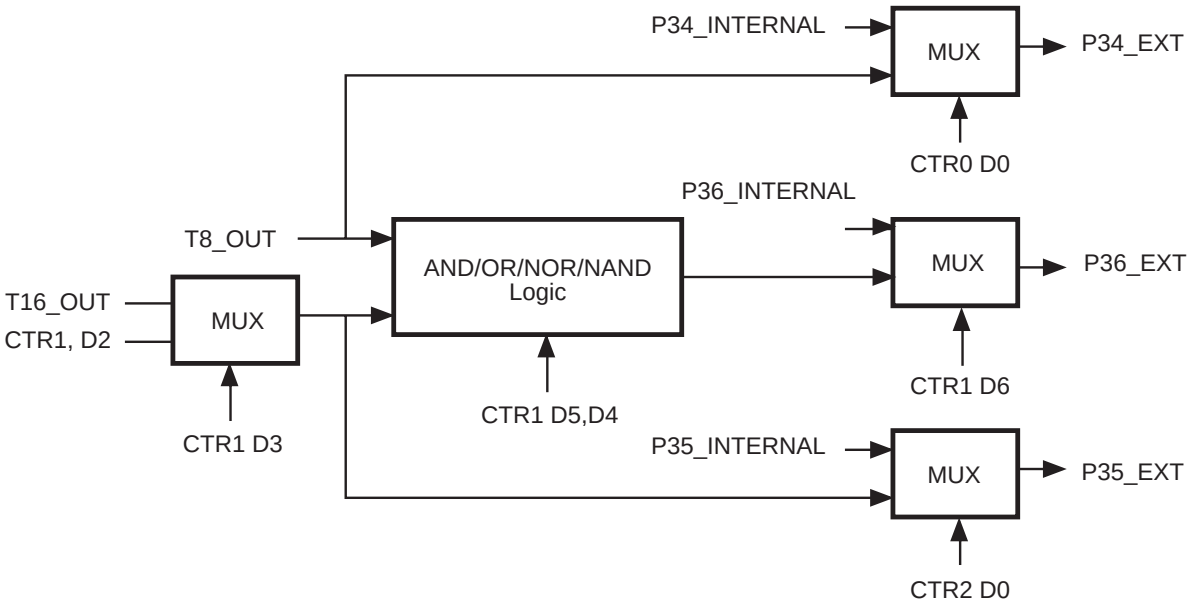


Figure 36. Output Circuit

Interrupts

The Z86E7X has five different interrupts. The interrupts are maskable and prioritized, as shown in Figure 37. The five sources are divided as follows: three sources are claimed by Port 3 lines P33–P31 and the remaining two by the counter/timers (see Table 26). The Interrupt Mask Register globally or individually enables or disables the five interrupt requests.

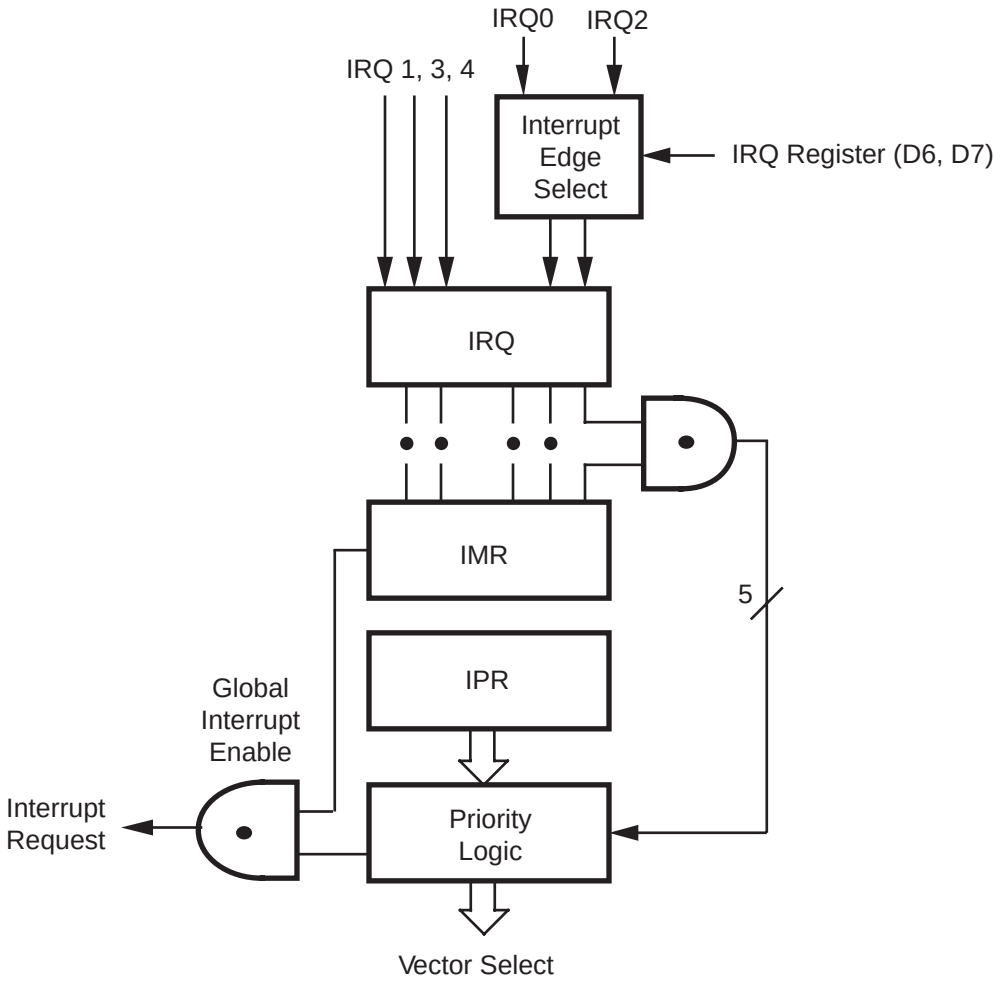


Figure 37. Interrupt Block Diagram

Table 26. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rising Falling Edge Triggered
IRQ1	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	/DAV2, IRQ2, T_{IN}	4,5	External (P31), Rising Falling Edge Triggered
IRQ3	T16	6, 7	Internal
IRQ4	T8	8, 9	Internal

Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the port to its standard I/O configuration.

Port 0 Output Mode (D2)

Bit 2 controls the output mode of Port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 40). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop-Mode Recovery signal. Bit D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

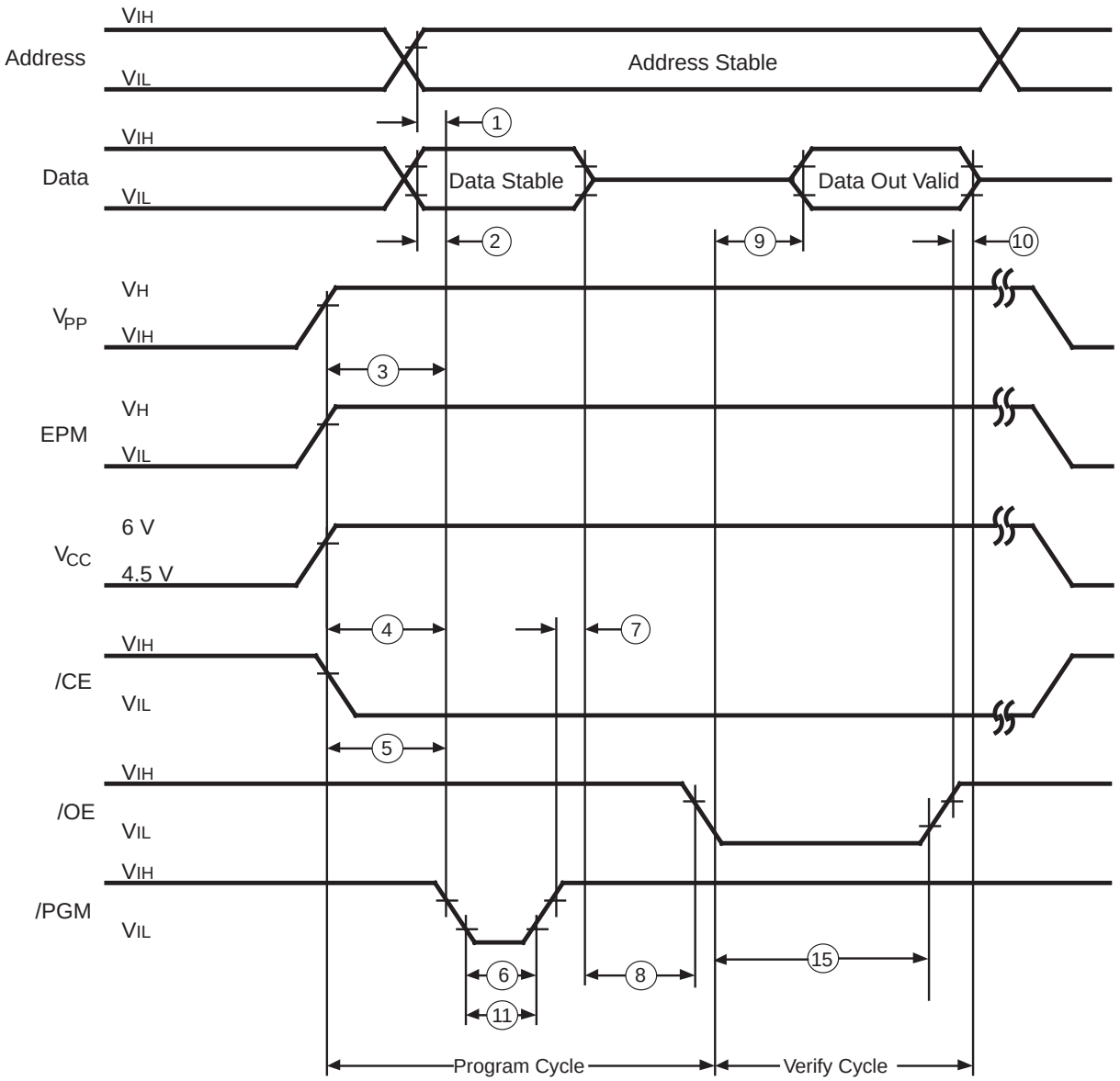


Figure 46. EPROM Program and Verify

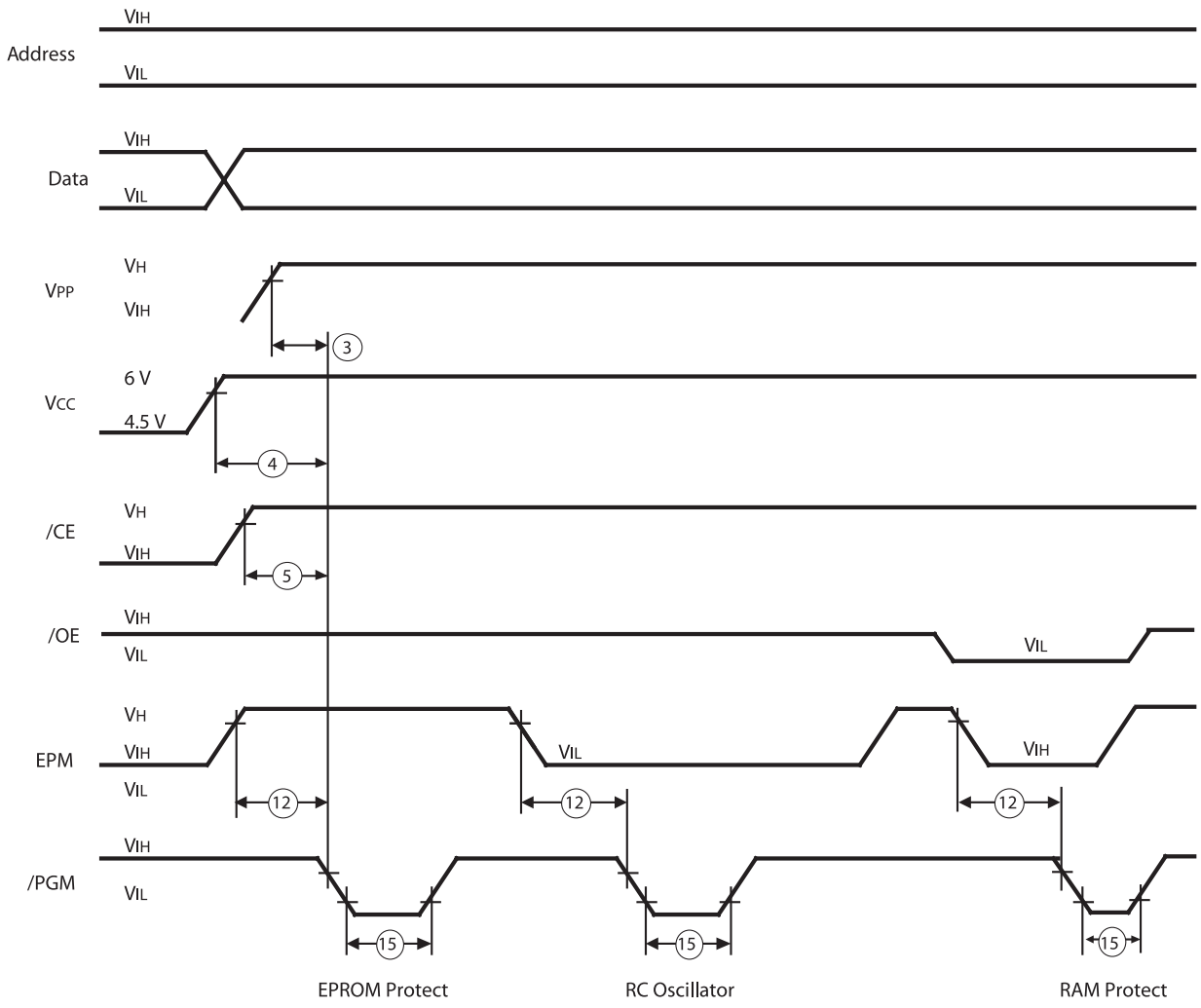


Figure 47. Programming EPROM, RAM Protect, and 16K Size Selection

Figure 48 shows the programming flowchart.

Z8 Standard Control Register Diagrams

Figure 58 through Figure 66 show the Z8 standard control register diagrams.

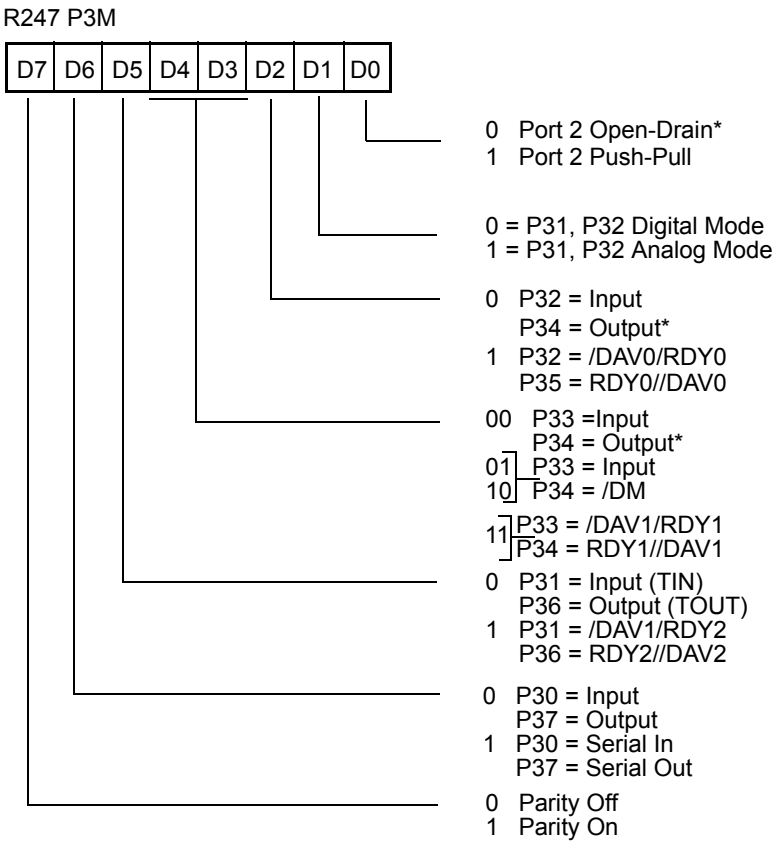
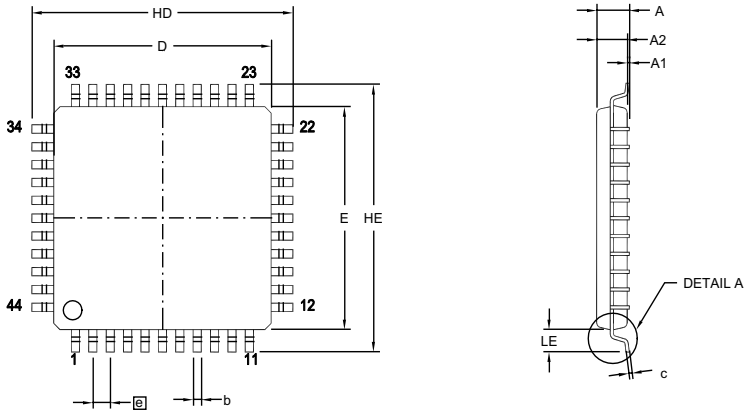


Figure 58. Port 3 Mode Register—F7H: Write Only



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.40	1.60	0.055	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.30	0.45	0.012	0.018
c	0.09	0.20	0.004	0.008
HD	11.75	12.25	0.463	0.482
D	9.90	10.10	0.390	0.398
HE	11.75	12.25	0.463	0.482
E	9.90	10.10	0.390	0.398
e	0.80 BSC		0.031 BSC	
L	0.45	0.75	0.018	0.030
LE	1.00 REF		0.039 REF	

1. CONTROLLING DIMENSIONS : mm
2. MAX. COPLANARITY : .10mm / 0.004"

Figure 68. 44-Pin LQFP Package Diagram

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