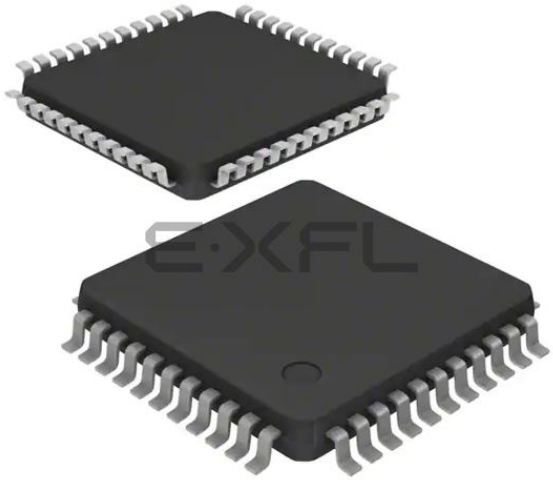

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e7316fsg

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As used herein

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

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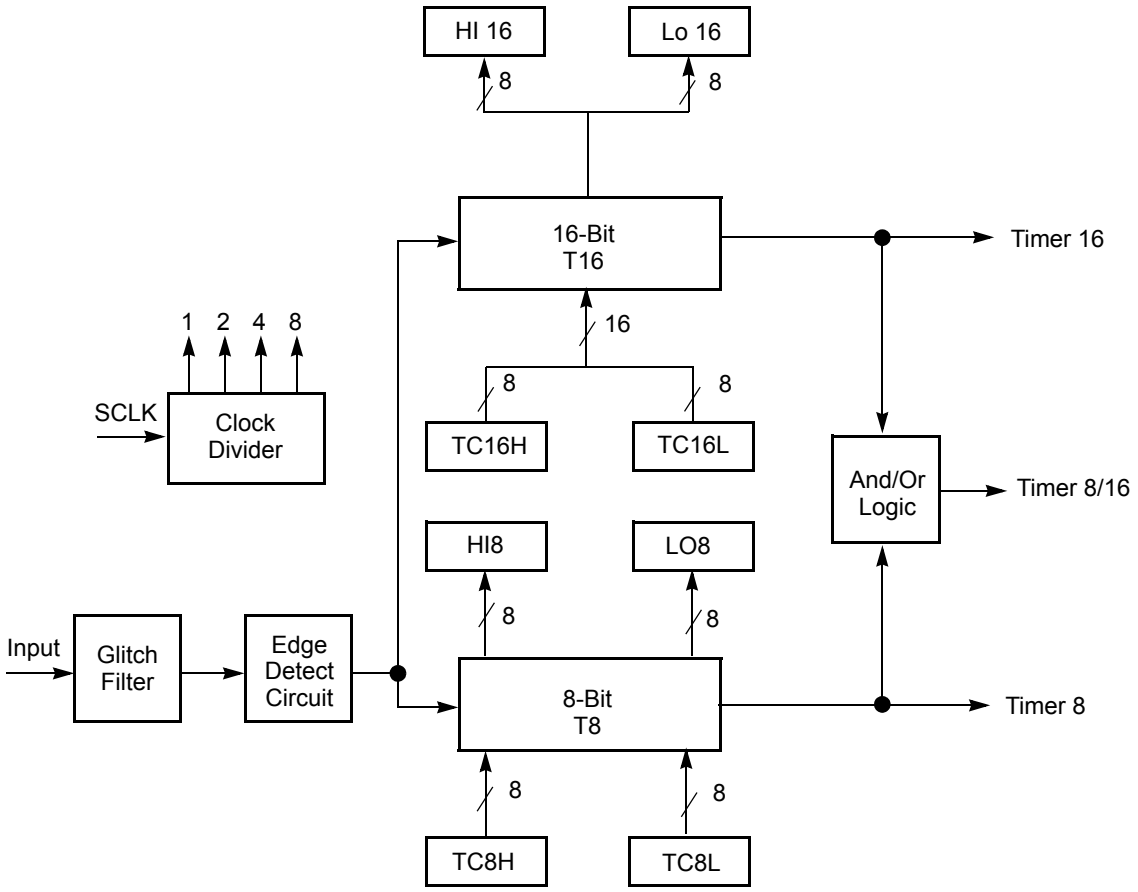


Figure 1. Z86E7X Counter/Timer Block Diagram

Power connections follow the conventions listed in Table 2.

Table 2. Power Connections

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Figure 2 displays the functional block diagram.

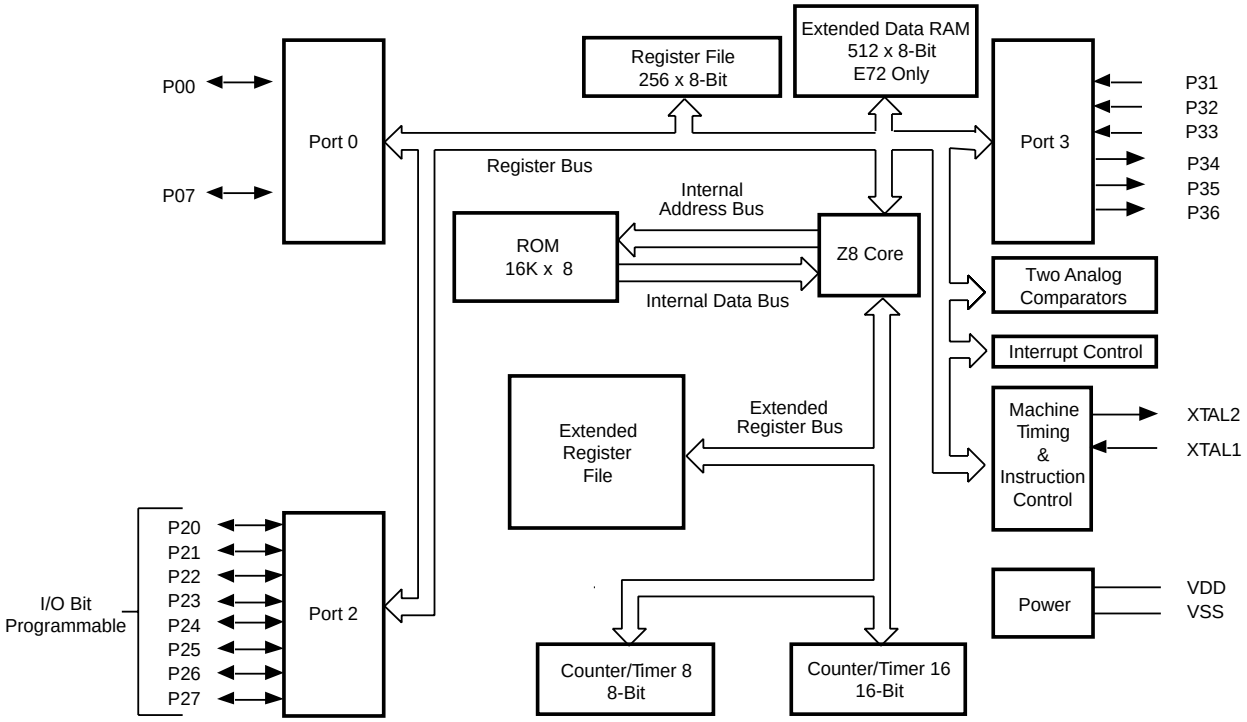


Figure 2. Z86E7X Functional Block Diagram

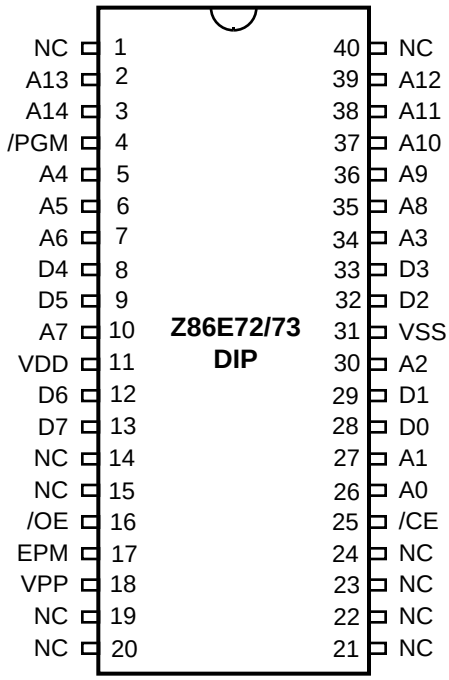


Figure 4. 40-Pin DIP Pin Assignments (EPROM Mode)

Figure 5 on page 7 shows the pin assignments for the standard mode of the 44-pin plastic leaded chip carrier (PLCC). Figure 6 on page 7 displays the pin assignments for the EPROM mode of the 44-pin PLCC.

Table 3. Pin Identification (Standard Mode) (Continued)

40-Pin DIP #	44-Pin PLCC #	44-Pin LQFP #	Symbol	Direction	Description
14	27	10	XTAL2	Output	Crystal, Oscillator Clock
11	23, 24	6, 7	V_{DD}		Power Supply
31	1, 2, 34	17, 28, 29	V_{SS}		Ground
25	39	22	Pref1	Input	Comparator 1 Reference
NC	12	39	R//RL	Input	ROM//ROMless

Table 4. Z86E72/73 40-Pin DIP Identification—EPROM Mode

40-Pin #	Symbol	Function	Direction
1	N/C	Not Connected	
2–3	A13–14	Address 13, 14	Input
4	/PGM	Program Mode	Input
5–7	A4–A6	Address 4, 5, 6	Input
8–9	D4–D5	Data 4, 5	Input/Output
10	A7	Address 7	Input
11	V_{DD}	Power Supply	
12–13	D6–D7	Data 6, 7	Input/Output
14–15	N/C	Not Connected	
16	/OE	Output Enable	Input
17	EPM	EPROM Prog. Mode	Input
18	V_{PP}	Prog. Voltage	Input
19–24	N/C	Not Connected	
25	/CE	Chip Enable	Input
26–27	A0–A1	Address 0, 1	Input
28–29	D0–D1	Data 0, 1	Input/Output
30	A2	Address 2	Input
31	V_{SS}	Ground	
32–33	D2–D3	Data 2, 3	Input/Output

Table 5. Z86E72/73 44-Pin LQFP/PLCC Pin Identification—EPROM Mode

44-Pin LQFP	44-Pin PLCC	Symbol	Function	Direction
41–42	14–15	A13–A14	Address 13, 14	Input
43	16	/PGM	Prog. Mode	Input
44	17	A4	Address 4	Input

Absolute Maximum Ratings

Table 6 lists the absolute maximum ratings for the Z86E72/73 microcontrollers.

Table 6. Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
V_{MAX}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temperature	–65°	+150°	C
T_A	Oper. Ambient Temperature		†	C

Notes:
* Voltage on all pins with respect to GND.
† See “Ordering Information” on page 97.

Stresses greater than those listed under Absolute Maximum Ratings might cause permanent damage to the device. This rating is a stress rating only. Operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

dictated by the I/O direction to Port 0 of the upper nibble P07–P04. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 can provide address bits A11–A8 (lower nibble) or A15–A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

Port 0 is set in the High-Impedance Mode if selected as an address output state along with Port 1 and the control signals /AS, /DS, and R//W.

A software option is available to program 0.4 V_{DD} CMOS trip inputs on P00–P03. This allows direct interface to mouse/trackball IR sensors.

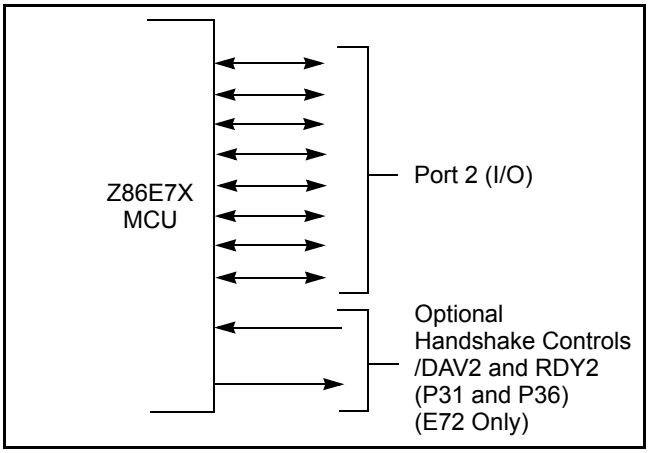
An optional 200±50% KΩ resistive transistor pull-up is available as a software option of all Port 0 bits with nibble select.

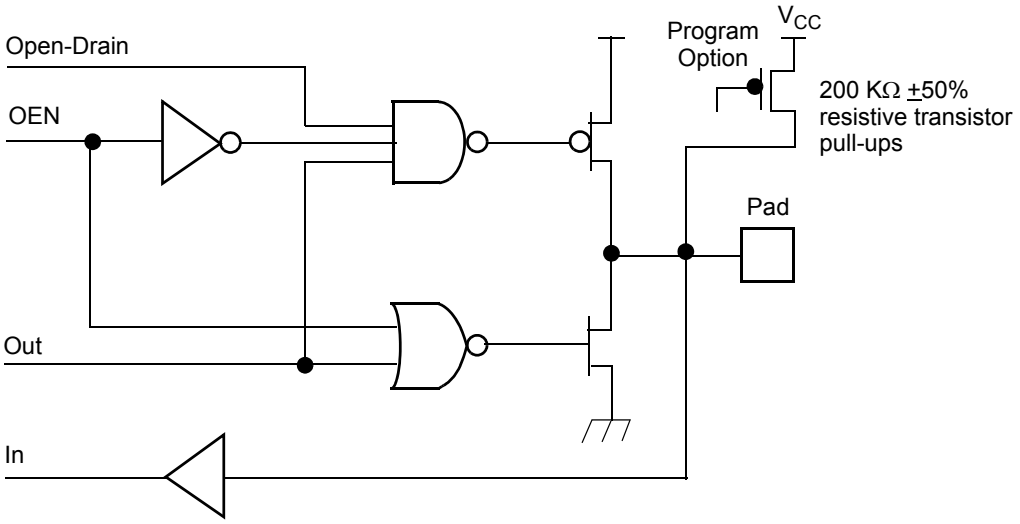
These pull-ups are disabled when configured (bit by bit) as an output. See Figure 14.

Figure 15. Port 1 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 16). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A software option is available to connect eight 200 KΩ (±50%) pull-up resistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. Port 2 can be placed under handshake control. In this configuration, Port 3 lines, P31 and P36 are used as the handshake controls lines /DAV2 and RDY2. The handshake signal assignment for Port 3, lines P31 and P36 is dictated by the direction (input or output) assigned to Bit 7, Port 2.





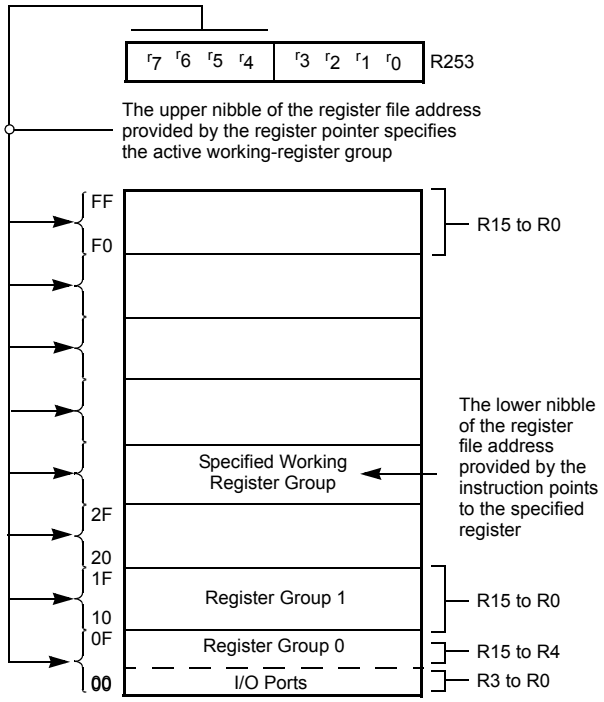


Figure 24. Register Pointer

Stack

The Z86E7X external data memory or the internal register file is used for the stack. An 8-bit stack pointer (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH is used as a general-purpose register only when using internal stacks.

Note: When SPH is used as a general-purpose register and Port 0 is in address mode, the contents of SPH are loaded into Port 0 whenever the internal stack is accessed.

Counter/Timer Register Description

Table 13 describes the expanded register group D.

Table 13. Expanded Register Group D

(D) 0Ch	Reserved
(D) 0Bh	HI8
(D) 0Ah	LO8

Table 23. CTR1(D)01h Register (Continued)

Field	Bit Position		Value	Description
Initial_T8_Out/Rising_Edge	------1-			Transmit Mode
		R/W	0	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/Falling _Edge	-------0			Transmit Mode
		R/W	0	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

Note: * Indicates the value upon Power-On Reset.

Mode

If it is 0, the counter/timers are in the transmit mode; otherwise, they are in the demodulation mode.

P36_Out/Demodulator_Input

In transmit mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In demodulation mode, this bit defines whether the input signal to the counter/timers is from P20 or P31.

T8/T16_Logic/Edge _Detect

In transmit mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In demodulation mode, this field defines which edge needs to be detected by the edge detector.

Transmit_Submode/Glitch Filter

In transmit mode, this field defines whether T8 and T16 are in the “Ping-Pong” mode or in independent normal operation mode. Setting this field to “Normal

CTR2(D)02h Register

Table 24 describes the Counter/Timer16 Control Register.

Table 24. CTR2(D)02h Register

Field	Bit Position		Value	Description
T16_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Submode/Modulo-N	-6------	R/W		Transmit Mode
			0	Modulo-N
			1	Single Pass
				Demodulation Mode
			0	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
Time_Out	--5-----	R	0	No Counter Time-Out
			1	Counter Time-Out Occurred
		W	0	No Effect
			1	Reset Flag to 0
T16 _Clock	---43---	R/W	00	SCLK
			01	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	-----2--	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	------1-	R/W	0	Disable Time-Out Int.
			1	Enable Time-Out Int.
P35_Out	-------0	R/W	0*	P35 as Port Output
			1	T16 Output on P35

Note: * Indicates the value upon Power-On Reset.

T16_Enable

This field enables T16 when set to 1.

Single/Modulo-N

In transmit mode, when set to 0, the counter reloads the initial value when terminal count is reached. When set to 1, the counter stops when the terminal count is reached.

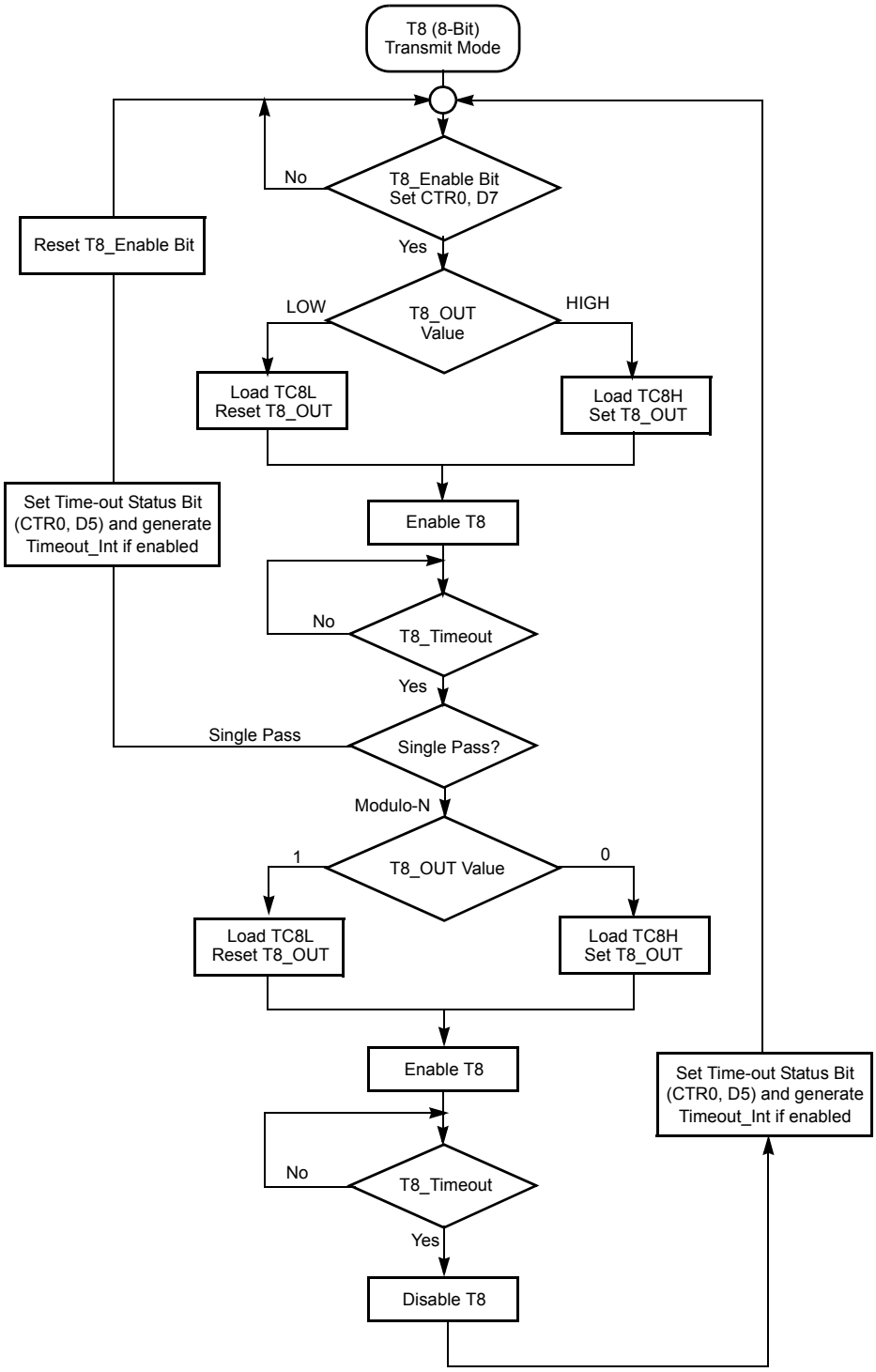


Figure 27. Transmit Mode Flowchart

If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A time out of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If D6 bit of CTR2 is toggled (by writing a 0 and then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both, depending on CTR1 D5, D4) but continues to ignore subsequent edges.

When T16 reaches 0, it continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt time-out can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in transmit mode. T8 and T16 need to be programmed in Single-Pass Mode (CTR0 D6, CTR2 D6), and Ping-Pong Mode needs to be programmed in CTR1 D3, D2. You can begin the operation by enabling either T8 or T16 (CTR0 D7 or CTR2 D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1 D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled and T16 is enabled. T16_OUT switches to its initial value (CTR1 D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, and the whole cycle repeats. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0 D1, CTR2 D1). To stop the Ping-Pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 35.

Note: Enabling Ping-Pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and then reset the status flags before instituting this operation.

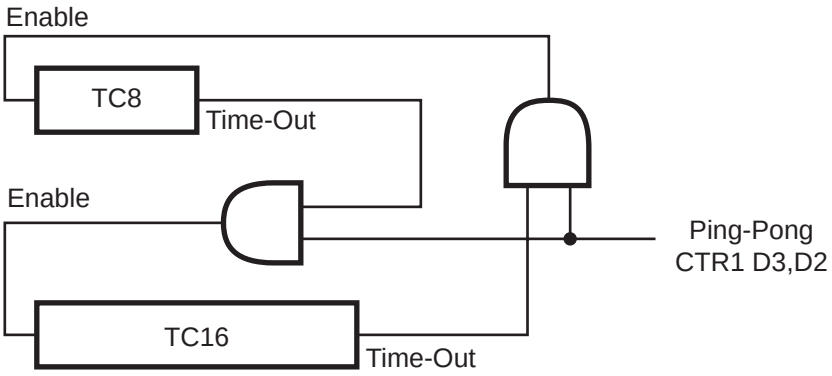


Figure 35. Ping-Pong Mode

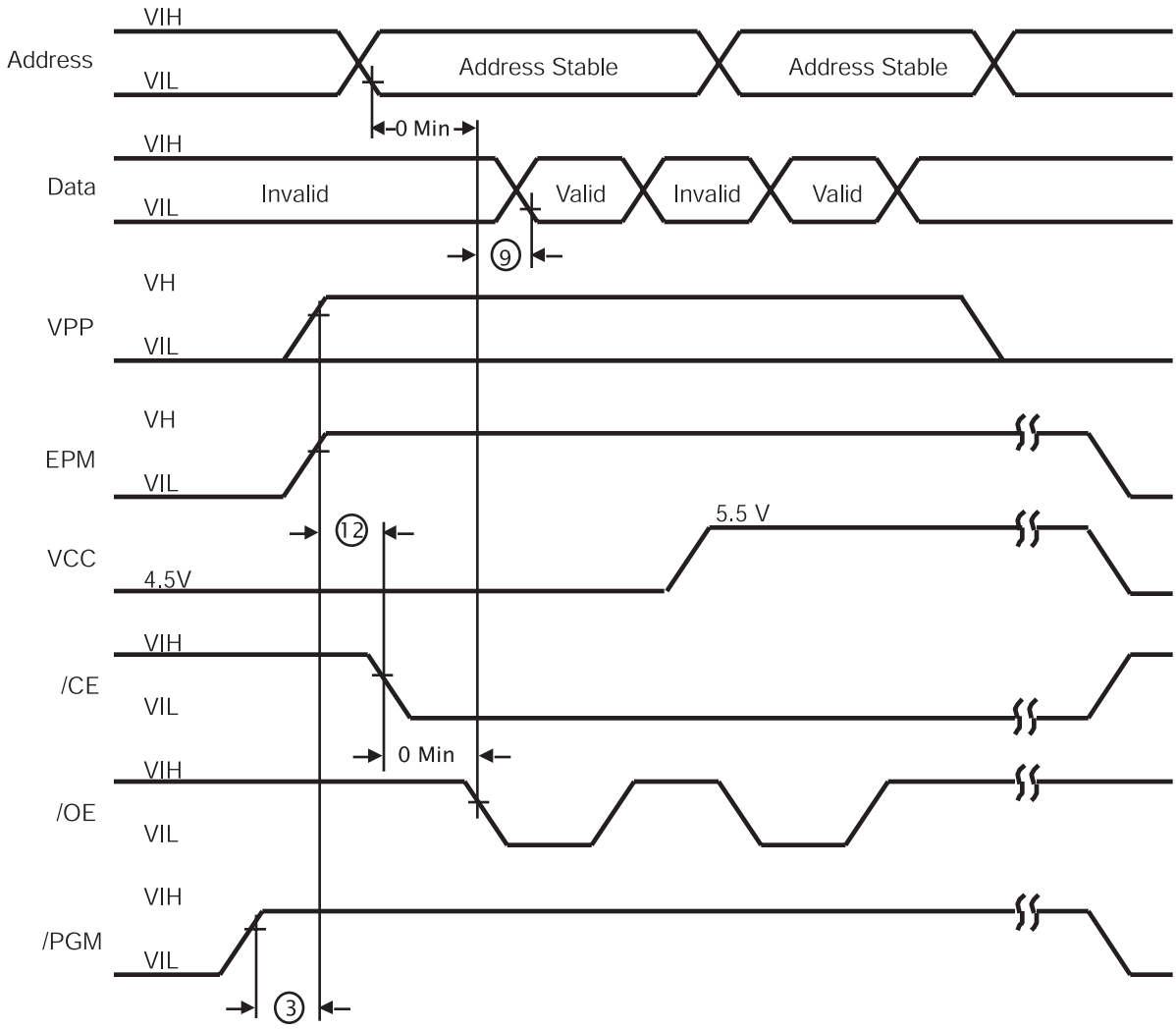


Figure 45. EPROM Read

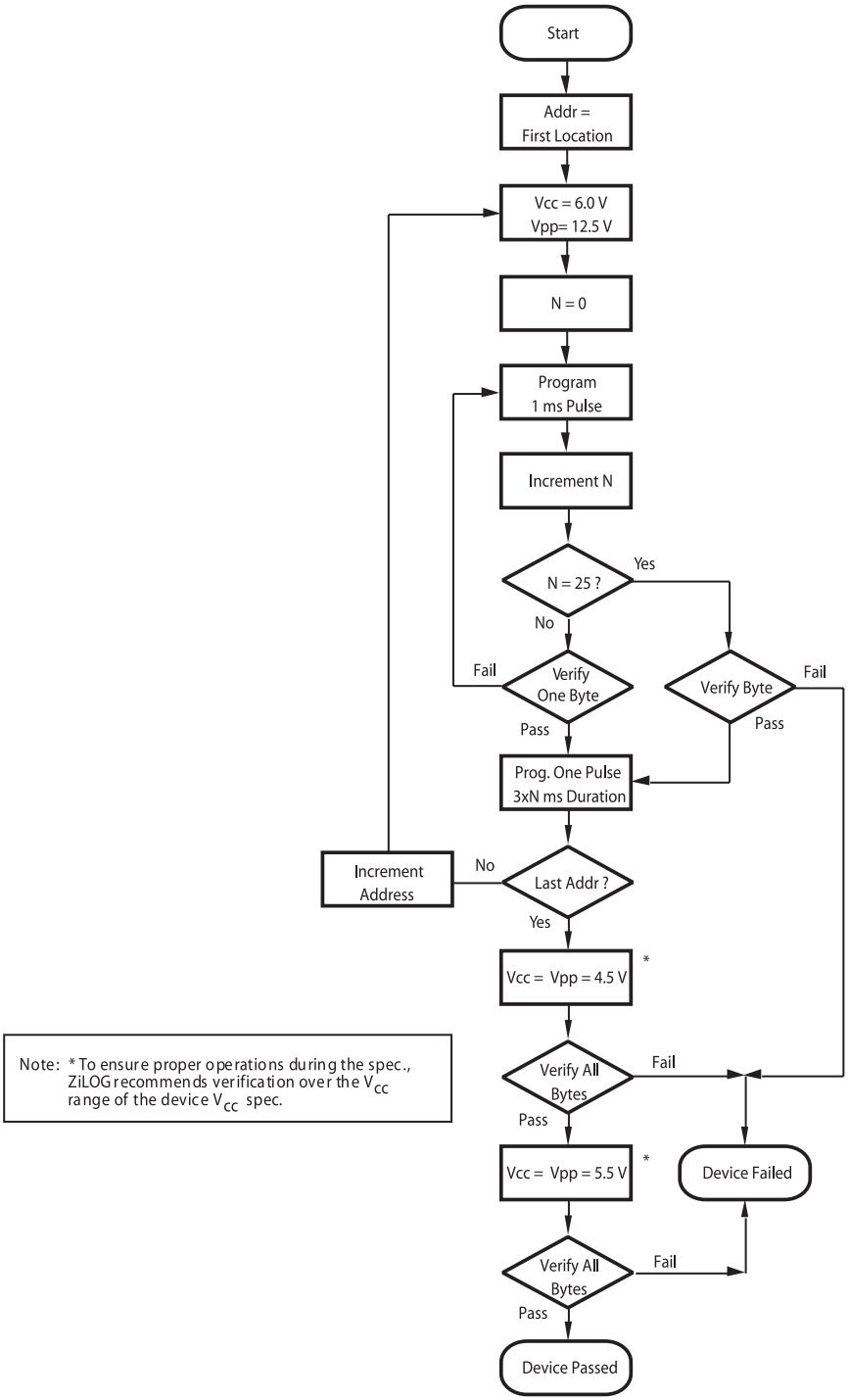


Figure 48. Programming Flowchart

Expanded Register File Control Registers (0D)

Figure 49 through Figure 51 show the expanded register file control registers (0D).

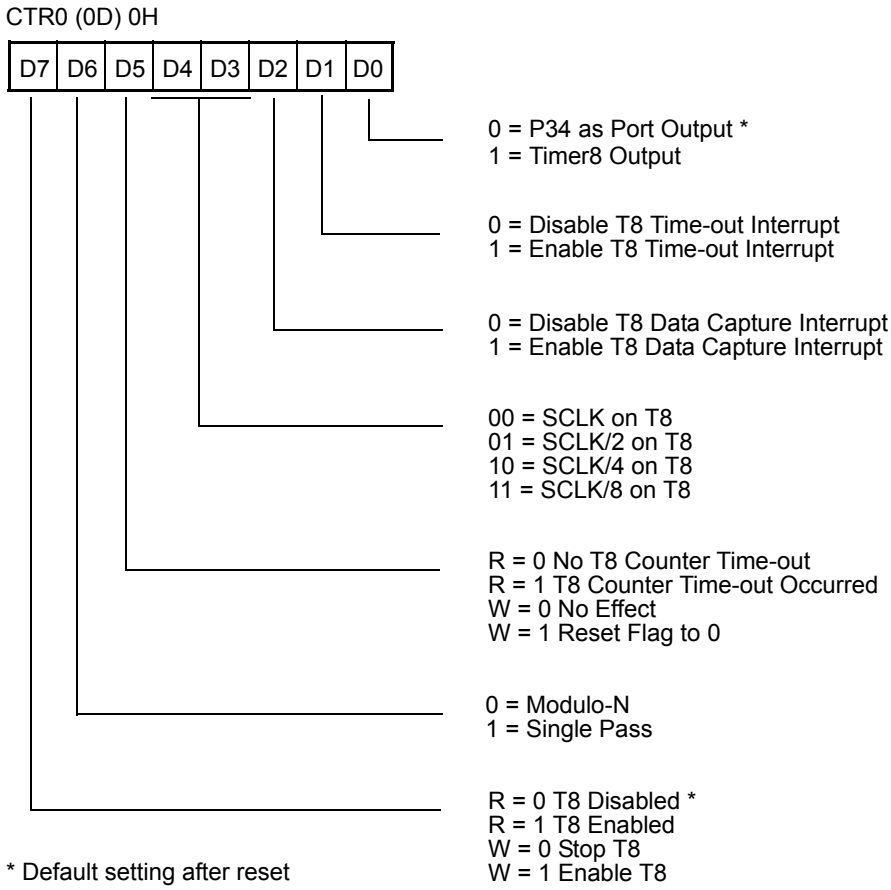


Figure 49. TC8 Control Register—(0D) 0H: Read/Write Except Where Noted

Figure 66. Stack Pointer Low—(0) FFH: Read/Write

Ordering Information

Table 33 lists the ordering codes for the 16-MHz Z86E72/73.

Table 33. Ordering Codes

40-Pin DIP	44-Pin PLCC	44-Pin LQFP
Z86E7216PSC	Z86E7216VSC	Z86E7216ASC
Z86E7316PSC	Z86E7316VSC	Z86E7316ASC

Figure 70 shows an example of what the ordering codes represent.

Example:

Z 86E73 16 P S C is a Z86E73, 16 MHz, DIP, 0 °C to +70 °C, Plastic Standard

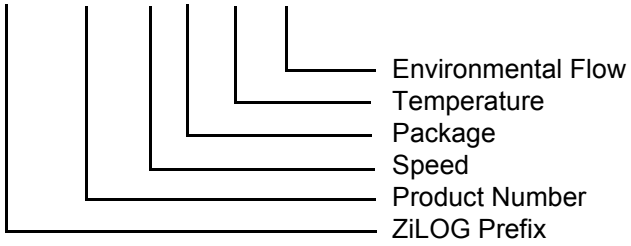


Figure 70. Ordering Codes Example

For fast results, contact your local ZiLOG sales office for assistance in ordering the part wanted.

Package

P = Plastic DIP
A = Low-profile Quad Flat Pack
V = Plastic Chip Carrier

Temperature

S = 0 °C to +70 °C

Speed

16 = 16 MHz

Environmental

C = Plastic Standard

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